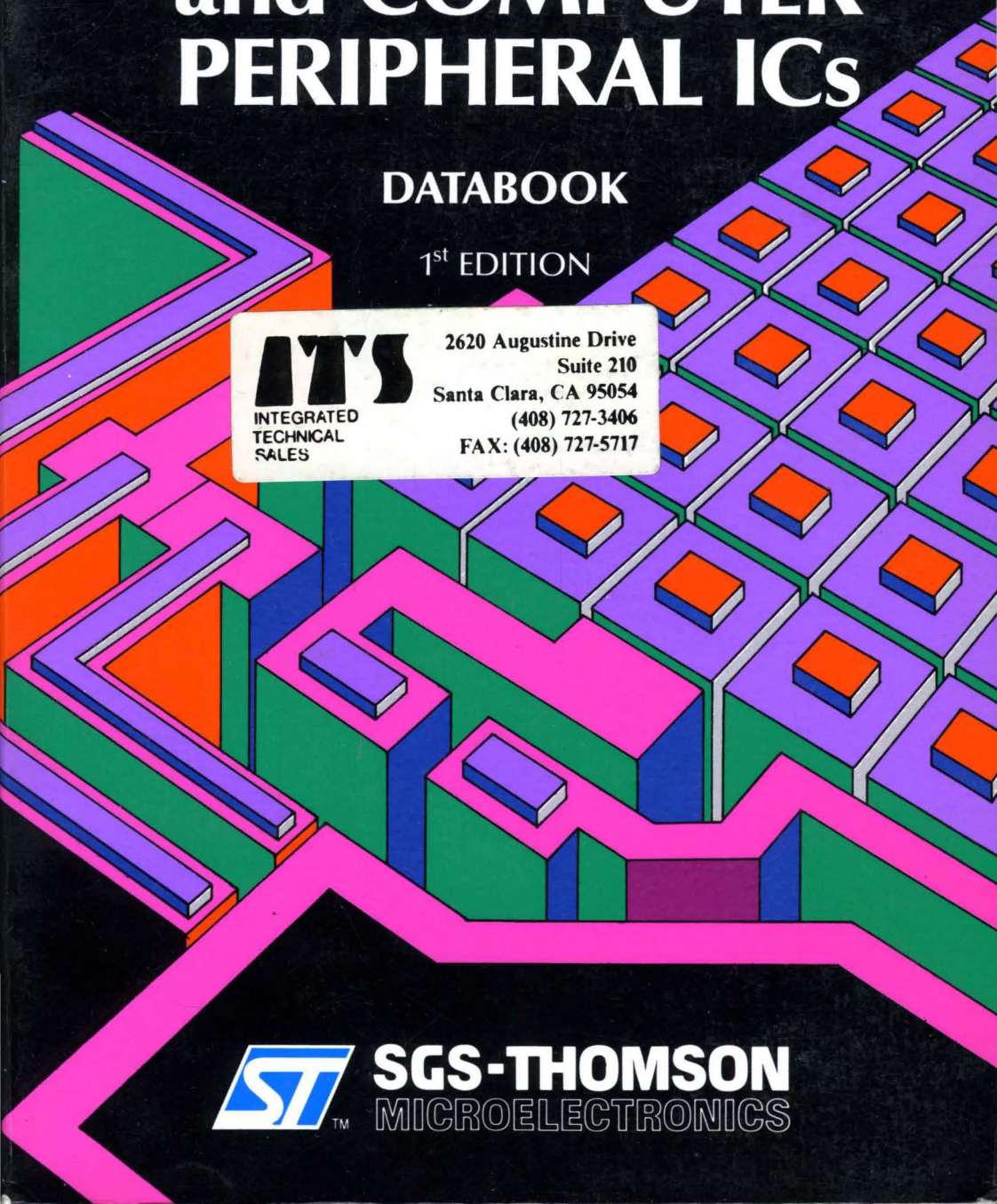
INDUSTRIAL and COMPUTER PERIPHERAL ICs

DATABOOK

1st EDITION



SGS-THOMSON MICROELECTRONICS

INDUSTRIAL AND COMPUTER PERIPHERAL ICs

DATABOOK

1st EDITION

OCTOBER 1988

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

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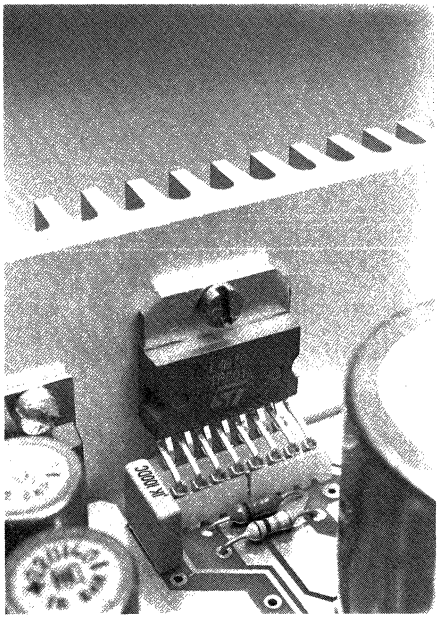
1. Life support devices or systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perfom, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

INDUSTRIAL & COMPUTER PERIPHERAL ICs FROM THE BRIGHTER POWER

Since the first high power ICs emerged at the end of the 1960s SGS-THOMSON has set the pace in power IC process technology, plastic power packages and innovative circuit design.



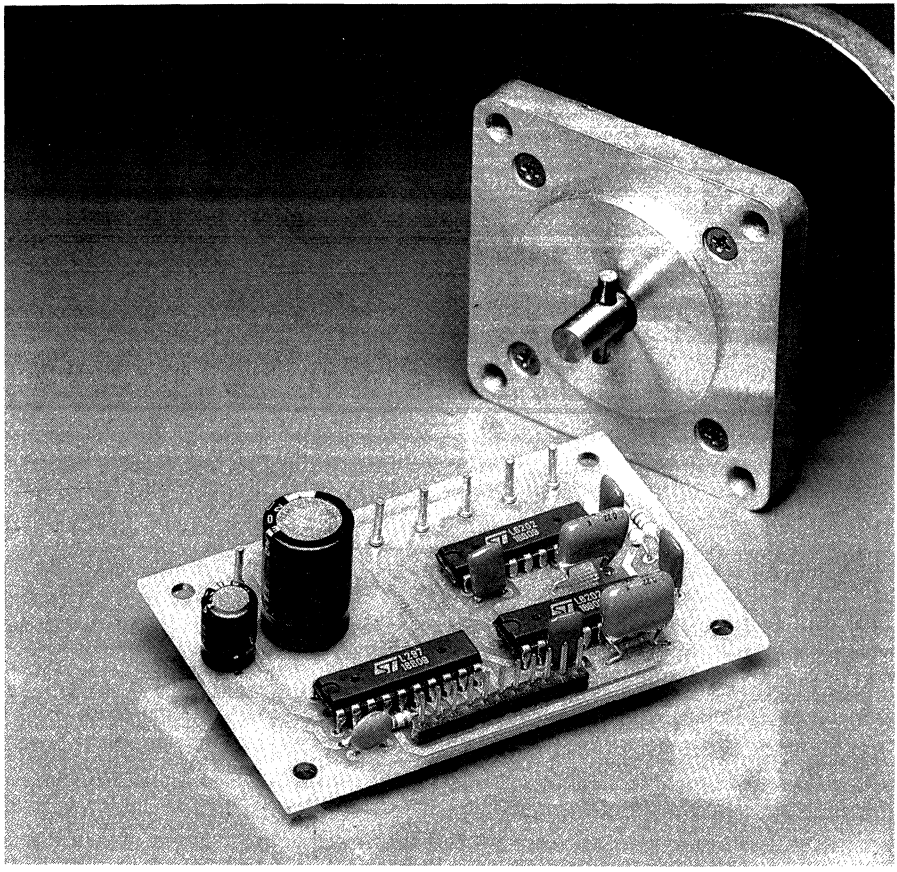
Realized with SGS-THOMSON's unique Multipower-BCD technology, the L4970 power switching regulator delivers an impressive 10A output current. A host of protection features are integrated.

Originally this technology knowhow was applied to consumer circuits such as high power amplifiers and TV vertical deflection stages, so when motor driving ICs arrived at the end of the seventies SGS-THOMSON already possessed a unique understanding of the problems involved and, more important, how they could be solved.

SGS-THOMSON is not just the leader in smart power technology, it is also the #1 supplier of smart power ICs in the western world (Dataquest, May 1988), selling more than any American or European semiconductor company.

Many of the milestones in smart power technology have been developed by SGS-THOMSON and many are still unmatched. Today's leading edge is a family of smart power technologies integrating bipolar, CMOS and DMOS on the same chip. Using this technology the company has produced a new generation of ultra-efficient power ICs that are changing the whole approach to power system design.

Just one example of the way this technology can be applied is the L6202

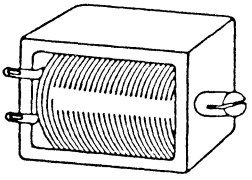


Thanks to the high efficiency of Multipower-BCD technology's DMOS power transistors, the L6202 H-bridge motor driver delivers 1.5A/48V with no heatsink.

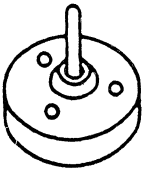
bridge driver, containing a full DMOS H-bridge power stage plus control circuits.
Because of the very high efficiency of the power stage this IC can deliver 70W to the load yet it is assembled in a DIP package.

Many more world-beating products are included in this databook: the L4970 switching regulator, L6230 brushless motor driver, L6114 quad switch, the industrial power switch family and much more. So if you're looking for the brightest solution to your industrial and computer peripheral application problems you'll find the answer right here.

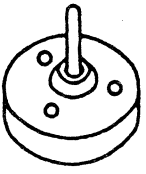
SOLENOID, HAMMER, NEEDLE, RELAY



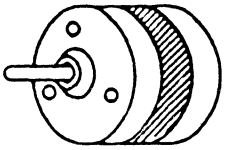
UNIPOLAR STEPPER MOTORS



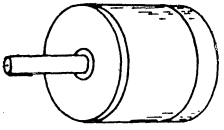
BIPOLAR STEPPER MOTORS



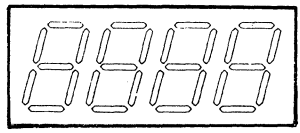
BRUSHLESS MOTORS



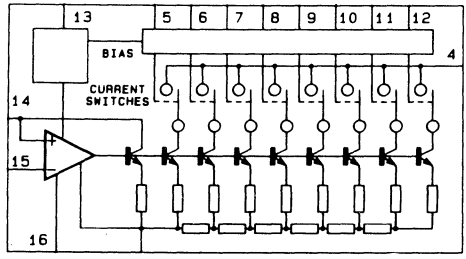
DC MOTORS



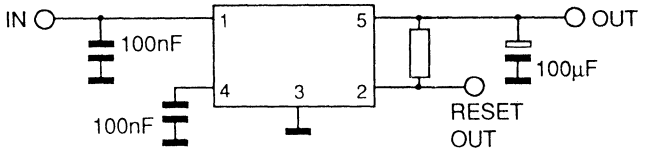
DISPLAYS



SPECIAL FUNCTIONS



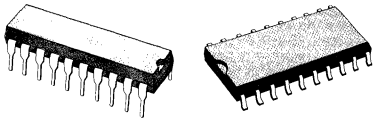
VOLTAGE REGULATORS



DATASHEETS

12-BIT HIGH SPEED D/A CONVERTERS

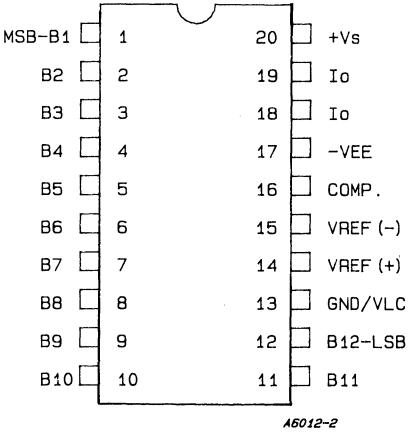
- ALL GRADES 12-BIT MONOTONIC OVER TEMPERATURE
- DIFFERENTAL NONLINEARITY TO ±0.012% (13 BITS) MAX OVER TEMPERATURE (A GRADES)
- 250ns TYPICAL SETTLING TIME
- FULL SCALE CURRENT 4mA
- HIGH SPEED MULTIPLYING CAPABILITY
- TTL/CMOS/ECL/HTL COMPATIBLE
- HIGH OUTPUT COMPLIANCE: −5V TO +10V
- COMPLEMENTARY CURRENT OUTPUTS
- LOW POWER CONSUMPTION: 230mW



DIP-20 Plastic (0.4)

SO-20L

PIN CONNECTION



DESCRIPTION

The AM6012 is an industry standard monolithic 12-bit digital-to analog converter. Complementary current output and high speed multiplying capability make the AM6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures. The AM6012 is packaged in a 20-pin plastic DIP and is SO-20L for surface mounting. Although tested and specified at ±15V, the AM6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of +5 volts, −12 volts to ±18 volts. The AM6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as high as 0.012% (13 bits) for the A grades and 0.025% (12 bits) for the standard grades over the entire temperature range.

Guaranteed monotonicity and low cost make the AM6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

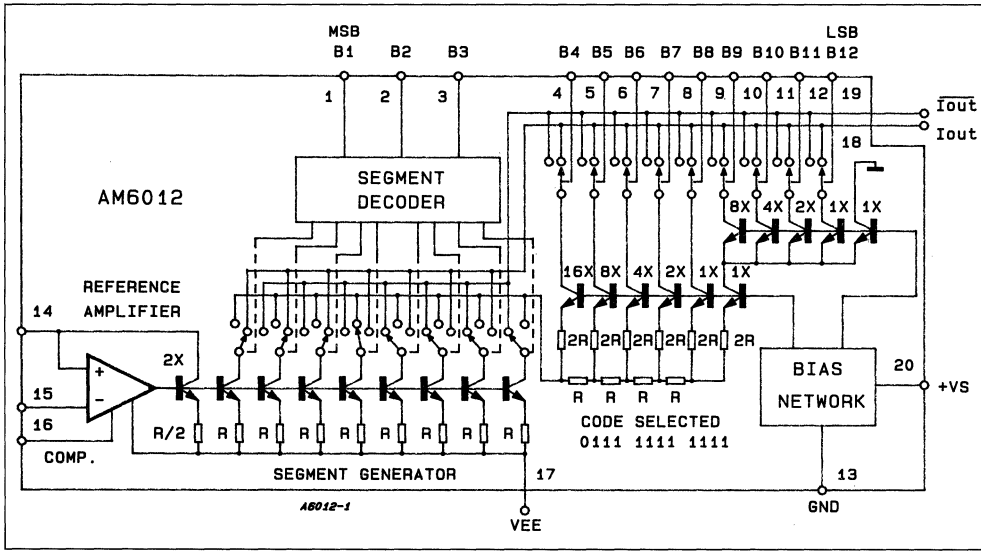
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0 to 70	°C
Storage Temperature	−65 to + 125	°C
Power Supply Voltage	±18	V
Logic Inputs	−5 to +18	V
Voltage at Current Outputs Pins	−8 to +12	V
Reference Inputs	$+V_S$ to $-V_{EE}$ ±18V max Differential	V
Reference Input Current	1.25	mA

CONNECTION DIAGRAM AND ORDERING INFORMATION

Type	Differential linearity (%)	Temperature Range (°C)	Package
AM6012PC	0.025	0 to 70	DIP.20
AM6012APC	0.012		
AM6012 D	0.025	0 to 70	SO.20L
AM6012 AD	0.012		

BLOCK DIAGRAM



THERMAL DATA

$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_S = +15V$, $V_{EE} = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	—	—	±.012	—	—	±.025	%FS
			13	—	—	12	—	—	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	—	—	±.05	—	—	±0.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Temp.Co.		—	±5	±20	—	±10	±40	ppm°C
			—	±.0005	±.002		±.001	±.004	%FS°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohme typ.	−5	—	+10	−5	—	+10	V
I_{FSS}	Full Scale Symmetry	I_{FS}-I_{FS}	—	±0.2	±1.0	—	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		—	—	0.10	—	—	0.10	μA
I_S	Setting Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	—	250	500	—	250	500	nSec
t_{PLH} t_{PHL}	Propagation Delay - all bits	50% to 50%	—	25	50	—	25	50	nSec
C_{OUT}	Output Capacitance		—	20	—	—	20	—	pF
V_{IL}	Logic Input Levels — Logic "O"		—	—	0.8	—	—	0.8	V
V_{IH}	Logic Input Levels — Logic "1"		2.0	—	—	2.0	—	—	V
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	—	—	40	—	—	40	μA
V_{IS}	Logic Input Swing	$V_{EE} = -15V$	−5	—	+18	−5	—	+18	V
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA

ELECTRICAL CHARACTERISTICS (Continued)

Param.	Description	Test Conditions	AM6012A			AM6012			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
di/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ $CC = OpF$	4.0	8.0	—	4.0	8.0	—	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$V_S = (+13.5V$ to $+16.5V)$ $V_{EE} = -15V$	—	±.00005	±.001	—	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		$V_{EE} = -13.5V$ to $-16.5V$ $V_S = +15V$	—	±.00025	±.001	—	±.00025	±.001	
V_S	Power Supply Range	$V_{OUT} = 0V$	4.5	—	18	4.5	—	18	V
V_{EE}			−18	—	−10.8	−18	—	−10.8	
I+	Power Supply Current	$V_S = +5V$, $V_{EE} = -15V$	—	5.7	8.5	—	5.7	8.5	mA
I−			—	−13.7	−18.0	−	−13.7	−18.0	
I+		$V_S = +15V$, $V_{EE} = -15V$		5.7	8.5	—	5.7	8.5	
I−			—	−13.7	−18.0	−	−13.7	−18.0	
P_D	Power Dissipation	$V_S = +5V$, $V_{EE} = -15V$	—	234	312	—	234	312	mW
		$V_S = +15V$, $V_{EE} = -15V$	—	291	397	—	291	397	

Fig. 1 - Relative Accuracy Error

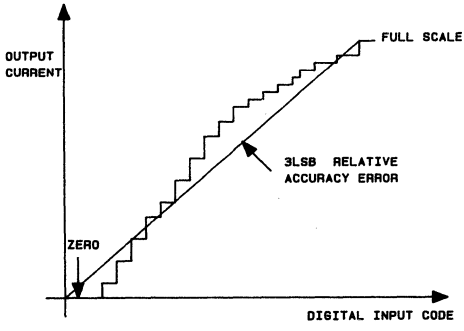


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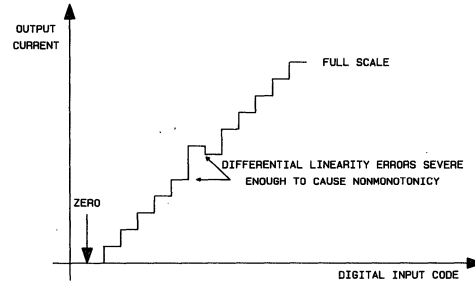
Fig. 2 - Example of Nonmonotonic Behavior



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APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The segmented design of the AM6012, shown in the block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AM6012.

In a conventional R-2R type DAC, when the input code is increemented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AM6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time. For example, consider the MSB carry in an AM6012. In the initial state of 011111111111 as shown in the block diagram, the switches in the segment generator are set in such a way that currents I_O, I_I and I_2 are steered directly into the noninverting output I_{OUT}. In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT}. With the 9LSBs set to "I", all of the I_3 current is directed to I_{OUT} except for the 1/512 that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0, I_1, I_2 and I_3. None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of 511/512 in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlinearity at this transition than in a comparable R-2R DAC.

RELATIVE ACCURACY VS. DIFFERENTIAL NONLINEARITY

We defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 1 has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a ILSB change in digital input code.

For example, for a 4mA full scale output, a change of ILSB in digital input code should result in a 0.98μA change in the analog output current (ILSB = 4mA x 1/4096 = 0.98μA). If in actual use, however, a ILSB change in the input code results ina change of only 0.24μA (1/4LSB) in output current, the differential linearity error would be 0.74μA or 3/4LSB.

The AM6012 has very good differential linearity in spite of the porr relative accuracy. Conversely, the DAC of Figure 1 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be nonmonotonic at one or more of the major carries. In most case the worst differential linearity error will occur at the MSB transition point.

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. Differential linearity is verified on all AM6012s with 100% final testing. In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit onverters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AM6012 is especially well suited for these applications since it has inherently low differential linearity error.

APPLICATION INFORMATION (Continued)

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + I_O = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increase I_O as in a negative or inverter logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin one.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures fro guidance. For example, operation at −9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and mononicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is flight, typically ±10ppm/°C with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ms. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 2\mu A$, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be octained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATION INFORMATION (Continued)

REFERENCE AMPLIFIER SETUP

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{RF} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 3).
Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V-$ plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The positive common-mode range is V+ less 1.23V.
When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.
For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

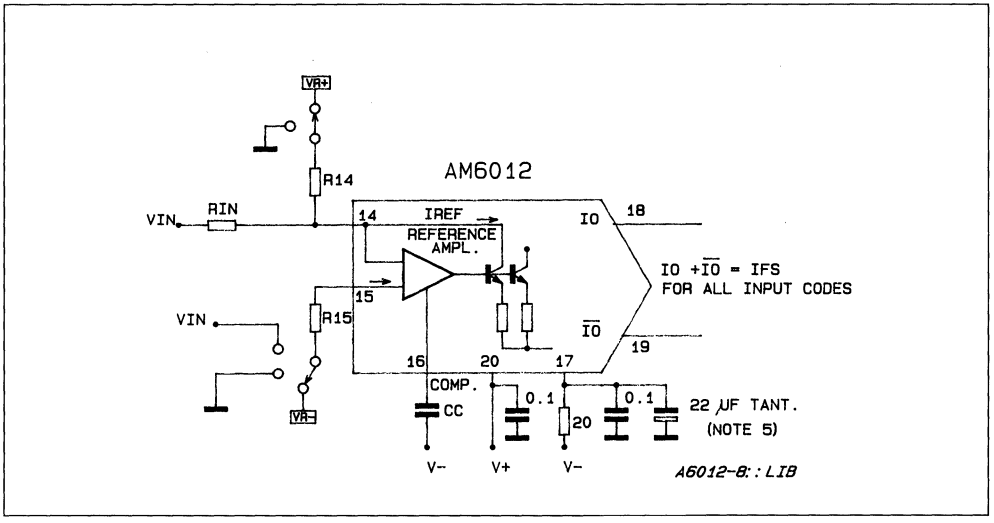
REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5 OkΩ; minimum values of C_C are 5, 12 and 25 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin (See Figure 4 and 5).
For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven be a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from $I_{REF} = 0$ to I_{REF} = 1mA in 250ns.
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and $C_C = 0$. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic inputs may swing between −5 and +10V.
This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1mA is recommended. For interfacing other logic families, see block titled "Interfacing with Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 1.1mA typical, external circuitry should be designed to accommodate this current (Figure 6).

Fig. 3 - Reference amplifier biasing



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01µF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01µF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor a function of the impedance seen at the $+V_{REF}$ input and must be at least $5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V - with 20Ω and bypass with 22µF tantulum capacitor.
6. Reference current and reference resistor - there is a 1 to 4 schale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

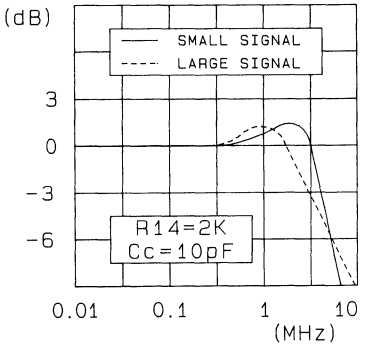
$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4mA} = 10k\Omega \quad R_{14} = R_{15}$$

Fig. 4 - Minimum size compensation capacitor (I_{FS} = 4mA, I_{REF} = 1.0mA)

$R_{14(EQ)}$(KΩ)	C_C(pF)
10	50
5	25
2	10
1	5
5	0

Note: A 0.01 μF capacitor is recommended for fixed reference operation.

Fig. 5 - Reference Amplifier Frequency response



A6012-11: : DI

Fig. 6 - Interfacing Circuits

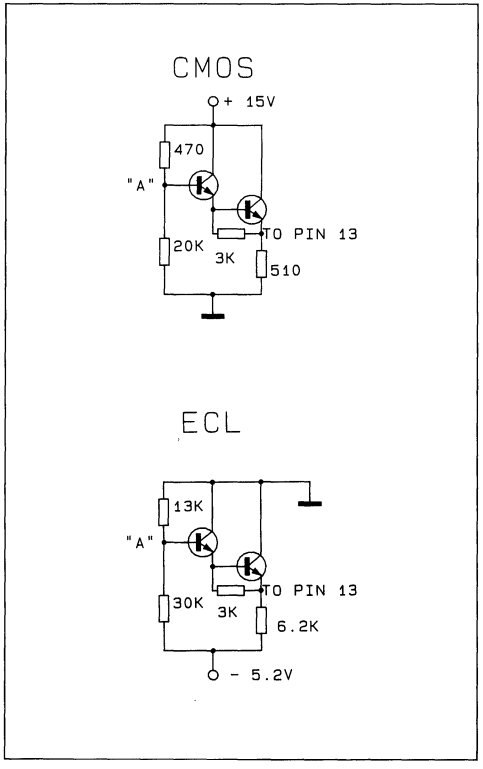


Fig. 7 - Accomodating Bipolar Reference

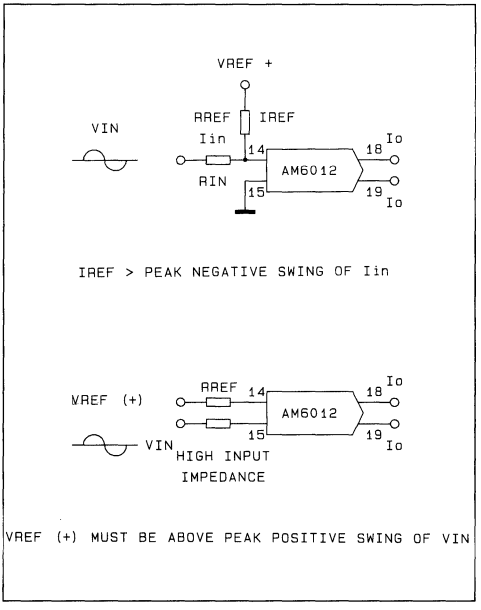
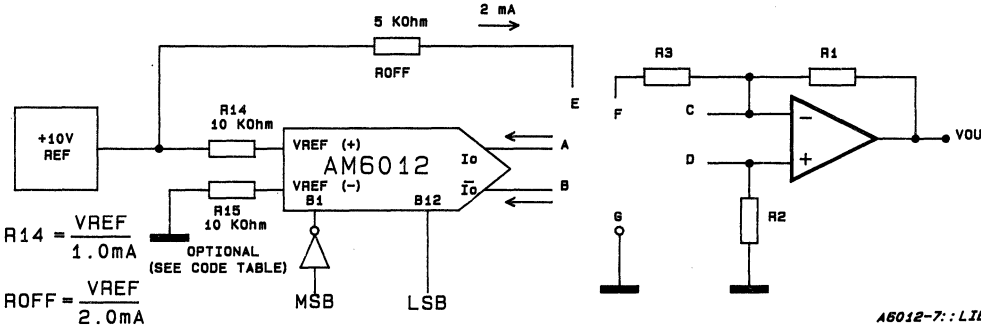


Fig. 8 - AM6012 Logic Inputs



Code Format		Connec.	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0	$\overline{I_0}$	V_{OUT}
Unipolar	Straight bynary one polarity with true input code, true zero output.	a-c b-g $R_1=R2=2.5K$	Positive full scale Positive full scale-LSB Zero scale	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0	1 0 0	3.999 3.998 .000	.000 .001 3.999	9.9978 9.9951 .0000
	Complementary binary one polarity with complementary input code, true zero output.	a-g b-c R1=R2=2.5K	Positive full scale Positive full scale-LSB Zero scale	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 0 1	0 1 1	.000 .001 3.999	3.999 3.998 .000	9.9976 9.9951 .0000
Symmetrical Offset	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c b-d f-0 R1=R3=2.5K R2=1.25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	1 1 1 0 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	3.999 3.998 2.000 1.999 .001 .000	.000 .001 1.999 2.000 3.998 3.999	9.9976 9.9927 .0024 -.0024 -9.9927 -9.9976
	1's complement offset half scale symmetrical about zero, no true zero output MSB complemented (need inverter at B1).	a-c b-d f-g R1=R3=2.5K R2=1.25K	Positive full scale Positive full scale-LSB (+) Zero scale (-) Zero scale Negative full scale-LSB Negative full scale	0 0 0 1 1 1	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 1 0 1 0 0	1 0 0 1 1 0	3.999 3.998 2.000 1.999 .001 .000	.000 .001 1.999 2.000 3.998 3.999	9.9976 9.9927 .0024 -.0024 -9.9927 -9.9976
Offset with True Zero	Offset binary, offset half scale, true zero output.	e-a-c b-g R1=R2=5K	Positive full scale Positive full scale-LSB +LSB Zero Scale -LSB Negative full scale+LSB Negative full scale	1 1 1 1 0 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 1 0 1 1 0	1 0 1 0 1 1 0	3.999 3.998 2.001 2.000 1.999 .001 .000	.000 .001 1.998 1.999 2.000 3.998 3.999	9.9951 9.9902 .0049 .000 -.0049 -9.9951 -10.000
	2's complement offset half scale true zero output MSB complemented (need inverter at B1)	e-a-c b-g R1=R2=5K	Positive full scale Positive full scale-LSB +1 LSB Zero scale -1 LSB Negative full scale+LSB Negative full scale	0 0 0 0 1 1 1	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 0 0 1 0 0	1 1 1 0 1 1 0	1 0 1 0 1 1 0	3.999 3.998 2.001 2.000 1.999 .001 .000	.006 .001 1.998 1.999 2.000 3.998 3.999	9.9951 9.9902 .0049 .000 -0.049 -9.9951 -10.000

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

Fig. 9 - Basic Negative Reference Operation

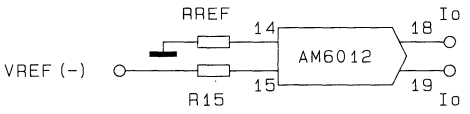


Fig. 10 - Recommended Full-scale Adjustment Circuit

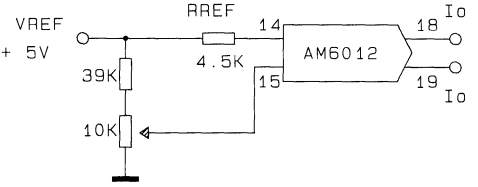


Fig. 11 - CRT Display Driver

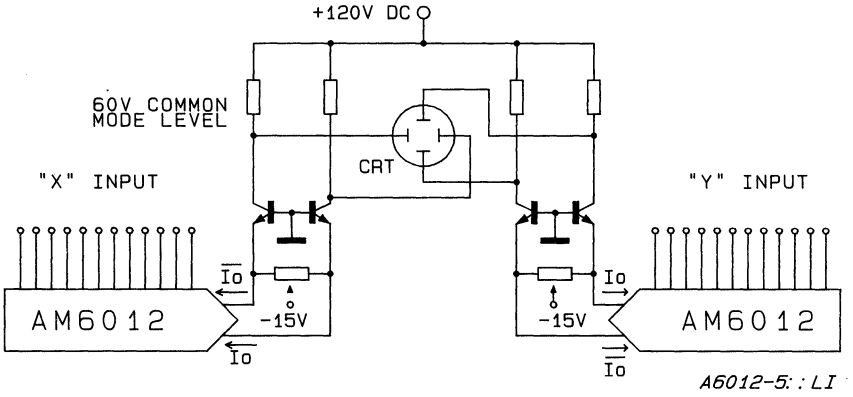


Fig. 12 - 12-BIT High-Speed A/D Converter

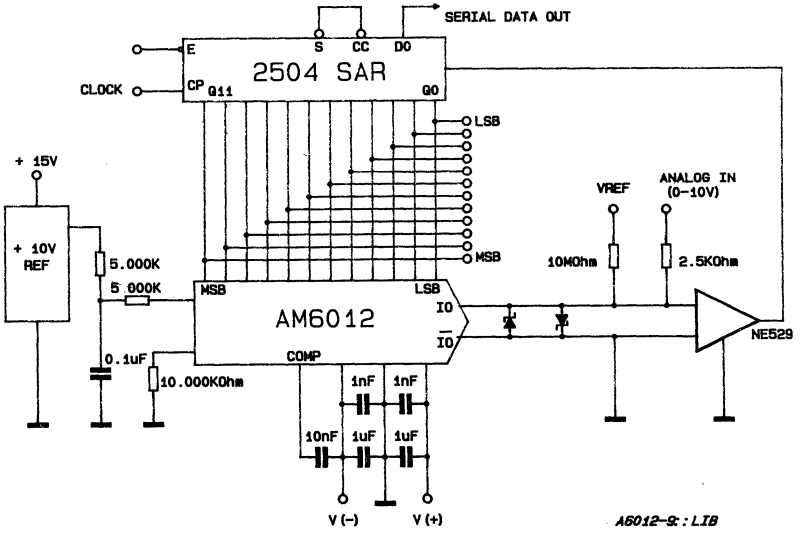


Fig. 13 - Interface with 8-bit Microprocessor Bus

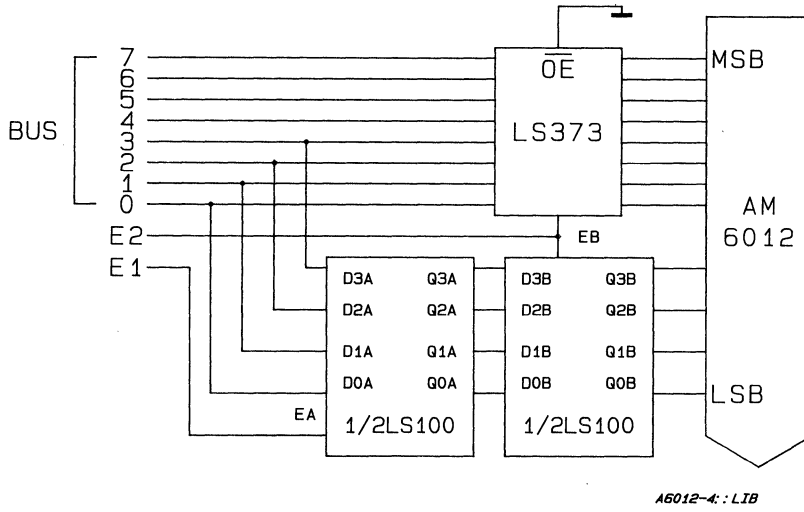
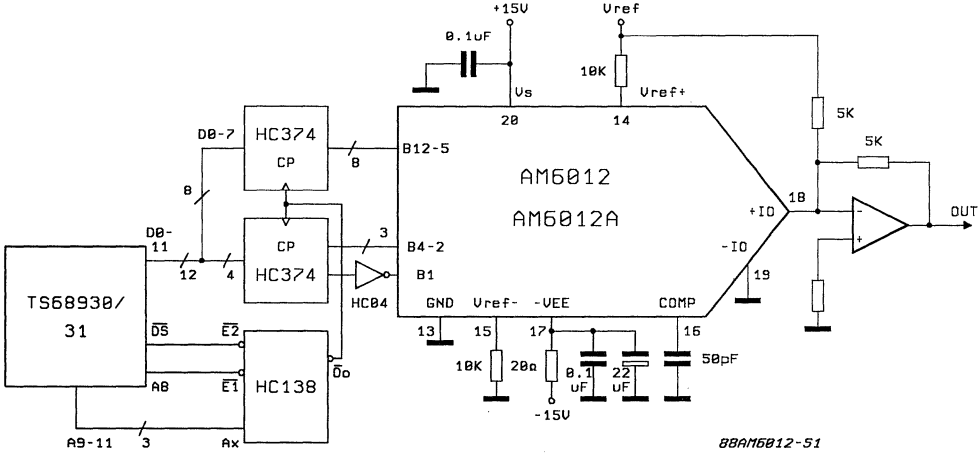
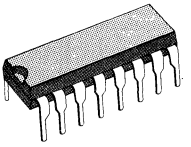


Fig. 14 - Interface with digital signal processor TS68930/31

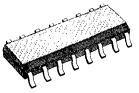


8-BIT D/A CONVERTERS

- RELATIVE ACCURACY: ±0.19% ERROR MAXIMUM (DAC0808)
- FULL SCALE CURRENT MATCH: ±1 LSB TYP
- 7 AND 6-BIT ACCURACY AVAILABLE (DAC0807, DAC0806)
- FAST SETTING TIME: 150 ns TYP
- NONINVERTING DIGITAL INPUTS ARE TTL AND CMOS COMPATIBLE
- HIGH SPEED MULTIPLYING INPUT SLEW RATE: 8 mA/μs
- POWER SUPPLY VOLTAGE RANGE: ±4.5V to ±18V
- LOW POWER CONSUMPTION: 33 mW @ ±5V

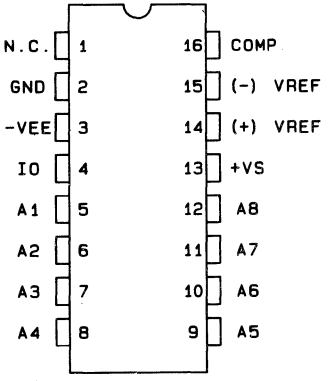


DIP-16 Plastic (0.25) and Ceramic



SO-16J

PIN CONNECTION



DAC0808-13

DESCRIPTION

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than 0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, or CMOS logic levels, and is a direct replacement for the MC1508/MC1408.

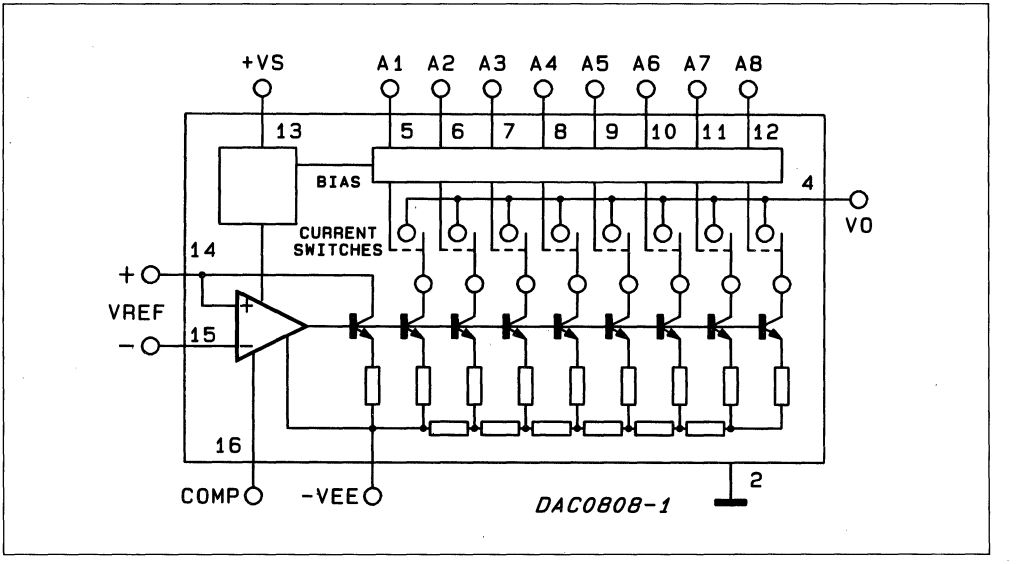
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
V_S	+18 V
V_{EE}	−18 V
Digital Input Voltage V5 − V12	−10 V to +18 V
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC} , V_{EE}
Operating Temperature Range	
DAC0808L	$-55°C \leq T_A \leq +125$ °C
DAC0808LC/D1	$0 \leq T_A \leq +75$ °C
Storage Temperature Range	−65°C to +150 °C

ORDERING INFORMATION

Accuracy	Temperature range	Plastic DIP-16	Ceramic DIP-16	SO-16
8 bit	0 to 75°C	DAC0808LCN	DAC0808LCJ	DAC0808D
7 bit	0 to 75°C	DAC0807LCN	DAC0807LCJ	DAC0807D
6 bit	0 to 75°C	DAC0806LCN	DAC0806LCJ	DAC0806D
8 bit	−55 to 125°C	—	DAC0808LJ	—

BLOCK DIAGRAM



THERMAL DATA

		Ceramic DIP-16	SO-16	Plastic DIP-16
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	150°C/W	120°C/W	100°C/W

ELECTRICAL CHARACTERISTICS

(V_S = 5V, V_{EE} = −15V, $V_{REF}/R14$ = 2 mA, $T_A = T_{MIN}$ to T_{MAX} and all digital inputs at high logic level unless otherwise noted.)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 10)*				%
	DAC0808L				±0.19	%
	DAC0807LC/D1 (Note 1)				±0.39	%
	DAC0806LC/D1 (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2) *(Figure 11)*		150		ns
t_{PLH} t_{PHL}	Propagation Delay Time	T_A = 25°C *(Figure 11)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB V_{IH} V_{IL}	Digital Input Logic Levels	*(Figure 9)*				
	High Level, Logic "1"		2			V_{DC}
	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 9)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 9)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V. R14 = 1000Ω				
		(Figure 9)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 9)*		0	4	μA
	Output Voltage Compliance	$E_r \leq 0.19\%$, T_A = 25°C				
	V_{EE} = −5V				−0.55, +0.4	V
	V_{EE} Below −10V				−5.0 , +0.4	V
SRI_{REF}	Reference Current Siew Rate	*(Figure 14)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \leq V_{EE} \leq -16.5V$		0.05	2.7	μA/V
Power Supply Current (All Bits Low)		*(Figure 9)*				
I_S				2.3	22	mA
I_{EE}				−4.3	−13	
Power Supply Voltage Range		T_A = 25°C *(Figure 9)*				
V_S			4.5	5.0	5.5	V
V_{EE}			−4.5	−15	−16.5	
	Power Dissipation					
	All Bits Low	V_S = 5V. V_{EE} = −5V		33	170	mW
		V_S = 5V. V_{EE} = −15V		106	305	mW
	All Bits High	V_S = 15V. V_{EE} = −5V		90		mW
		V_S = 15V. V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

Fig. 1 - Supply Current vs Temperature

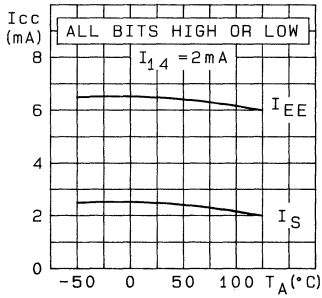


Fig. 2 - Supply Current vs Supply Voltage (V_{EE})

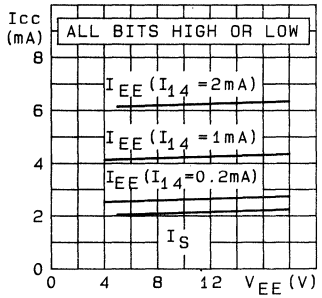


Fig. 3 - Supply Current vs Supply Voltage (V_S)

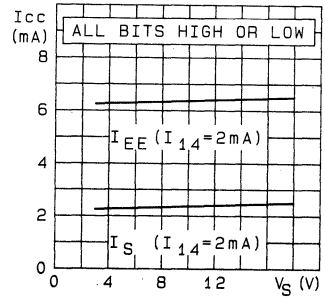


Fig. 4 - Logic Input Current vs Input Voltage

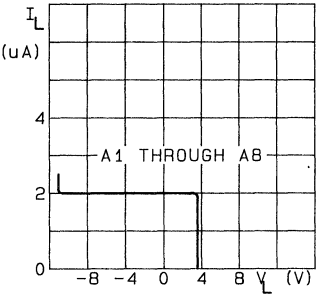


Fig. 5 - Bit Transfer Characteristics

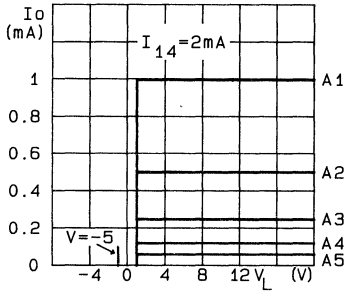


Fig. 6 - Output Voltage Compliance

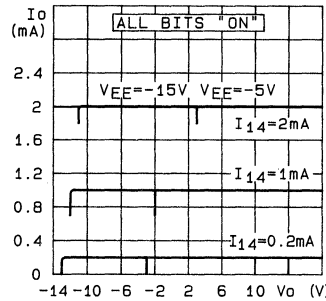


Fig. 7 - Output Voltage Compliance vs Temperature

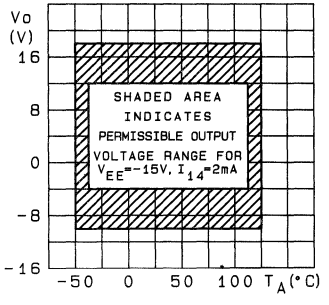
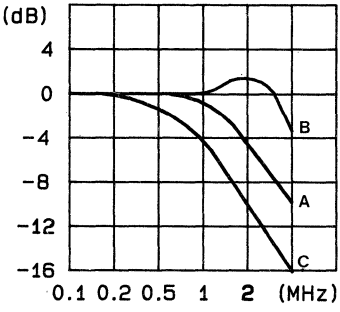


Fig. 8 - Frequency response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

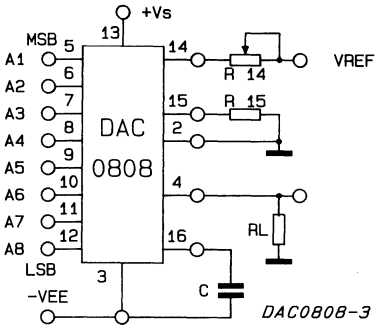
Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp. R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

Test Circuits

FIGURE 9. Notation Definitions



The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 10. Relative Accuracy

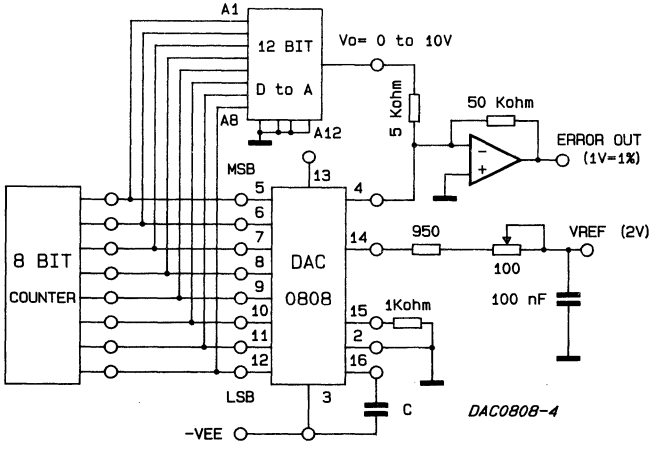
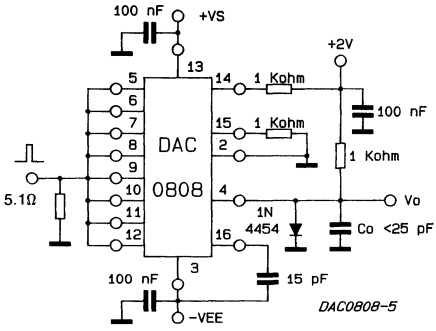


FIGURE 11. Transient Response and Settling Time



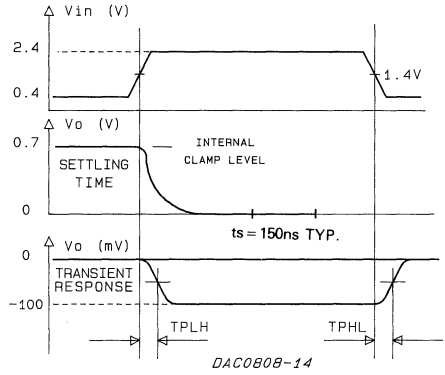


FIGURE 12. Positive V_{REF}

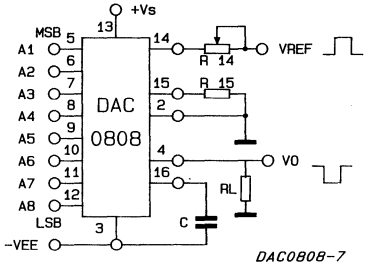


FIGURE 13. Negative V_{REF}

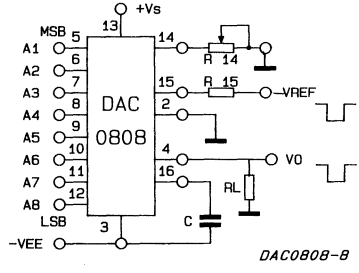
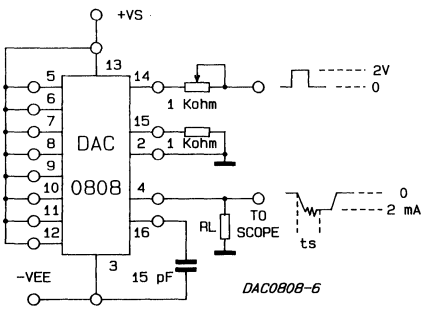


FIGURE 14. Reference Current Slew Rate Measurement



APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The DAC0808 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Nota that there is always a remainder current which is equal to the last significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 12*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15,37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 13*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive by pass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to 0.5V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case setting time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mis-match in the NPN current source pair. The accuracy test circuit is shown in *Figure 10*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA.

Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.019% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB for 8-bit accuracy and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These timers apply when $R_L \leqslant 500$ ohms and $C_0 \leqslant 25$ pF.

The test circuit of Figure 11 requires a smaller voltage swing for the current switches due to internal voltage clamping in the DAC0808 A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 200 ns.
Thus, it is voltage swing and not the output RC time constant that determines setting time for most applications.
Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time.
Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mondatory.

PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTEPUATOR

When used in the multiplying mode can be applied as a digital attenuator. See Figure 15. One advantage of this technique is that if $R_S = 50$ ohms, no compensation capacitor is needed. The small and large signal band are now identical and are shown in Figure 8C.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ± 1.0 mA variation in relation to I_{14}. I_{14} can never be negative.
The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes accoupling necessary.

CURRENT TO VOLTAGE CONVERSION

Voltage output of a larger magnitude are obtainable with the circuit of fig. 16 which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the DAC0808 ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and setting time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases over compensation may be desirable.
Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input. The LM301 can be used in a feedforwerd mode resulting in a full scale setting time on the order of 2.0 μs.

COMBINED OUTPUT AMPLIFIER AND VOLTAGE REFERENCE

For many of its applications the DAC0808 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular LM723 voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA output current. See Figure 17. The reference voltage is developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its amplifier as a classic current-to-voltage converter with the non-inverting input grounded.
Since ± 15V and $+5.0$V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.
Full scale output may be increasing R_O and raising the $+15$V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the LM723 C_O may be decreased to maintain the same R_O-C_O product if maximum speed is desired.

PROGRAMMABLE POWER SUPPLY

The circuit of figure 17 can be used as a digitally programmed power supply by the addition of thumb-wheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to $+25.5$ volts in 0.1 $-$volt increments, ± 10 mV.

PANEL METER READOUT

The DAC0808 can be used to read out the status of BCD or binary registers or counters a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 20 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref} (see fig. 18).

CHARACTER GENERATOR

In a character generation system fig. 19 one DAC0808 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

TWO-DIGIT BCD CONVERSION

Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter (fig. 21). If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an DAC0806 may be used for the least significant word.

FIGURE 16.

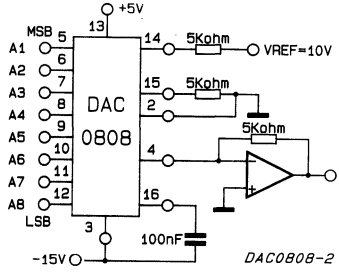
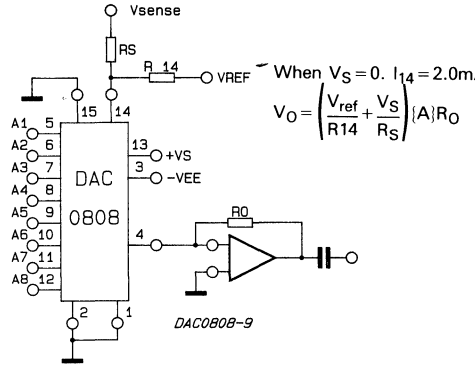


FIGURE 15. Programmable Gain Amplifier or Digital Attenuator Circuit



$$V_O = 10V\left(\frac{A1}{2} + \frac{A2}{4} + \cdots \frac{A8}{256}\right)$$

FIGURE 17. Combined output amplifier and voltage reference circuit

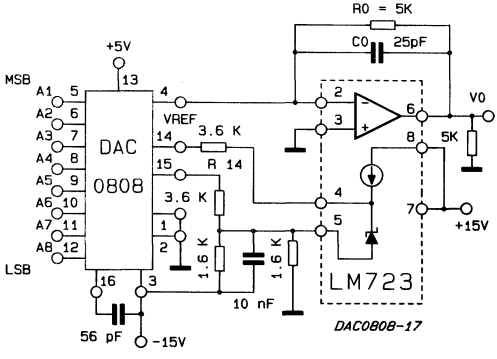
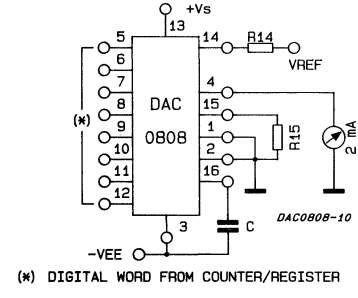
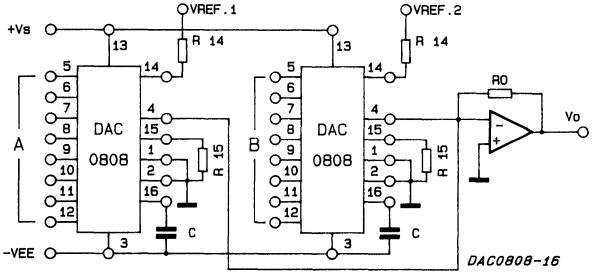


FIGURE 18. Panel meter readout circuit



(*) DIGITAL WORD FROM COUNTER/REGISTER

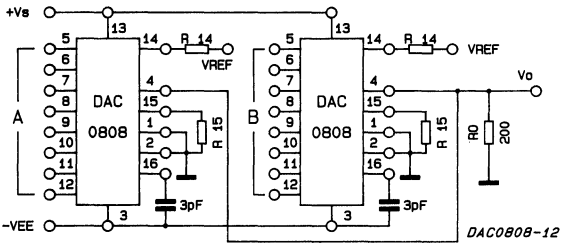
FIGURE 19. Digital summing and character generation



$$V_O = (I_{O1} + I_{O2})\, R_O$$

$$V_O = \left[\frac{V_{ref1}}{R14_1}\{A\} + \frac{V_{ref2}}{R14_2}\{B\}\right] R_O$$

FIGURE 20. Analog product of two digital words (High Speed Operation)



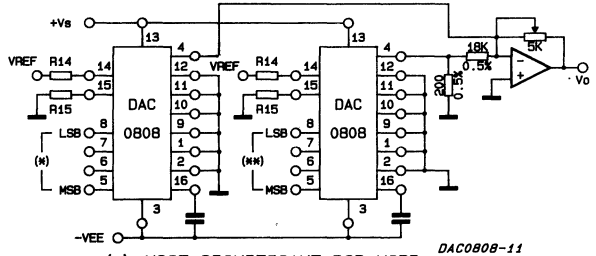
$$V_O = -I_{O1}\, R_O = \frac{V_{ref}}{R14_1}\{A\}\, R_O$$

$$I_{O2} = \frac{\{B\}\,|V_{O1}|}{R14_2} = \frac{\{B\}}{R14_2}\left[R_O\left(\frac{V_{ref}}{R14_1}\right)\{A\}\right]$$

Since $R_O = R14_2$ and $K = \dfrac{V_{ref}}{R14_1}$

$$\boxed{I_{O2} = K\{A\}\{B\}}$$ K can be an analog variable

FIGURE 21. Two-digit BCD conversion



(*) MOST SIGNIFICANT BCD WORD
(**) LEAST SIGNIFICANT BCD WORD

SGS-THOMSON MICROELECTRONICS

ESM1600B

QUAD COMPARATOR INTERFACE CIRCUIT

- MINIMUM HYSTERESIS VOLTAGE AT EACH INPUT : 0.3 V
- OUTPUT CURRENT : 15 mA
- LARGE SUPPLY VOLTAGE RANGE : + 10 V to + 35 V
- INTERNAL THERMAL PROTECTION
- INPUT AND OUTPUT CLAMPING PROTECTION DIODES.

DESCRIPTION

The ESM1600B is a quadruple comparator intented to provide an interface between signal processing and transmitting lines in very noisy industrial surroundings.

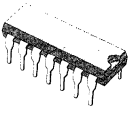
Output of each comparator, used as line driver, supplies a constant current (PNP output stage) and is specially well protected against powerful overvoltages. The open collector output circuit allows the connection of several comparators to a single transmitting line.

The ESM1600B can operate as receiver on a line transmitting noisy high-voltage signals. Hysteresis effect, internally implemented on inputs of each comparator provides an excellent noise immunity. In addition, each input is also protected against overvoltages.

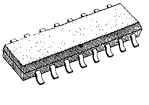
The ESM1600B can operate in a wide supply voltage range (standard operational amplifier ± 15 V supply or single + 12 V or + 24 V supplies used in industrial electronic sets).

Moreover, internal thermal protection circuitry cuts out the output current of the four comparators when power dissipation becomes excessive.

DIP-14/2
(Plastic)



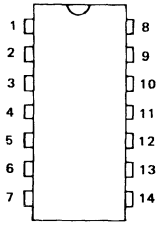
SO16J



ORDER CODES : ESM1600B (DIP-14)
ESM1600BFP (SO16J)

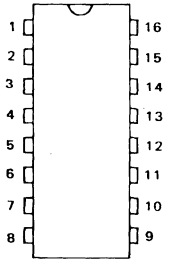
PIN CONNECTIONS (top view)

DIP-14



1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - Output 4
12 - Non-inverting input 4
13 - Inverting input 4
14 - V_{CC}

SO16J

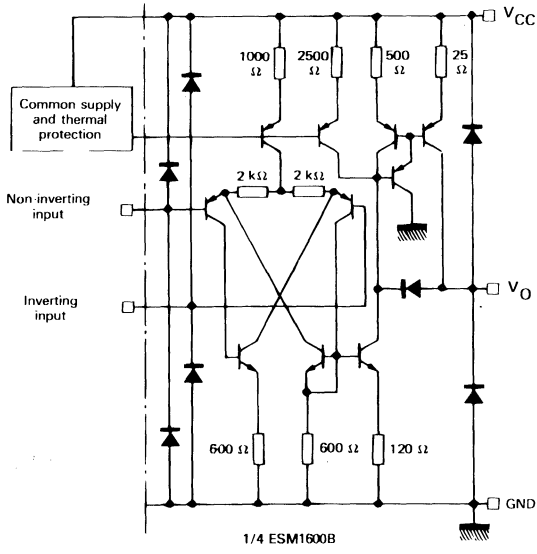


1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - N.C.
9 - N.C.
10 - Output 3
11 - Inverting input 3
12 - Non-inverting input 3
13 - Output 4
14 - Non-inverting input 4
15 - Inverting input 4
16 - V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	45	V
V_{ID}	Differential Input Voltage	45	V
V_I	Input Voltage	– 0.7 to + 45	V
$I_{O\ (max)}$	Output Current	Internally Limited	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{op}	Operating Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 40 to + 150	°C

SCHEMATIC DIAGRAM

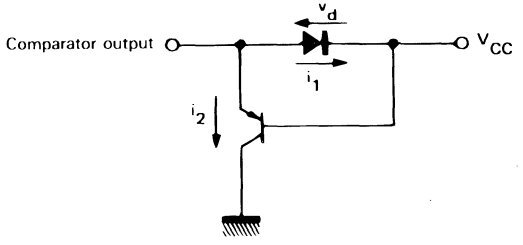


ELECTRICAL CHARACTERISTICS V_{CC} = + 35 V, - 25 °C ≤ T_{amb} ≤ + 85 °C (unless otherwise specified)

Symbol	Parameter	Value Min.	Value Typ.	Value Max.	Unit	Fig.
V_I^+	Input Voltage Range - Note 1				V	–
V_I^-	Non-inverting Input	0	–	33		
	Inverting Input	2	–	33		
V_C	Input Control Voltage (2 V < V_{CM} < 33 V) - Note 2	150	–	500	mV	1
I_{IB}	Input Bias Current - Note 3	–	1	5	µA	–
I_{SC}	Short-circuit Output Current				mA	2
	V_{CC} = + 10 to + 35 V	6	–	25		
V_{CC}–V_O	Output Saturation Voltage (high level) - (I_O = – 10 mA)	–	1	1.5	V	3
I_{OL}	Output Off-state Current (V_I^+ = 2 V, V_I^- = 33 V)	–	1	5	µA	4
I_{OH}						
I_{CC}	Supply Current					
	R_L = ∞ for the 4 Comparators	–	3	5	mA	5
	R_L Common for the 4 Comparators	–	9	12		
S_{VO}	Output Slew-rate (R_L = 3 kΩ, T_{amb} = + 25 °C)	1	–	–	V/µs	–
V_F	Input Protective Diode Forward Voltage (I = 20 mA, T_{amb} = + 25 °C)	–	–	1.5	V	–
–	Energy of Pulses against which Circuit Output is Protected. (T_{amb} = + 25 °C) - Note 4	–	–	20	mJ	–
–	Pulsed Current Applied to Protective Output Diodes (T_{amb} = + 25 °C) - Note 5	–	0.4	–	A	6

Notes :

1. When negative input is biased between 0 and 2 volts output is always low.
2. Comparator hysteresis voltage on positive input on the one hand and negative input on the other hand equals sum of input control voltages V_{C1} + V_{C2} or V_{C3} + V_{C4}.
3. Input current flows out of the circuit owing to PNP input stage. This current is constant and independent of output level. So no load change is transmitted to inputs.
4. By definition, a circuit is immunized against powerful signals when no durable characteristic change occurs after the application of these signals and when the circuit has not been destroyed.
   In industrial surroundings, parasitic signals contain usually high voltage (over 200 V) AC harmonics having variable impedance of 500 Ω to 10 KΩ.
   The power dissipation of these signals is divided between clamping diodes and the V_{CC}. Simulation is used to determine the maximum energy level. The injected current value cannot in any case exceed 3 A.
5. Output protective diodes are tested individually by means of positive and negative discharge voltages of a capacitor. The negative discharge control occurs through a single diode. During positive discharge, due to the properties of integration, a grounded collector PNP transistor appears in parallel with the clamping diode connected to V_{CC}. A part of the current flows through this transistor, V_{CE} being greater than V_{CC}. If T is the total discharge duration, energy dissipated in the circuit is :



$$W = \int_0^T [\, i_1 \cdot vd + i_2 \,(VCC + vd)\,]\, dt$$

For a certain injected current, the lower the current I_2, that is to say the lower the PNP current gain the smaller the energy is dissipated in the circuit. Topology and technological processes have been chosen to shorten this current gain.

Figure 1: Input bias current

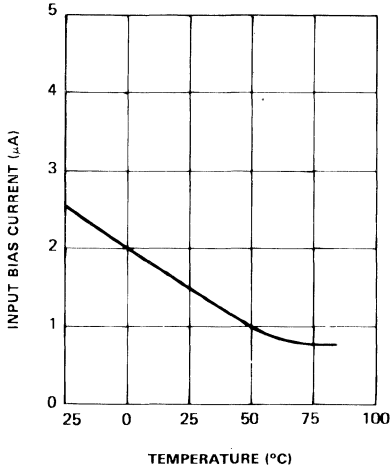


Figure 2: Output saturation voltage

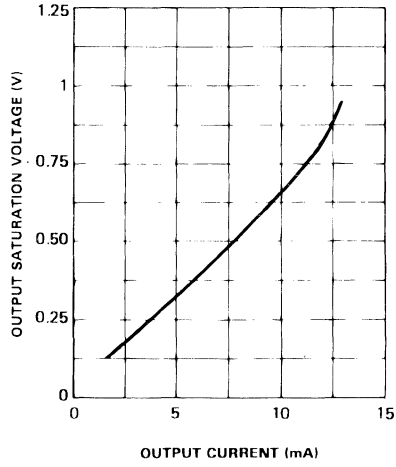


Figure 3: Output saturation voltage

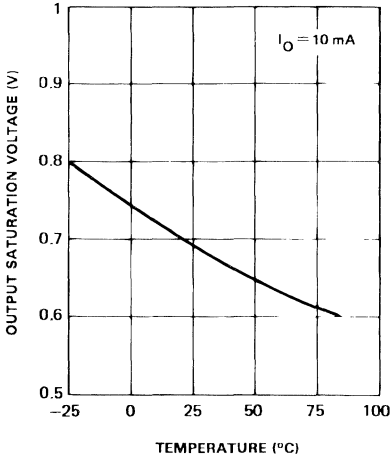
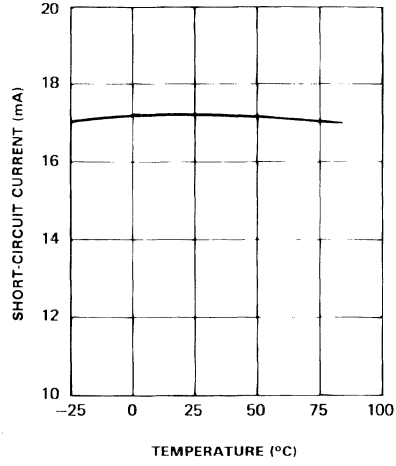


Figure 4: Short circuit corrent



TYPICAL APPLICATIONS

Figure 5 : Conversion of DTL, TTL, MOS Signals on a Transmitting Line.

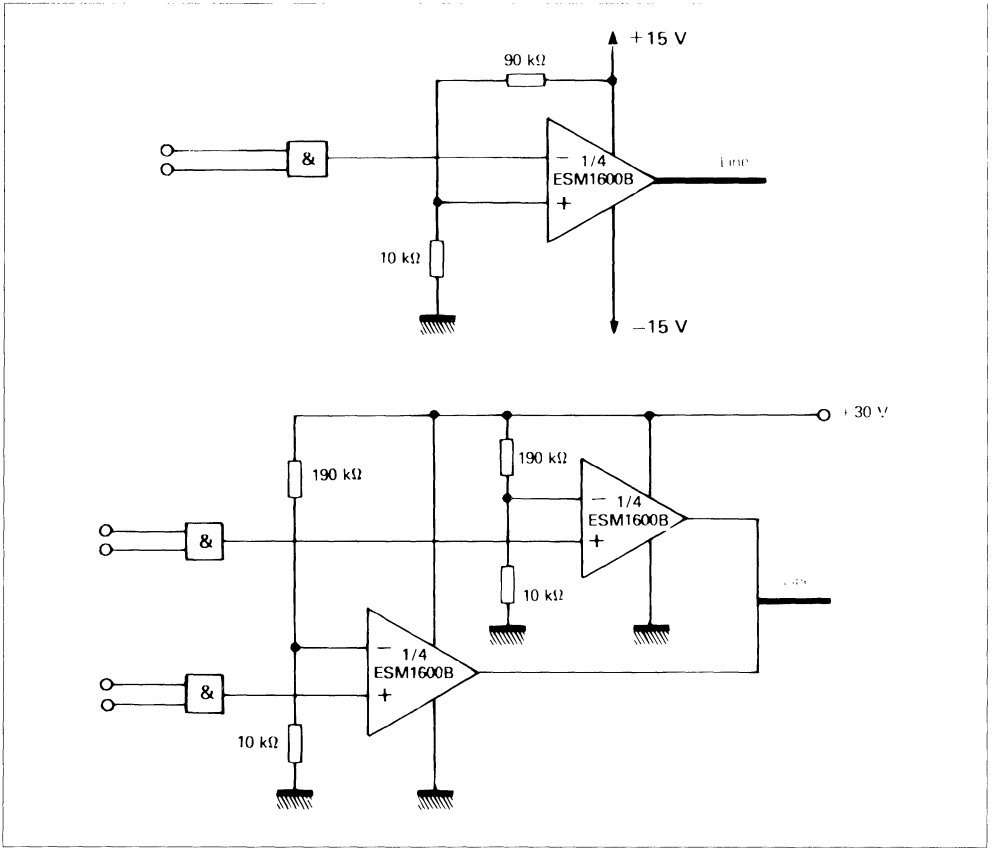
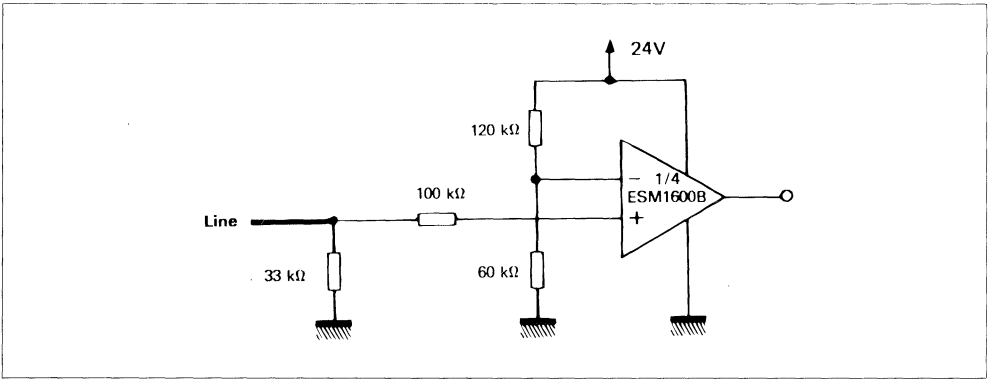


Figure 6 : Reception of Highly Noisy Signals.



TEST CIRCUIT

Figure 7.

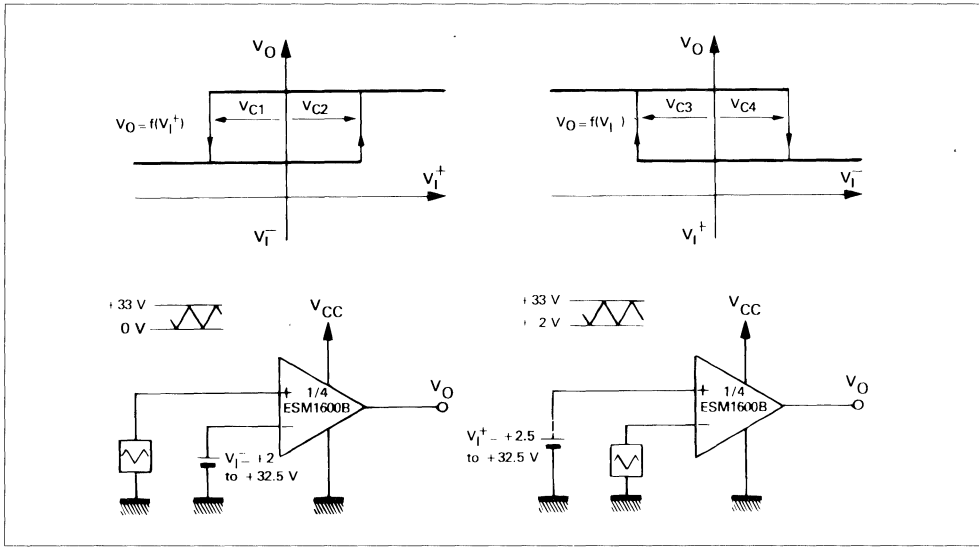


Figure 8.

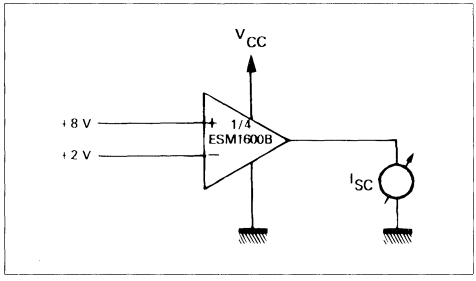


Figure 9.

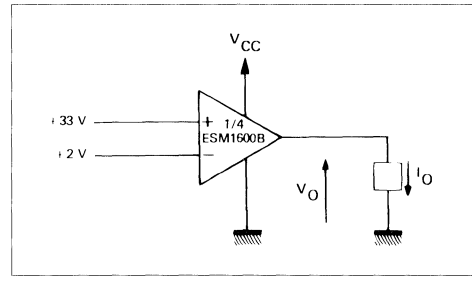


Figure 10.

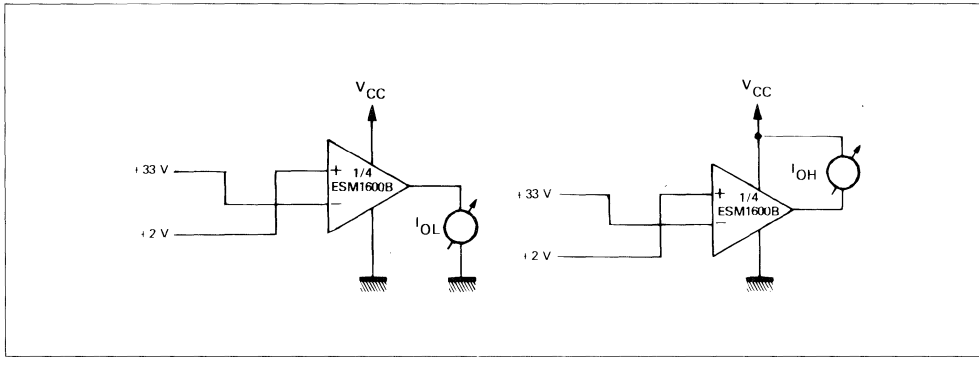


Figure 11.

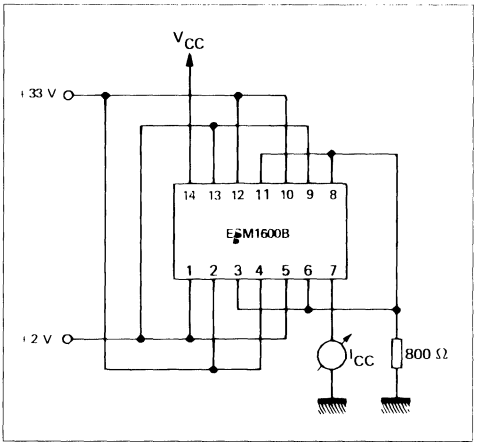


Figure 12.

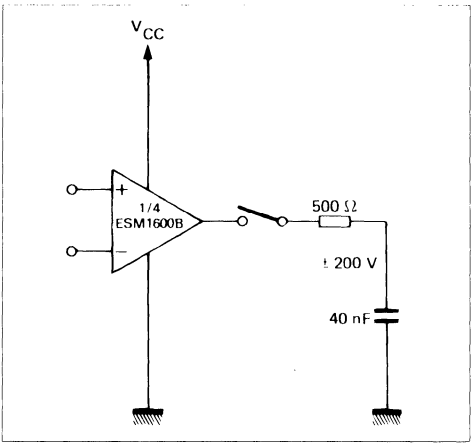
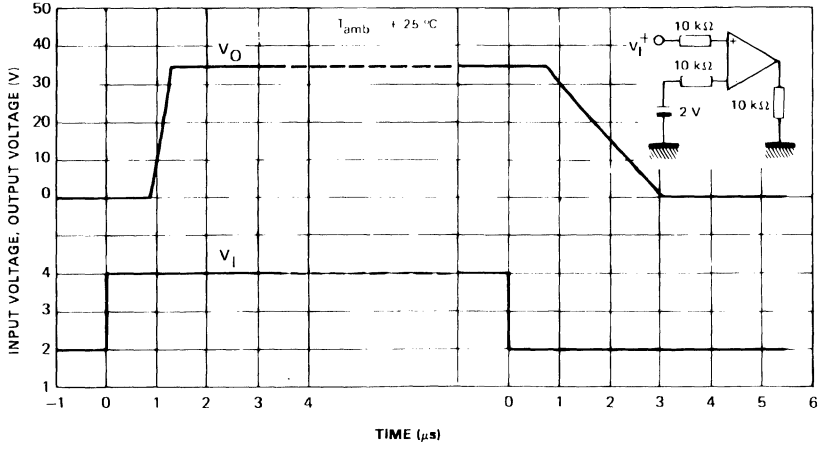


Figure 13 : Response Time.



ESM1602B

QUAD COMPARATOR INTERFACE CIRCUIT

- MINIMUM HYSTERESIS VOLTAGE AT EACH INPUT : 0.3 V
- OUTPUT CURRENT : 15 mA
- LARGE SUPPLY VOLTAGE RANGE : + 10 V TO + 35 V
- INTERNAL THERMAL PROTECTION
- INPUT AND OUTPUT CLAMPING PROTECTION DIODES

DESCRIPTION

The ESM1602B is a quadruple comparator intended to provide an interface between signal processing and transmitting lines in very noisy industrial surroundings.

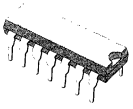
Output of each comparator, used as line driver, is well protected against powerful overvoltages. The output is a common emitter stage including complementary transistors. This arrangement ensures that no simultaneous conduction of high and low stages can occur in the presence of noise signals. Short-circuit currents toward V_{CC} and ground are limited to the same value.

The ESM1602B can operate as receiver on a line transmitting noisy high-voltage signals. It has the same input stage as ESM1600B. Hysteresis effect, internally implemented on inputs of each comparator provides an excellent noise immunity. In addition each input is also protected against overvoltages.

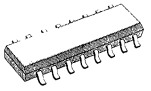
The ESM1602B can operate in a wide supply voltage range (standard operational amplifier ± 15 V supply or single + 12 V or + 24 V supplies used in industrial electronic sets).

Moreover, internal thermal protection circuitry cuts out the output current of the four comparators when power dissipation becomes excessive.

DIP-14/2
(Plastic)



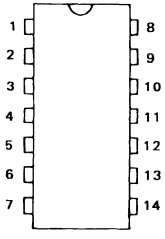
SO-16J



ORDER CODES : ESM1602B (DIP-14)
ESM1602BFP (SO-16J)

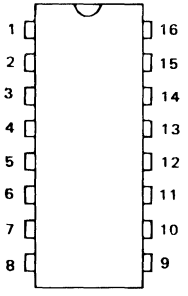
PIN CONNECTION (top view)

DIP-14



1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - Output 4
12 - Non-inverting input 4
13 - Inverting input 4
14 - V_{CC}

SO-16J

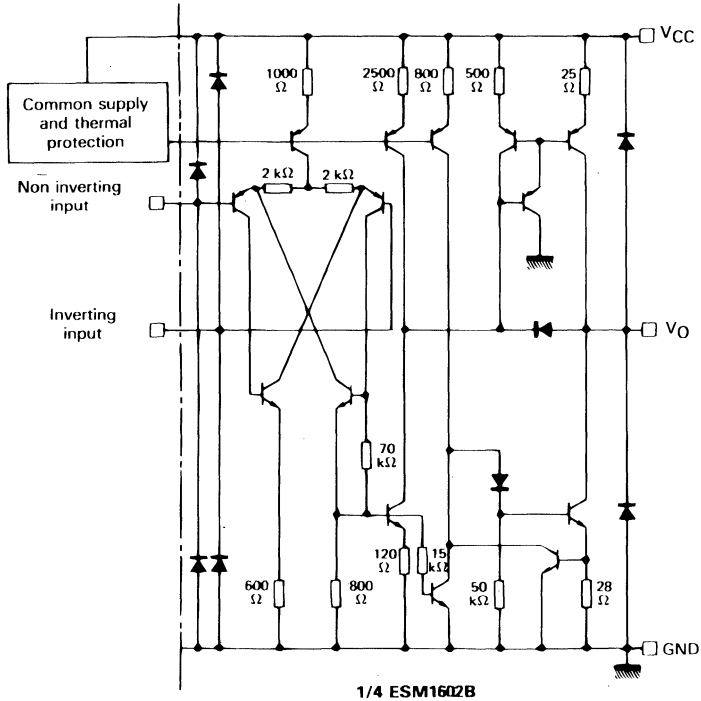


1 - Inverting input 1
2 - Non-inverting input 1
3 - Output 1
4 - Non-inverting input 2
5 - Inverting input 2
6 - Output 2
7 - GND
8 - N.C.
9 - N.C.
10 - Output 3
11 - Inverting input 3
12 - Non-inverting input 3
13 - Output 4
14 - Non inverting input 4
15 - inverting input 4
16 - V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	45	V
V_{ID}	Differential Input Voltage	45	V
V_I	Input Voltage	– 0.7 to + 45	V
$I_{O(max)}$	Output Current	Internally Limited	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{op}	Operating Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 40 to + 150	°C

SCHEMATIC DIAGRAM



1/4 ESM1602B

ELECTRICAL CHARACTERISTICS V_{CC} = + 35 V, − 25 °C ≤ T_{amb} ≤ + 85 °C
(unless otherwise specified)

Symbol	Parameter	Value			Unit	Fig.
		Min.	Typ.	Max.		
V_I^+ V_I^-	Input Voltage Range - Note 1 Non-inverting Input Inverting Input	 0 2	 – –	 33 33	V	–
V_C	Input Control Voltage (2 V < V_{CM} < 33 V) - Note 2	150	–	500	mV	8
I_{IB}	Input Bias Current - Note 3	–	1	5	µA	–
I_{SC}	Short-circuit Output Current V_{CC} = + 10 to + 35 V	 6	 –	 25	mA	 9
V_{CC}-V_O	Output Saturation Voltage (high level) - (I_O = − 10 mA)	–	1	1.5	V	11
V_O	Output Saturation Voltage (low level) - (I_O = + 10 mA)	–	1	1.6	V	12
I_{CC}	Supply Current R_L = ∞ for the 4 Comparators R_L Common for the Comparators	 – –	 4 10	 6 13	mA	 13,14
S_{VO}	Output Slew-rate (R_L = 3 KΩ, T_{amb} = + 25 °C)	1	–	–	V/µs	–
V_F	Input Protective Diode Forward Voltage (I = 20 mA, T_{amb} = + 25 °C)	–	–	1.5	V	–
–	Energy of Pulses against which Circuit Output is Protected (T_{amb} = + 25 °C) - Note 4	 –	 –	 20	mJ	–
–	Pulsed Current Applied to Protective Output Diodes (T_{amb} = + 25 °C) - Note 5	 –	– 0.4	 –	A	15

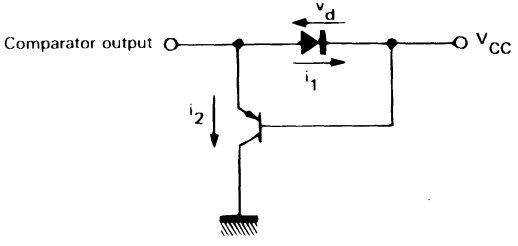
Notes : 1. When negative input is biased between 0 and 2 volts output is always low.

2. Comparator hysteresis voltage on positive input on the one hand and negative input on the other hand equals sum of input control voltages V_{C1} + V_{C2} or V_{C3} + V_{C4}.

3. Input current flows out of the circuit owing to PNP input stage. This current is constant and independent of output level. So no load change is transmitted to inputs.

4. By definition, a circuit is immunized against powerful signals when no durable characteristic change occurs after the application of these signals and when the circuit has not been destroyed.
In industrial surroundings, parasitic signals contain usually high voltage (over 200 V) AC harmonics having variable impedance of 500 Ω to 10 KΩ.
The power dissipation of these signals is divided between clamping diodes and the V_{CC}. Simulation is used to determine the maximum energy level. The injected current value cannot in any case exceed 3 A.

5. Output protective diodes are individually by means of positive and negative discharge voltages of a capacitor. The negative discharge control occurs through a single diode. During positive discharge, due to the properties of integration, a grounded collector PNP transistor appears in parallel with the clamping diode connected to V_{CC}. A part of the current flows through this transistor, V_{CE} being greater than V_{CC}. If T is the total discharge duration, energy dissipated in the circuit is :



$$W = \int_0^T [\, i_1 \cdot v_d + i_2 (V_{CC} + v_d) \,]\, dt$$

For a certain injected current, the lower the current I_2, that is to say the lower the PNP current gain the smaller the energy is dissipated in the circuit. Topology and technological processes have been chosen to shorten this current gain.

Fig. 1 – INPUT BIAS CURRENT.

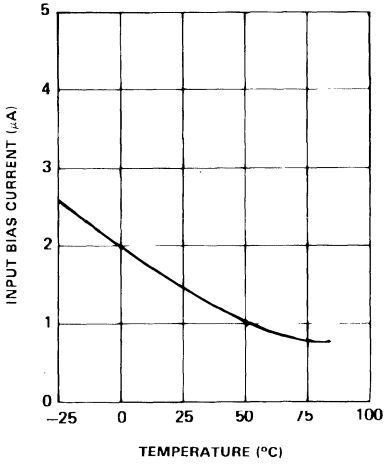


Fig. 2 – OUTPUT SATURATION VOLTAGE.

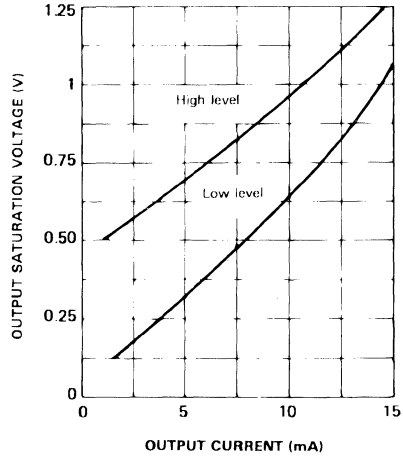


Fig. 3 – OUTPUT SATURATION VOLTAGE.

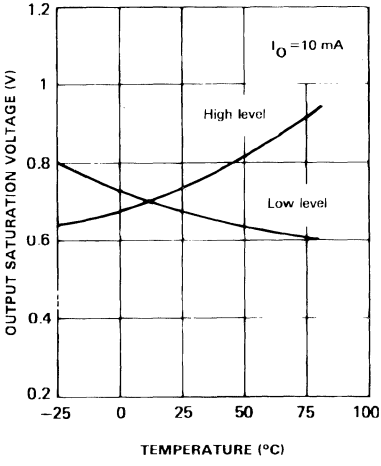
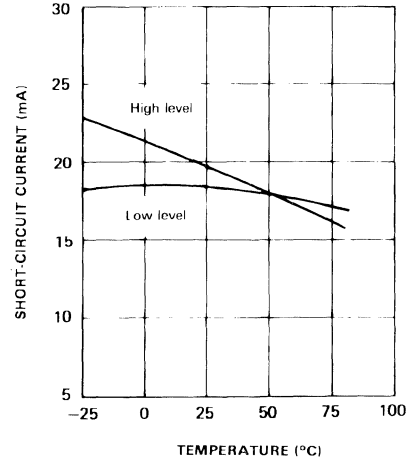


Fig. 4 – SHORT CIRCUIT CURRENT.



TYPICAL APPLICATIONS

Figure 5 : Conversion of DTL, TTL, MOS Signals on a Transmitting Line.

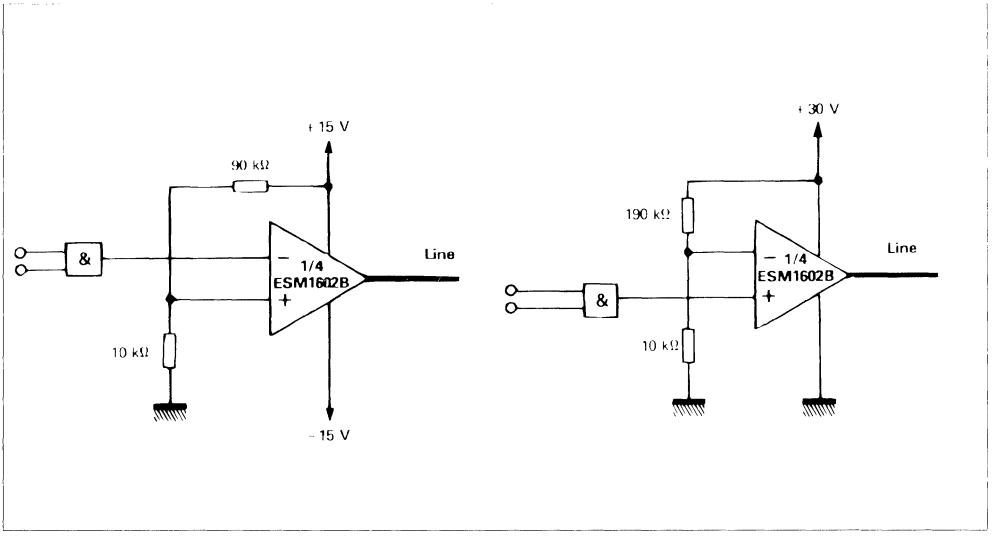


Figure 6 : Reception of Highly Noisy Signals.

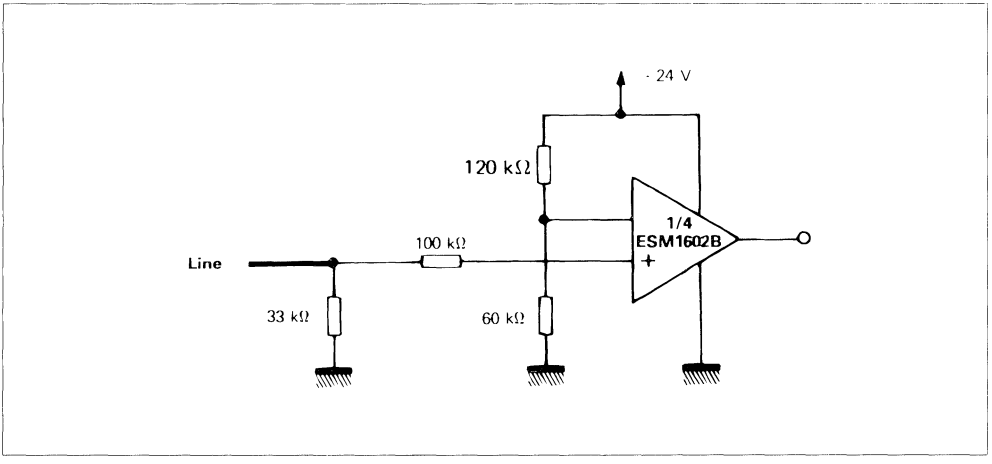
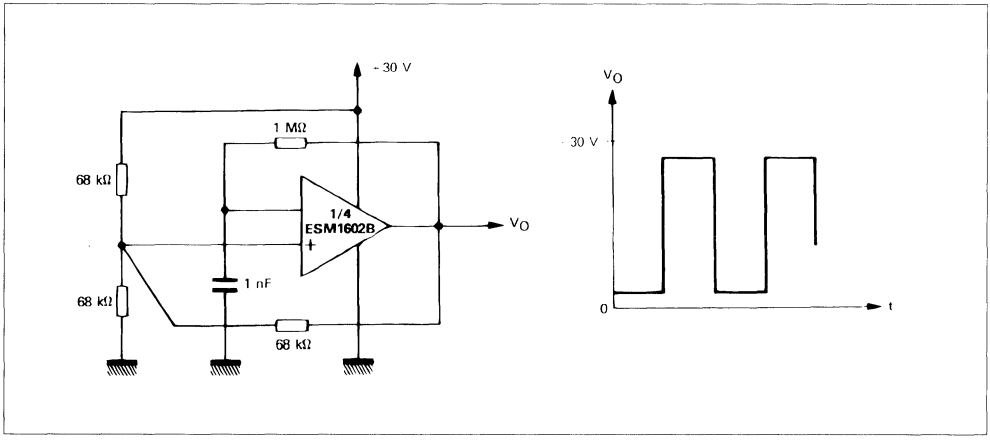


Figure 7 : Free-running Square Wave Oscillator.



TEST CIRCUITS

Figure 8.

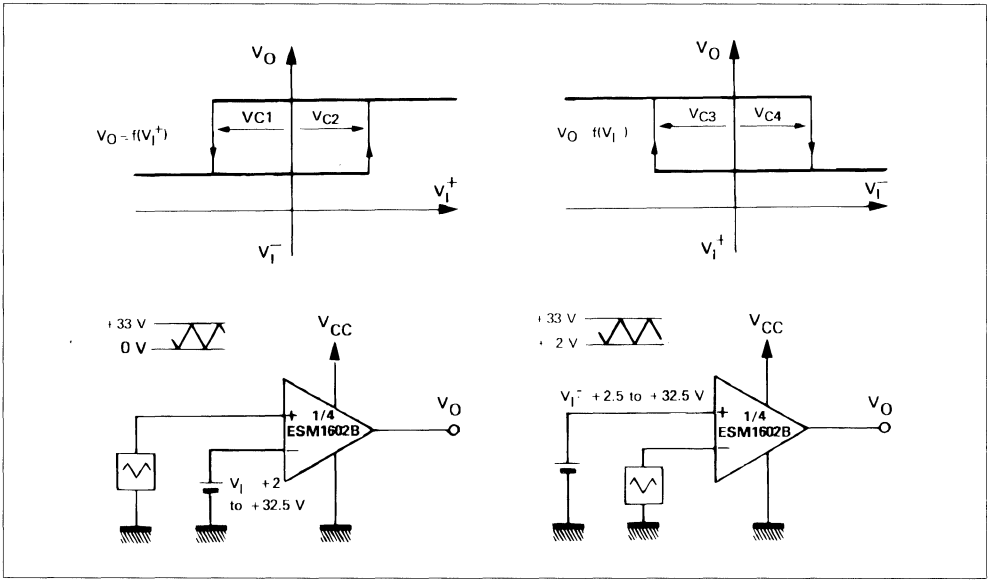


Figure 9.

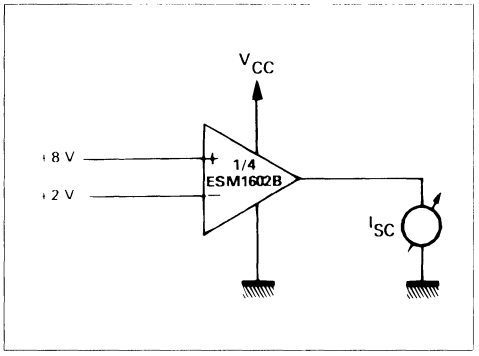


Figure 10.

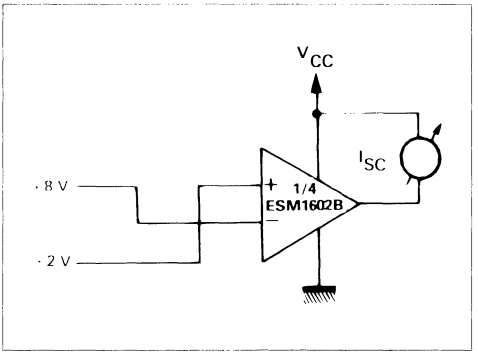


Figure 11.

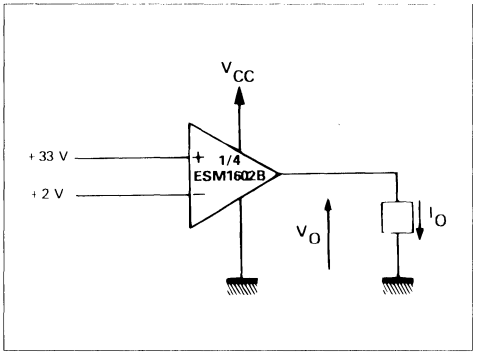


Figure 12.

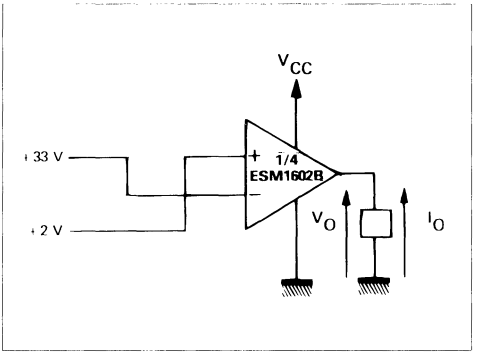


Figure 13.

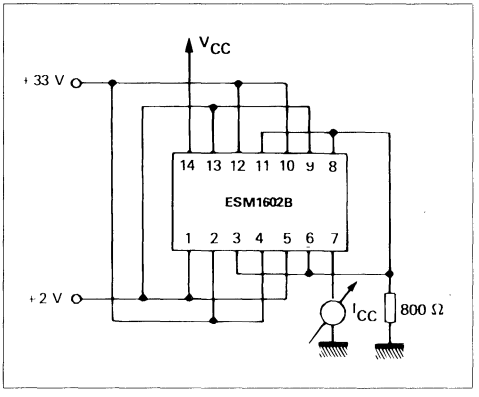


Figure 14.

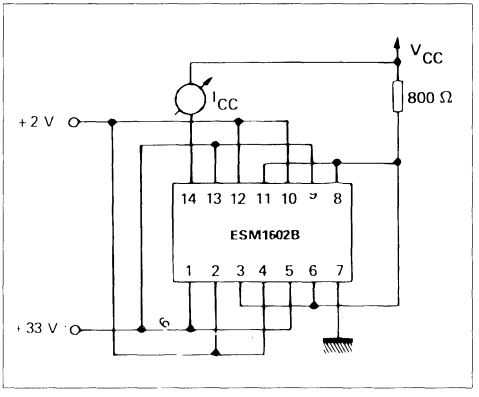


Figure 15.

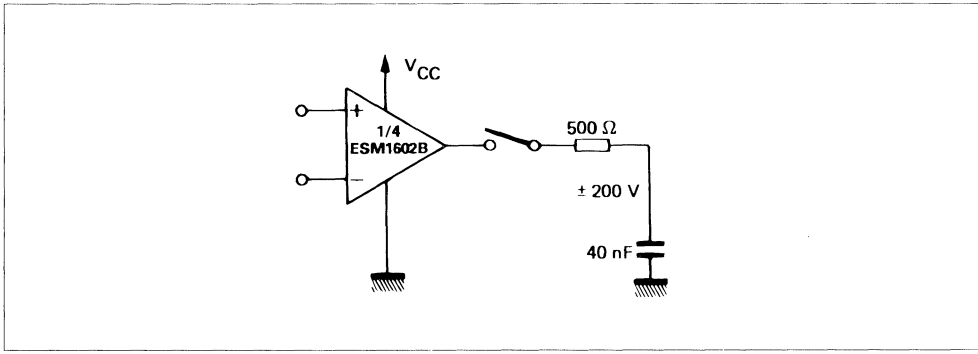
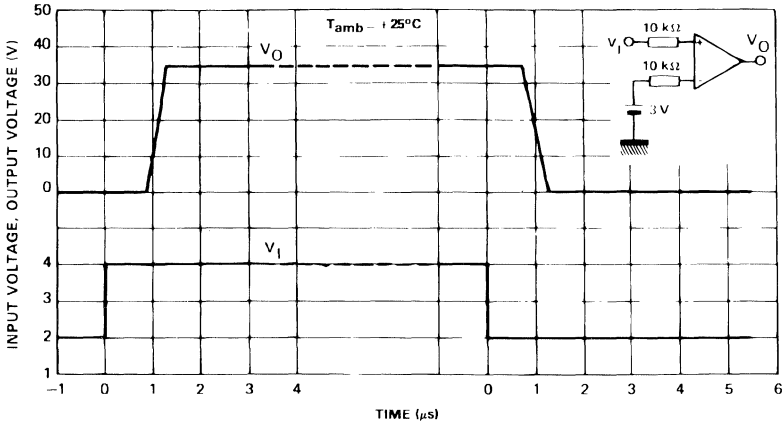


Figure 16 : Response Time.



SGS-THOMSON MICROELECTRONICS

GS-D050

0.5 A SWITCH MODE BIPOLAR STEPPER MOTOR DRIVER MODULE

- NO EXTERNAL COMPONENT REQUIRED
- INPUTS TTL/CMOS COMPATIBLE
- LOGIC INHIBIT/ENABLE
- CHOPPER REGULATION OF MOTOR BIPOLAR CURRENT
- PROGRAMMABLE MOTOR CURRENT (0.5 A max) (by steps or continuously)
- WIDE VOLTAGE RANGE (10-46 V)
- FULL-STEP, HALF-STEP AND QUARTER-STEP OPERATIONS
- OVERTEMPERATURE PROTECTION

ORDER CODE : GS-D050

DESCRIPTION

The GS-D050 is a driver for bipolar stepper motors that directly interfaces a microprocessor and two phase permanent magnet motors.

The motor current is controlled in a chopping mode up to 0.5 A. The small outline makes the GS-D050 ideal when space is a premium.

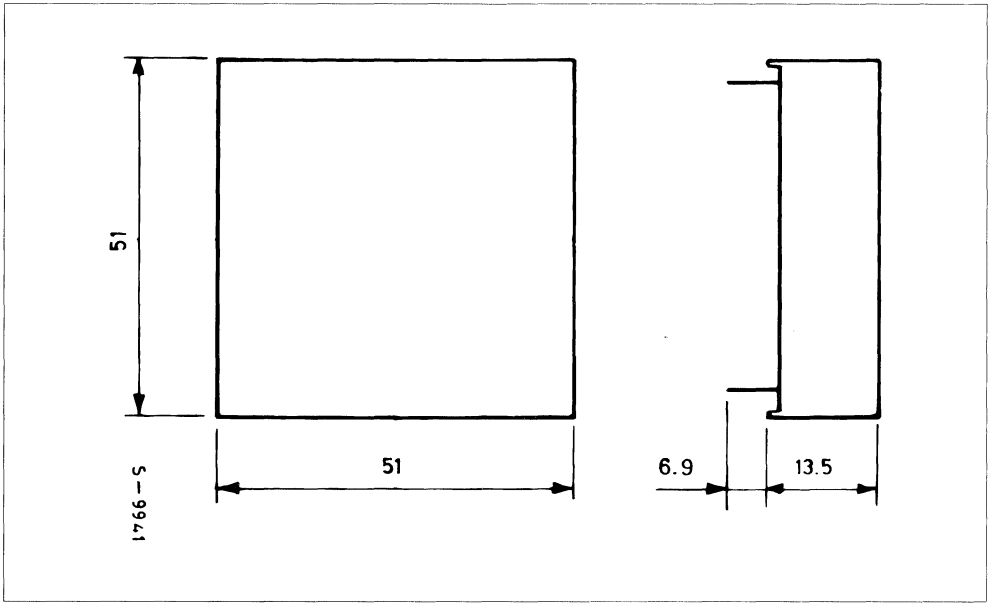
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	46	V
V_{ss}	Logic Supply Voltage	7	V
V_i	Logic Input Voltage	6	V
I_o	Peak Output Current	1.2	A
V_{ref}	Reference Input Voltage	5	V
T_{stg}	Storage Temperature Range	– 40 to + 105	°C
T_{cop}	Operating Case Temperature Range	– 20 to + 85	°C

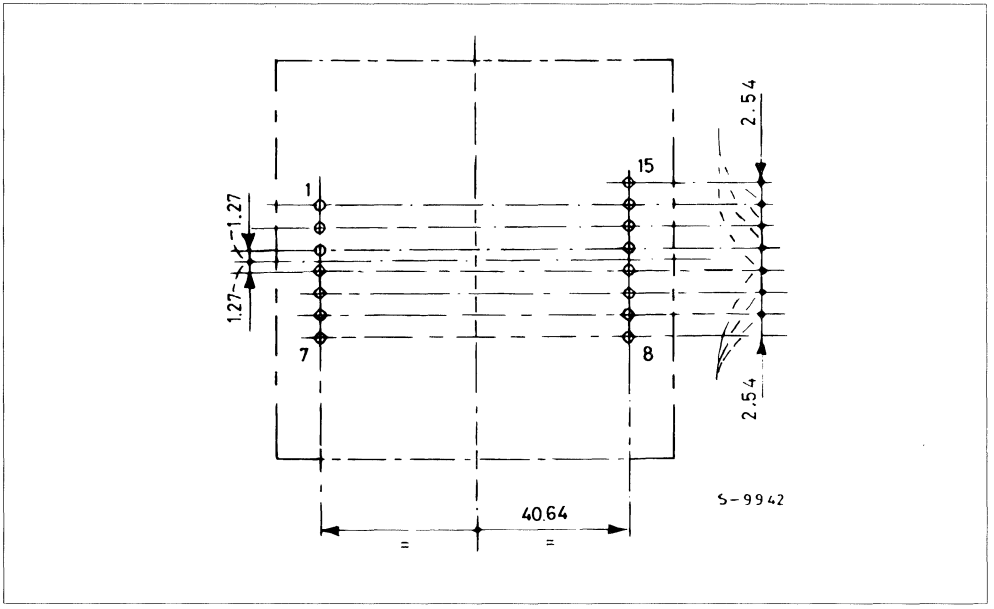
THERMAL DATA

$R_{th\ (c-a)}$	Case-ambient Thermal Resistance	Max	8.0	°C/W

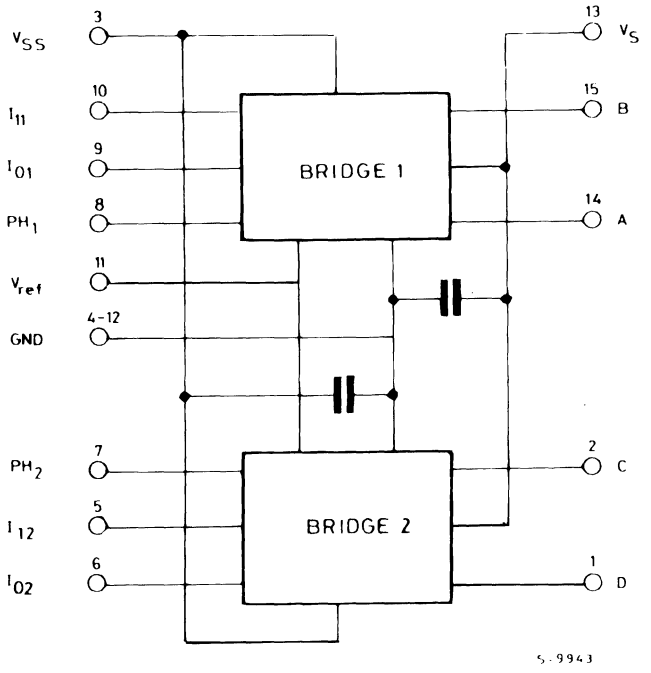
MECHANICAL DATA (dimension in mm)



MOTHER BOARD LAYOUT (top view)



EQUIVALENT BLOCK DIAGRAM OF GS-D050



PIN FUNCTIONS

Pin	Function
1 – D	Bridge Output D. This output has a phase opposite to the driving signal PH2.
2 – C	Bridge Output C. This output has the same phase of the driving signal PH2.
3 – V_{ss}	Logic Supply Voltage. Maximum applicable voltage is 7 V.
4 – GND	See Pin 12
5 – I_{12}	Input pin for current level and operating mode selection (see I_{11} description).
6 – I_{02}	Input pin for current level and operating mode selection (see I_{11} description).
7 – PH2	Phase 2 Logic Input
8 – PH1	Phase 1 Logic Input
9 – I_{01}	Input pin for current level selection (see I_{11} description)
10 – I_{11}	Input pin used, together with I_{01}, to select the current level according to the following table. I_{11}/I_{12} I_{01}/I_{02} Phase Current 0 0 I_{ph} = 100 % I_{set} 0 1 I_{ph} = 60 % I_{set} 1 0 I_{ph} = 19 % I_{set} 1 1 No Current
11 – V_{ref}	Reference Input Voltage for the Chopper Comparators. The voltage applied to this pin settles the phase current to the desired value. A 5 V ref sets a 0.5 A phase current when full-step drive is selected.
12 – GND	Ground Connection. Motor and logic supply voltage must be referenced, as well as the logic signals, to this pin.
13 – V_s	Motor Unregulated Supply Voltage. Maximum Applicable Voltage is 46 V.
14 – A	Bridge Output A. This output has the same phase of the driving signal PH1.
15 – B	Bridge Output B. This output has a phase opposite to the driving PH1.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specifed)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage	Pin 13	10		46	V
V_{ss}	Supply Voltage	Pin 3	4.75	5	5.25	V
I_s	Quiescent Supply Current	Pin 13 V_s = 35 V I_{out} = 0		15	30	mA
I_{ss}	Quiescent Supply Current	Pin 3. All Input High I_{out} = 0 V_{ss} = 5 V		15		mA
V_i	Input Voltage	Pin 5, 6, 7, 8, 9, 10 Low High	 2.0		0.8 V_{ss}	V V
I_i	Input Current	Pin 5, 6, 7, 8, 9, 10 Low High			0.4 10	mA µA
V_{sat}	Source Saturat. Voltage	Pin 1, 2, 14, 15 I_o = 0.5 A Conduction Period			2.1	V
V_{sat}	Source Saturat. Voltage	Pin 1, 2, 14, 15 I_o = 0.5 A Recirculation Period			1.4	V
V_{sat}	Sink Saturat. Voltage	Pin 1, 2, 14, 15 I_O = 0.5 A			1.4	V

MODULE OPERATION

The module consists of two identical sections each of them driving one winding of a bipolar permanent magnet stepper motor.

A brief description is given for one section.

An H bridge output stage (fig. 1) drives the winding of the motor by a constant current up to 0.5 A. The direction of the current depends on which diagonal of the H bridge is activated.

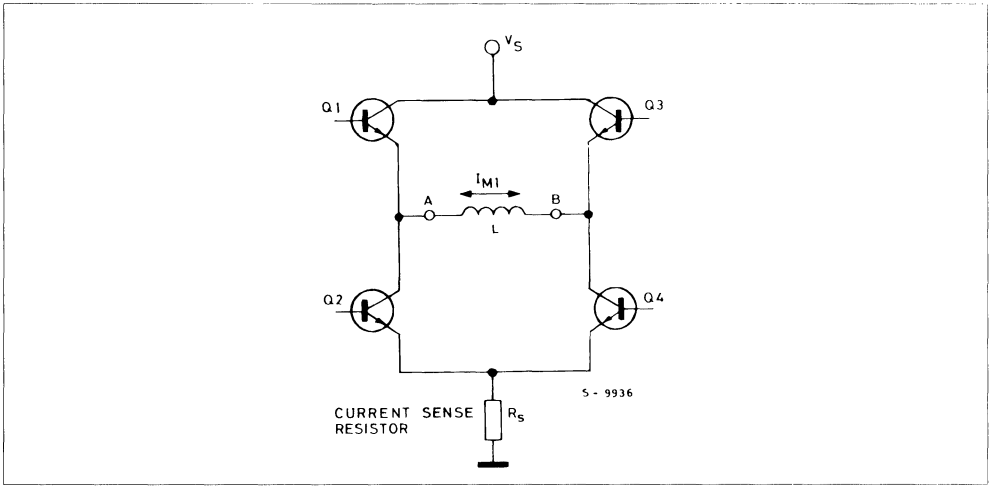
The input signal PH1 selects the diagonal. (See block diagram). When PH1 is high the two transistors Q_1 and Q_4 are switched ON and the current is sourced by the A pin and sinked by the B pin. When PH1 is low, Q_3 and Q_2 are switched ON. At switch ON the current through the winding increases almost linearly according to the equation :

$$\frac{dI_{M1}}{dt} = \frac{V_S}{L}$$

being L the inductance of the winding.

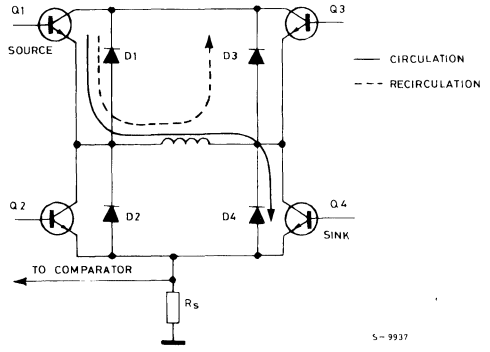
This current is sensed by a current sense resistor R_S and the voltage drop is compared to a reference voltage.

Figure 1 : Output Bridge Circuit.



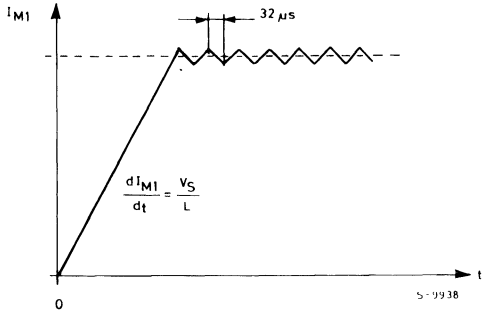
When the voltage drop is higher than reference the sink transistor (for example Q_4) is switched off and the current decays through the source transistor and the recirculating diode D3 (fig. 2).

Figure 2 : Current Paths During Current Level Control.



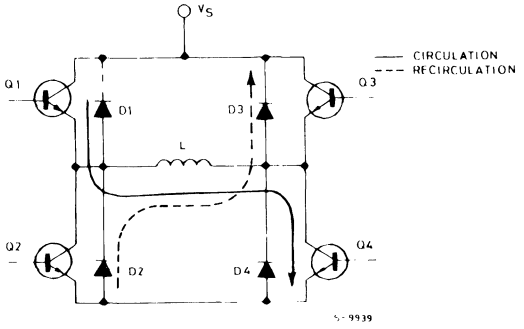
The module contains a monostable circuit that keeps OFF Q_4 for a fixed period of time (t_{OFF} = 32 µS). After t_{OFF}, Q_4 is switched on again and the cycle is repeated as long as PH1 signal is high fig 3).

Figure 3 : Output Current Waveforms.



When the signal PH1 changes state (from high to low), both Q_1 and Q_4 are switched OFF and Q_2 and Q_3 are switched ON. The current recirculates through D2 and D3 until it decays to zero and then it reverses the direction (fig. 4).

Figure 4 : Current Path During Phase Reversal.

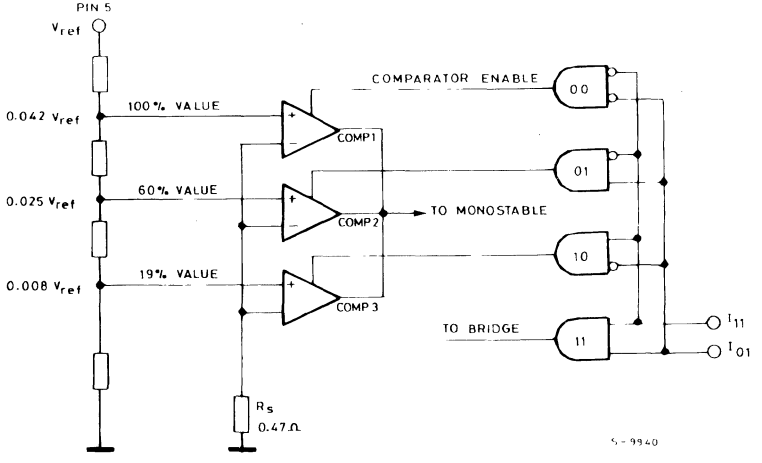


The current phase reversal is therefore obtained by a four quadrant operation while the current level control is by a two quadrant operation. The current decay by a four quadrant is faster being the total voltage applied to the winding almost equal to supply voltage.

The decay time during chopping control of the current level is internally fixed (t_{OFF}), the applied voltage to the inductance is also fixed (about 3 V) and, therefore, the amplitude of current decay or the current ripple depends exclusively on the value of L.

The level of the maximum current is fixed and controlled by a set of voltage dividers and comparators. Four current levels can be digitally selected according to the status of I_{11} and I_{01} (See block diagram and fig. 5).

Figure 5 : Current Level Setting.



When $I_{11} = I_{01} = 1$ the H bridge is disactivated and no current can circulate.

For $I_{11} = 0$; $I_{01} = 0$ the comparator 1 is enabled. The maximum current is allowed to flow through the bridge and the value of the current is given by

$$I_M = \frac{0{,}042\ V_{ref}}{R_S} = 100\ \%$$

$R_S = 0.47\ \Omega$ is internally fixed. For $V_{ref} = 5$ V the maximum allowed current is 0.45 A.

For $I_{11} = 0$; $I_{01} = 1$ the comparator 2 is enabled and the current is reduced to 60 % of the maximum value.

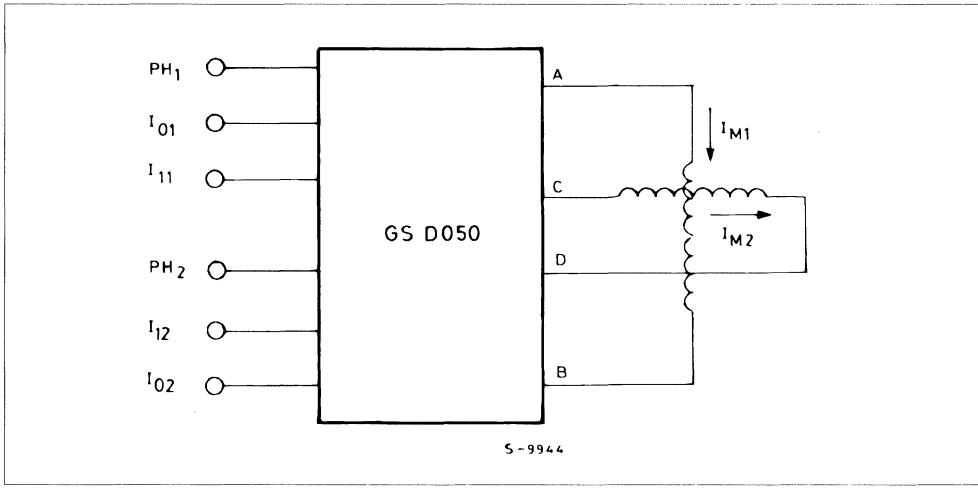
For $I_{11} = 1$; $I_{01} = 0$ the comparator 3 is enabled and the current is reduced to 19 %.

When in Wave or Half Step mode, the signals I_{11} and I_{01} are used also for the correct timing.

The following paragraphs show the mode operation of the GS-D050 making reference to the schematic of fig. 6.

The current is considered positive when flowing from A to B or from C to D.

Figure 6 : Basic GS-D050 Inputs and Outputs.



ONE PHASE ON OR WAVE DRIVE

Only one winding is energized at any given time according to the sequence (for FWD direction)

AB ; CD ; BA ; DC ;

(BA means a negative current flowing from B to A).

Fig. 7 and 8 show the timing of the input signals and of the output currents.

Figure 7 : Wave Drive FWD Direction.

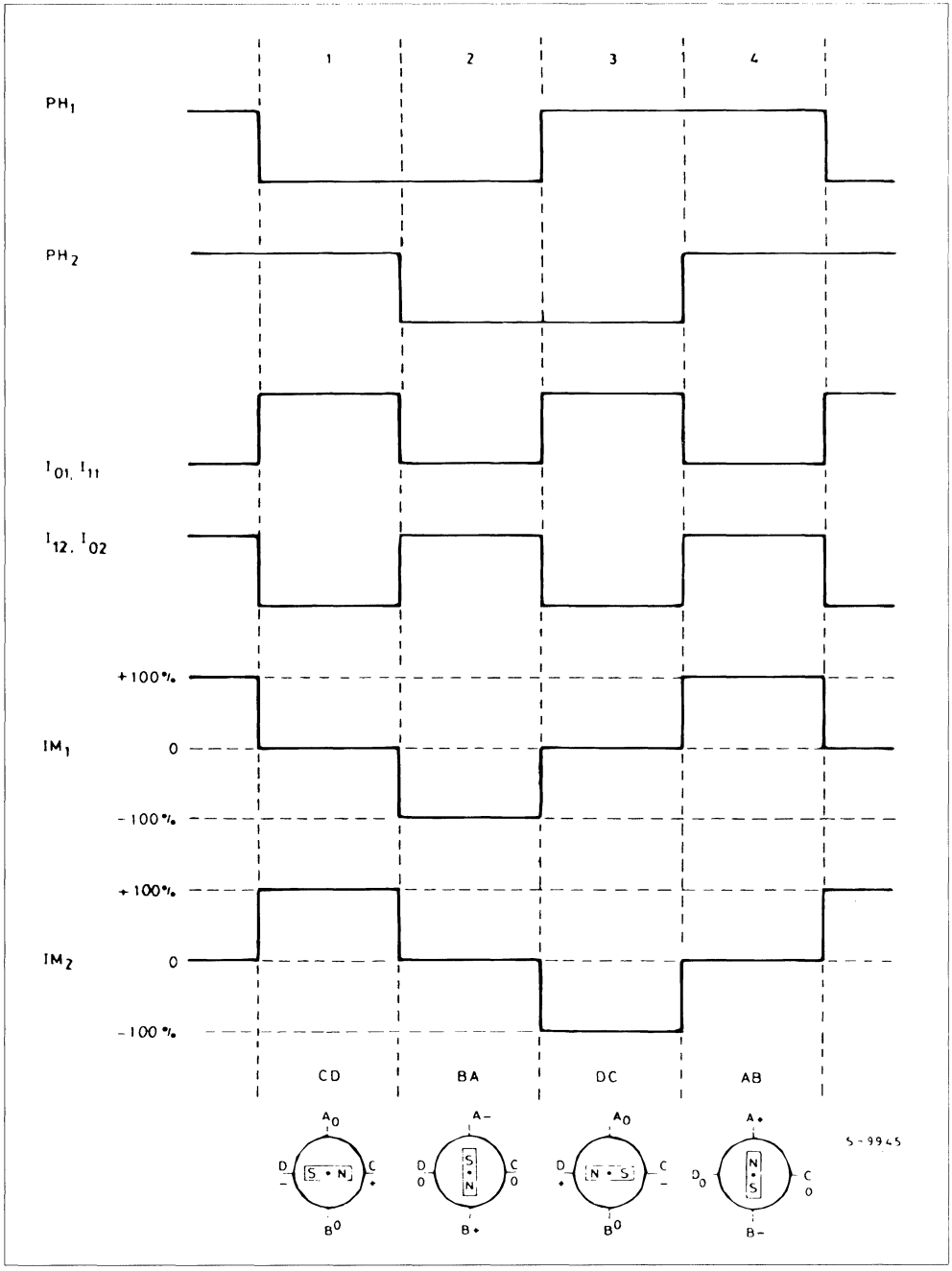
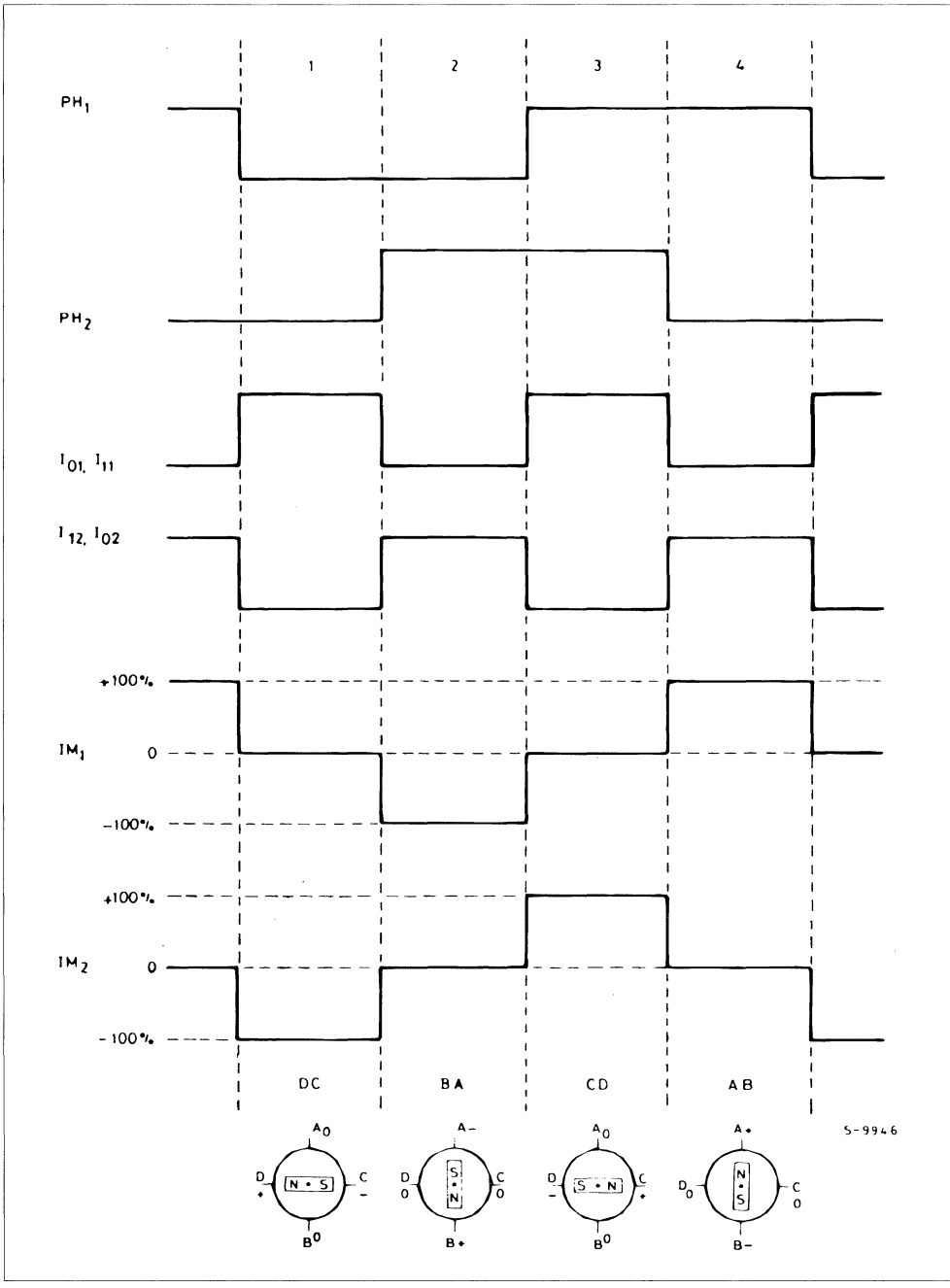


Figure 8 : Wave Drive REV Direction.



TWO PHASE ON OR NORMAL DRIVE

Two windings are energized at any given time according to the sequence (FWD direction).

AB & CD ; CD & BA ; BA & DC ; DC & AB

In this case I_{01}, I_{11} signals are used just for current level set.

Fig. 9 and 10 show the timing or various signals.

Figure 9 : Two Phase on -FWD Direction.

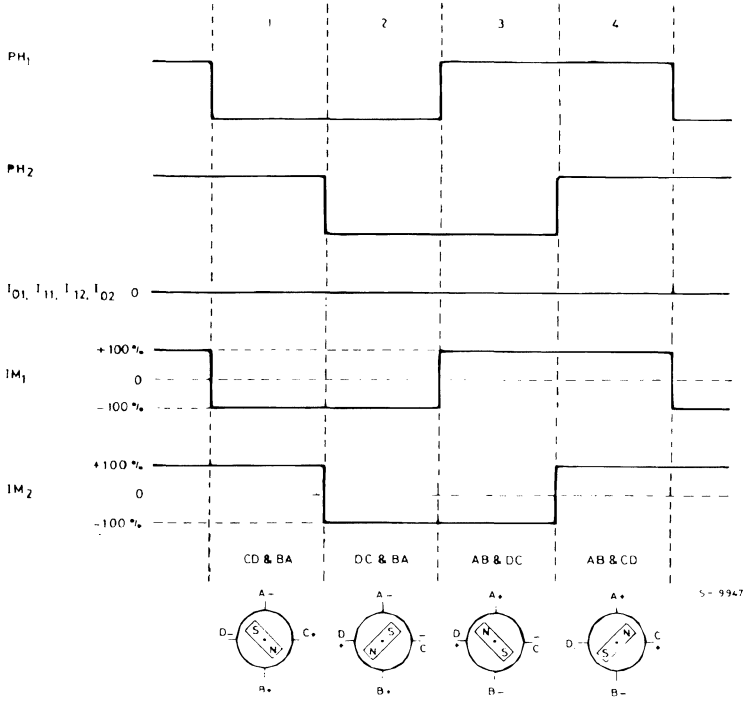
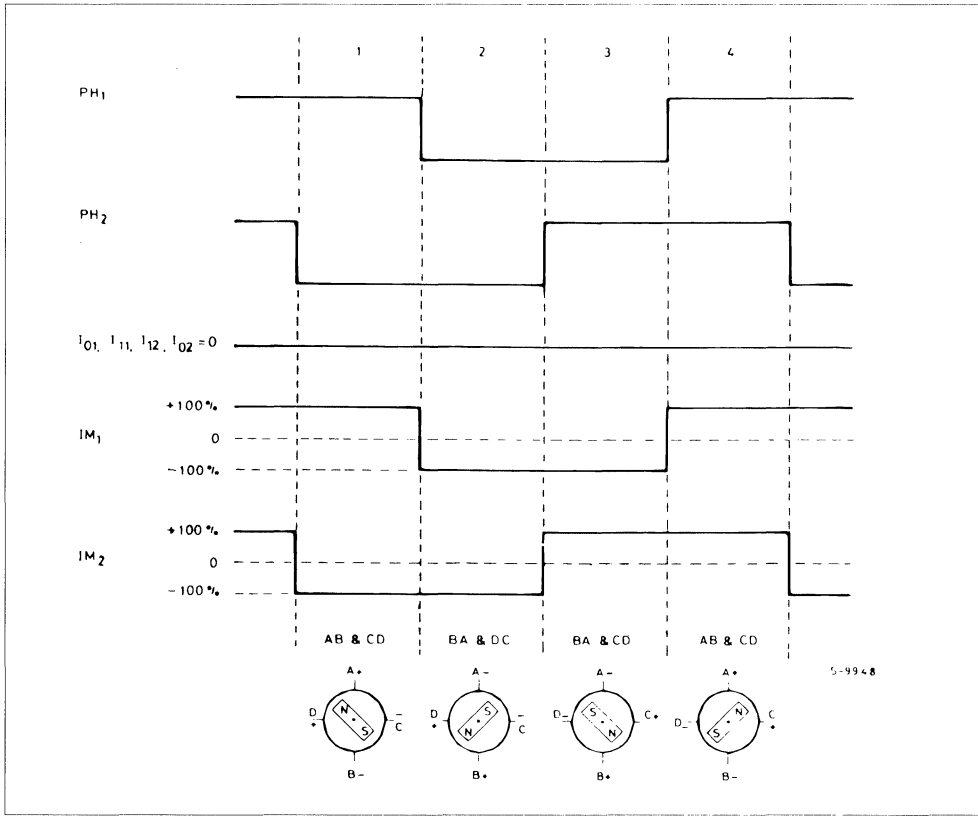


Figure 10 : Two Phase on -REV Direction.



HALF STEP DRIVE

By this mode one winding or two windings are alternatively energized. Eight steps are required for a complete revolution of the rotor.

For FWD direction the sequence is :

AB ; AB & CD ; CD & BA ; BA ; BA & DC ; DC ; DC & AB

Fig. 11 and 12 show the timing of various signals.

Figure 11 : Half Step -FWD Direction.

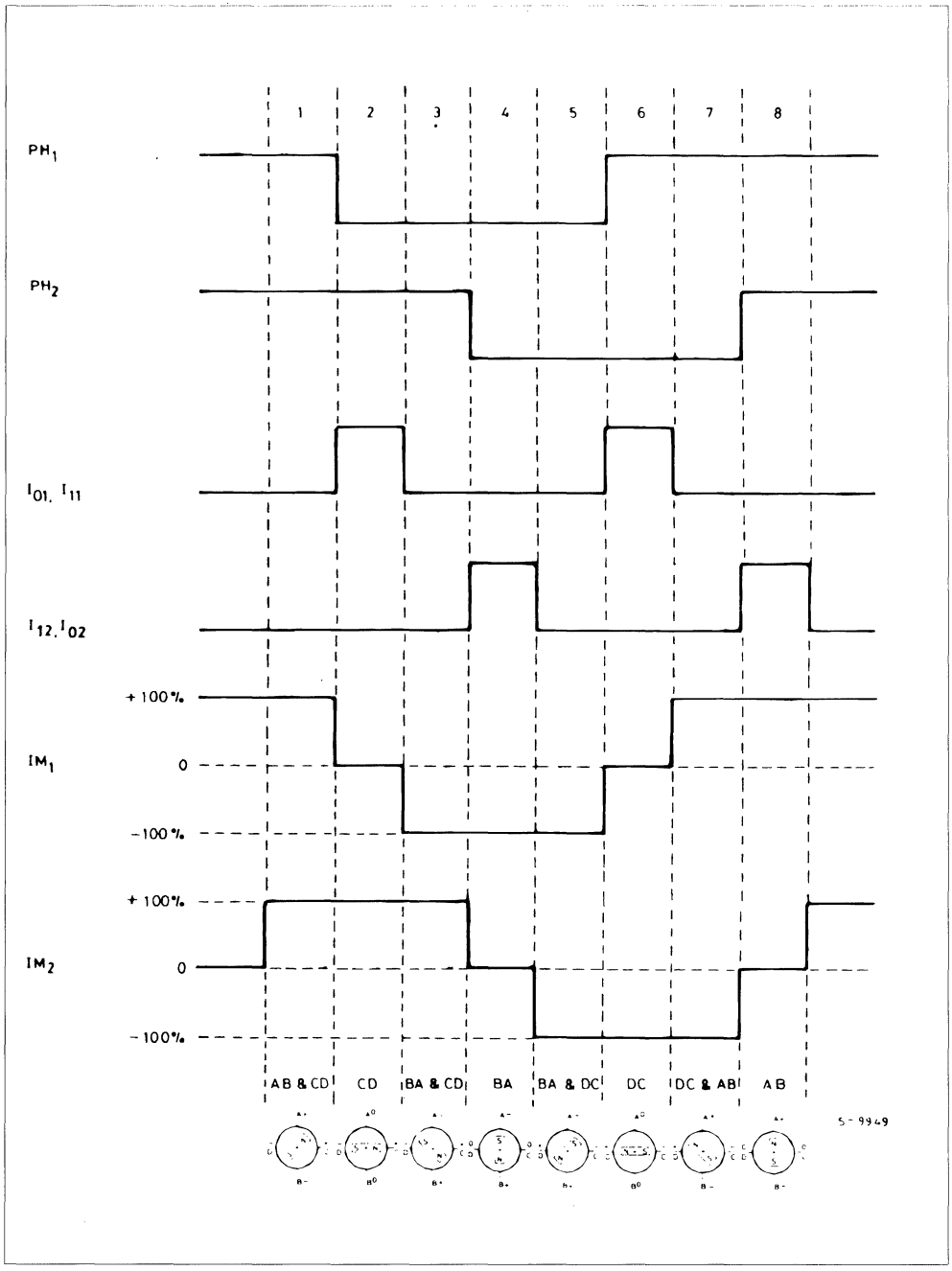


Figure 12 : Half Step -REV Direction.

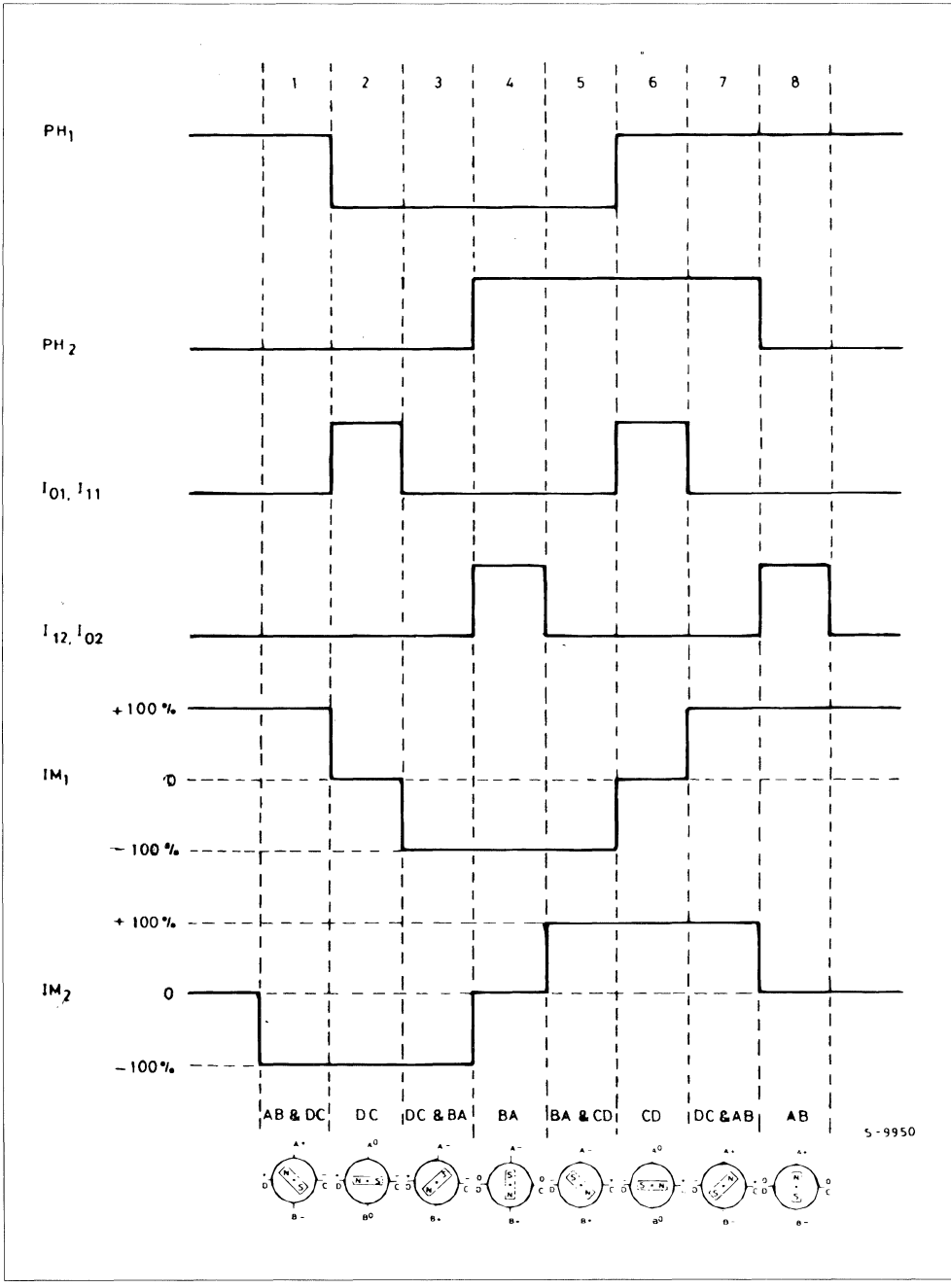


Figure 13 : Quarter Step-FWD Direction.

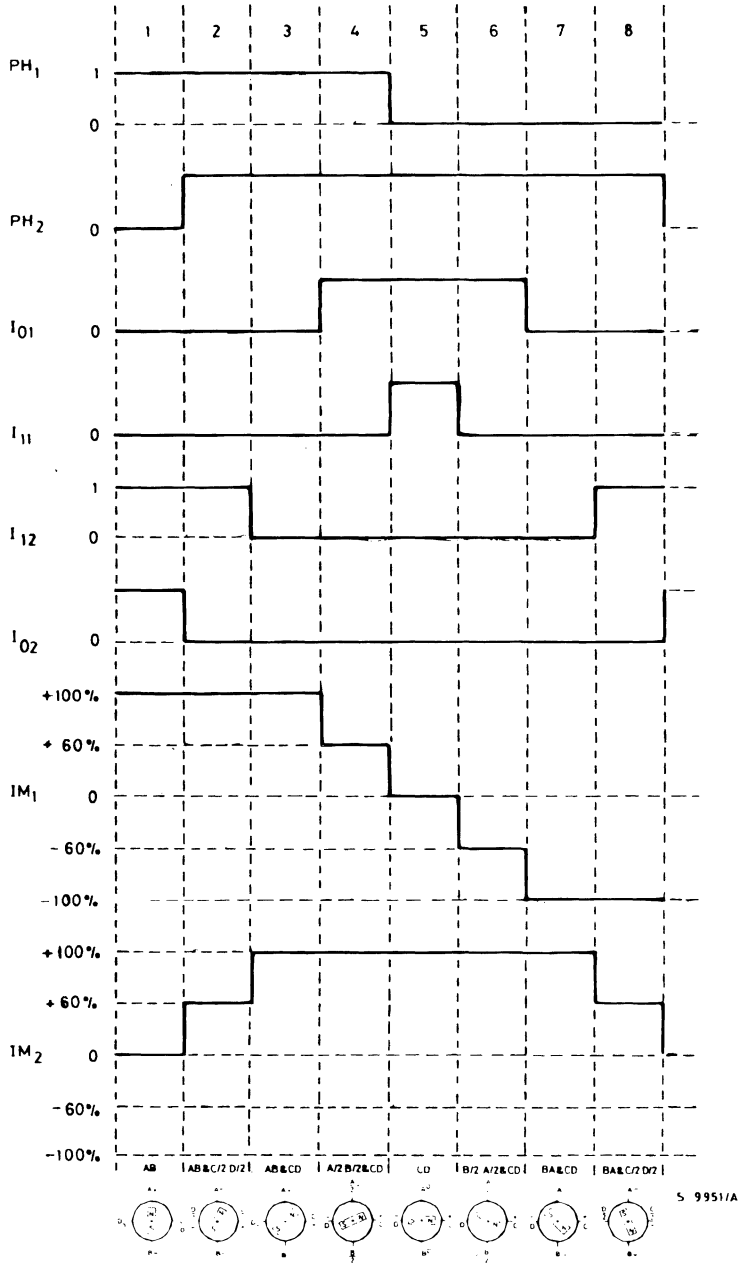
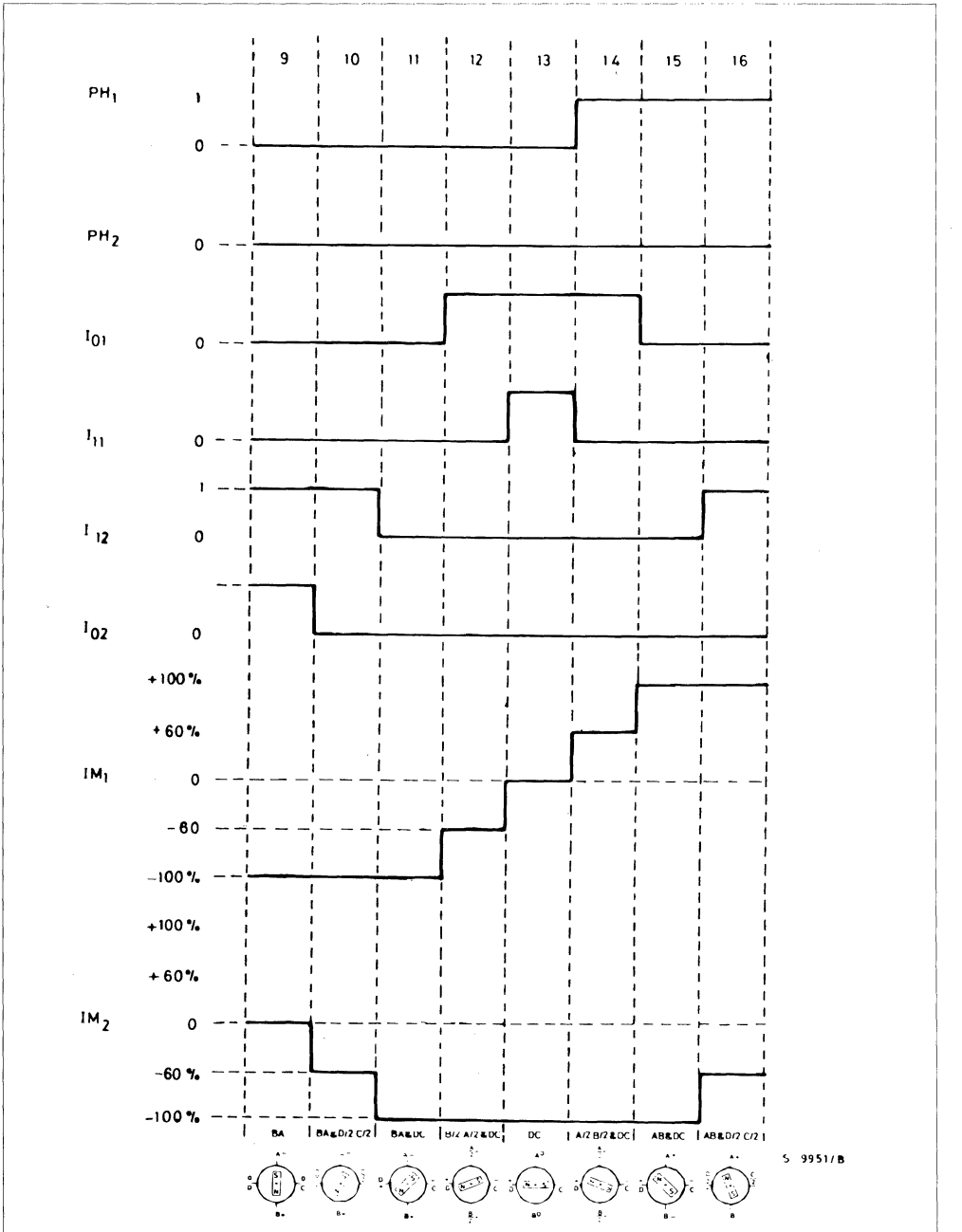


Figure 13 : Quarter Step-FWD Direction (continued).



For Wave, normal, half step, the driving can be made at any current level : for simplicity the previous diagrams refer to a condition where 100 % of the motor current is used, as set by the equation.

$$I_H = \frac{0.042\ V_{ref}}{R_S}$$

In half step mode it is advisable to reduce the current level to 60 % of the maximum when two windings are energized and to use the maximum value when one winding is energized : this allows a less irregular torque.

This operation can be simply performed by selecting the proper status of I_{01} and I_{02}.

QUARTER STEP DRIVE

It is preferable to perform the quarter step drive at full power to have a more regular torque.

The extra quarter steps are added to the half step sequence by putting one winding at half current according to the sequence.

AB ; AB & $\frac{CD}{2}$; AB & CD ; $\frac{AB}{2}$ & CD ; CD ;

CD & $\frac{BA}{2}$; CD & BA ; $\frac{CD}{2}$ & BA ; BA ;

BA & $\frac{DC}{2}$; BA & DC ; $\frac{BA}{2}$ & DC ; DC ;

DC & $\frac{AB}{2}$; DC & AB ; $\frac{DC}{2}$ & AB.

The timing for forward direction is shown on fig. 13. 16 steps are required for one complete revolution.

APPLICATION CIRCUIT

A typical application is shown on fig. 14 for a maximum winding current of about 0.5 A.

As shown, no external component is needed to drive the motor.

Signals I_{01}, I_{11}, I_{02}, I_{12} may be used to inhibit the module when they are permanently kept at high level. If they are left open, the GS-D050 treats them as at high logic level.

The case of the GS-D050 is electrically connected to ground : radiated EMI caused by chopping operation is therefore shielded by the case itself.

To reduce further EMI a low pass filter can be inserted across the outputs of the GS-D050 as shown on fig. 15.

L, C, components should be selected according to

$$L \approx \frac{L_M}{10} \qquad C = \frac{4 \cdot 10^{-10}}{L}$$

The module is protected against thermal overload.

If by any reasons (very high ambient temperature or high power dissipation or both) the junction temperatures of active components inside the GS-D050 reach 150 C the module automatically reduces the output power and the power dissipation.

Even if the module controls the maximum output current, a short circuit of the outputs can damage the device.

Figure 14 : GS-D050 Basic Application Circuit.

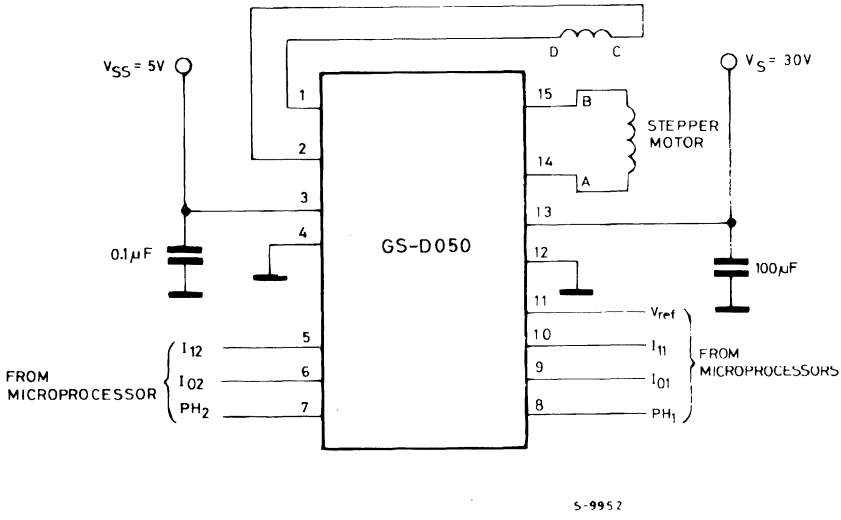
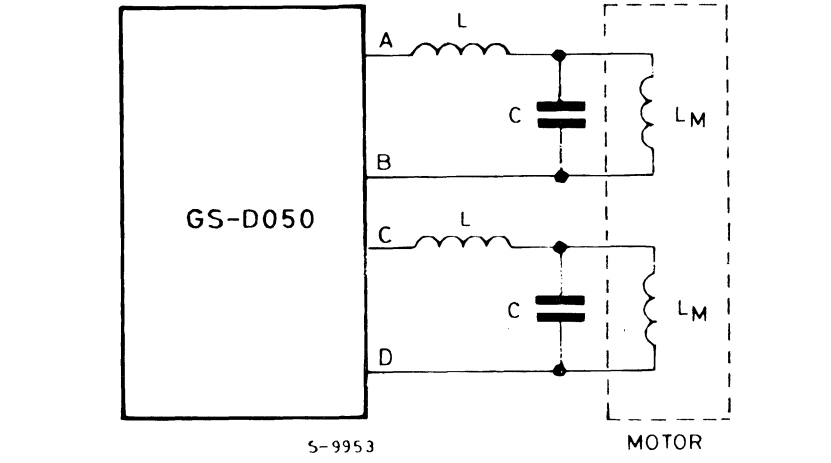


Figure 15 : Circuit for EMI Reduction.

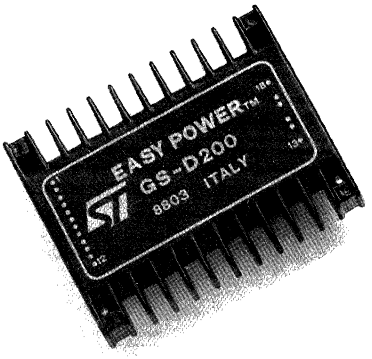


SGS-THOMSON MICROELECTRONICS

GS-D200

SWITCH MODE BIPOLAR STEPPER MOTOR DRIVER MODULE

- NO EXTERNAL COMPONENT REQUIRED
- NORMAL, WAVE, HALF STEP DRIVE CAPABILITY
- INPUTS TTL/CMOS COMPATIBLE
- CHOPPER REGULATION OF MOTOR CURRENT
- PROGRAMMABLE MOTOR CURRENT (2 A max)
- WIDE VOLTAGE RANGE (10–46 V)
- SELECTABLE SLOW/FAST CURRENT DECAY
- SYNCHRONIZATION FOR MULTIPLE APPLICATION
- REMOTE INHIBIT/ENABLE
- HOME POSITION INDICATOR
- OVERTEMPERATURE PROTECTION



ORDER CODE :
GS-D200

DESCRIPTION

The GS-D200 is a complete controller and driver for bipolar stepper motors that directly interfaces a microprocessor and two phase permanent magnet motors.

The motor current is controlled in a chopping mode up to 2 A. High flexibility in use is provided by GS-D200 that, furthermore, reduces the burden on the microprocessor and simplifies the software development in a complete microprocessor controlled stepper motor system.

ABSOLUTE MAXIMUM RATINGS

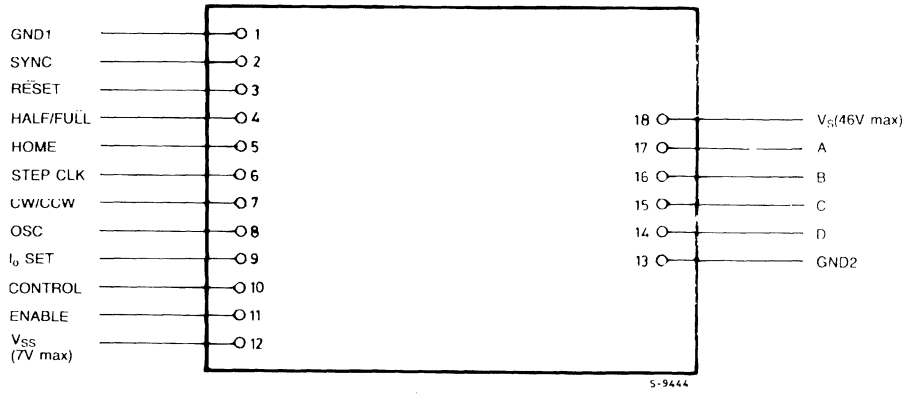
Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 18)	48	V
V_{ss}	Logic Supply Voltage (pin 12)	7	V
I_o	Peak Output Current	2	A
T_{stg}	Storage Temperature Range	– 40 to + 105	°C
T_{cop}	Operating Case Temperature Range	– 20 to + 85	°C

Recommended maximum operating input voltage is 46 V.

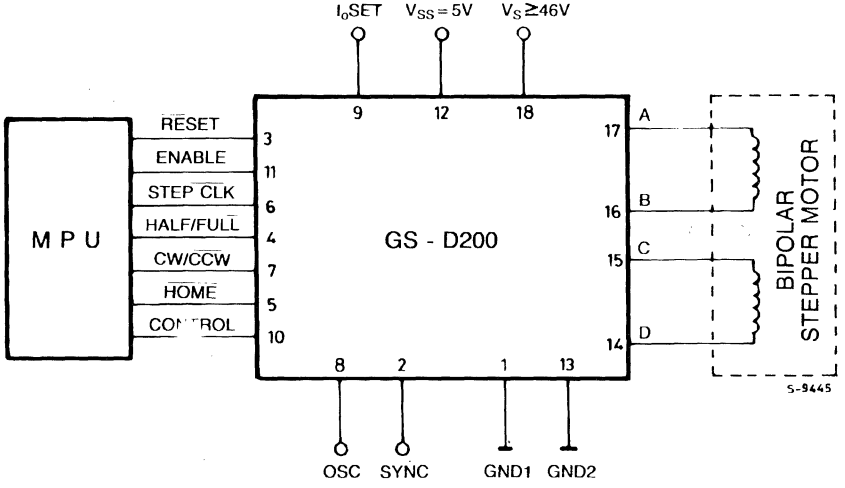
THERMAL DATA

$R_{th\ (c\text{-}a)}$	Case-ambient Thermal Resistance	Max	5.0	°C/W

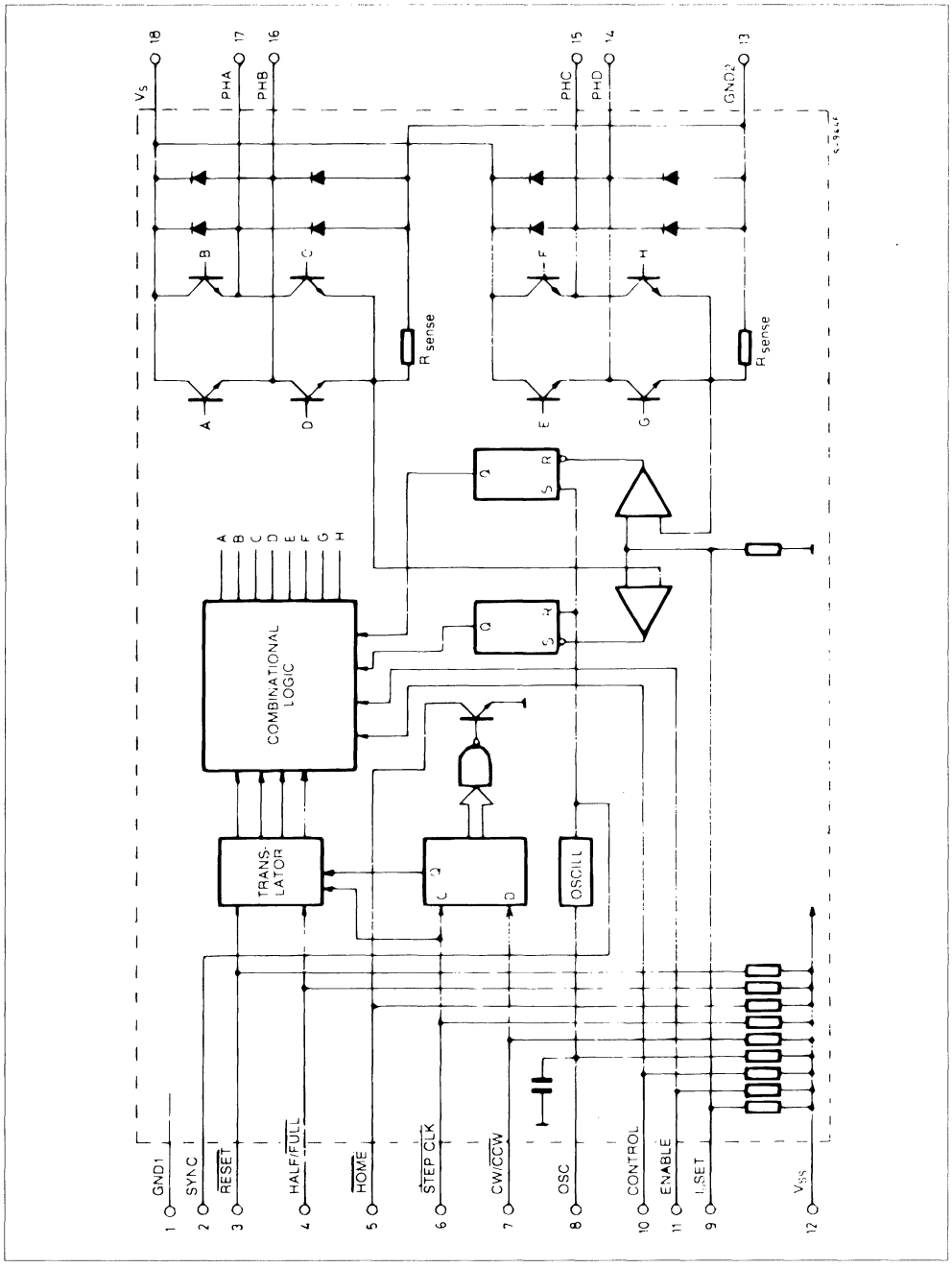
CONNECTION DIAGRAM (top view)



TYPICAL APPLICATION



EQUIVALENT BLOCK DIAGRAM OF GS-D200



PIN FUNCTIONS

Pin	Function
1 – GND1	Common Ground for Low Current Path
2 – SYNC	Output of the Module Chopper Oscillator. Several GS-D200 can be synchronized by connecting together all SYNC pins (see later). An external chopper clock source, if used, must be injected at this pin.
3 – $\overline{\text{RESET}}$	Reset Asynchronous Input. An active low pulse on this input restores the module to the $\overline{\text{HOME}}$ position (ABCD = 0101).
4 – HALF/$\overline{\text{FULL}}$	Half/Full Step Select Input. When high or not connected, it selects half step operation, when low it selects full step operation.
5 – $\overline{\text{HOME}}$	Output that indicates when the module is in its initial state (active low : ABCD = 0101 = state 1). This signal should be ANDed with the output of a mechanical home position sensor of the motor.
6 – $\overline{\text{STEPCLK}}$	A Pulse on this input moves the motor by one step. The step occurs on the rising edge of this signal.
7 – CW/$\overline{\text{CCW}}$	Clockwise/Counterclockwise Direction Control Input. When high or not connected clockwise rotation is selected. Physical direction of motor rotation depends also on connection of windings. Direction can be changed at any time being this signal synchronized inside the module.
8 – OSC	The chopper frequency of the module is internally fixed at ~ 17 KHz. This frequency can be increased by connecting a resistor between this pin and Vss or decreased by connecting a capacitor between this pin and GND1. When multi-GS-D200 configurations must be synchronized, this pin is connected to ground on all but one module.
9 – I_0 SET	The Motor Phas Current is Set at 1 A. This current can be decreased by connecting a resistor between this pin and GND1, or increased by connecting a 10 KΩ min resistor between this pin and V_{ss}.
10 – CONTROL	Control input that defines the motor current decay inherent to chop mode control. When low, a fast decay is obtained ; when high, or not connected, slow current decay is imposed to the motor current.
11 – ENABLE	Module Enable Input. When low the module is inhibited. When high or not connected the module is active.
12 – V_{ss}	5 V Supply Input. Maximum Voltage must not exceed 7 V.
13 – GND2	Common Ground for High Current Path
14 – D	Phase D Output
15 – C	Phase C Output
16 – B	Phase B Output
17 – A	Phase A Output
18 – V_s	Module Supply Voltage. Maximum voltage must not exceed 46 V.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specifed)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage	Pin 18	10		46	V
V_{ss}	Supply Voltage	Pin 12	4.75	5	5.25	V
I_s	Quiescent Supply Current	Pin 18 I_{out} = 0 V_s = 42 V		15	20	mA
I_{ss}	Quiescent Supply Current	Pin 12. All Input High I_{out} = 0 V_{ss} = 5 V		60		mA
V_i	Input Voltage	Pin 3, 4, 6, 7, 10 Low High	 2.0		0.8 V_{ss}	V V
I_i	Input Current	Pin 5, 4, 6, 7, 10 V_i = Low V_i = High			0.6 10	mA µA
V_{en}	Enable Input Votlage	Pin 11 Low High	 2.0		0.8 V_{ss}	V V
I_{en}	Enable Input Current	Pin 11 V_{en} = L V_{en} = H			0.6 10	mA µA
V_{home}	Home Output Voltage	Pin 5 Low I_{home} = 5 mA High			0.4 V_{ss}	V V
V_{sat}	Source Saturat. Voltage	Pin 14, 15,16, 17 I_o = 1 A			1.8	V
V_{sat}	Source Saturat. Voltage	Pin14, 15, 16, 17 I_o = 1 A			1.8	V
f_c	Chopper Freq.			17		KHz
f_{clk}	Stepclk Width	Pin 6 See Fig. a	0.5			µs
t_s	Set Up Time	See Fig. a	1.0			µs
t_h	Hold Time	See Fig. a	1.0			µs
t_R	Reset Width	See Fig. b	1.0			µs
t_{Rclk}	Reset to Clock Set Up Time	See Fig. b	1.0			µs

Figure a.

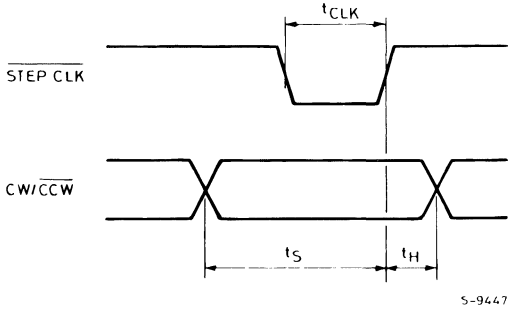
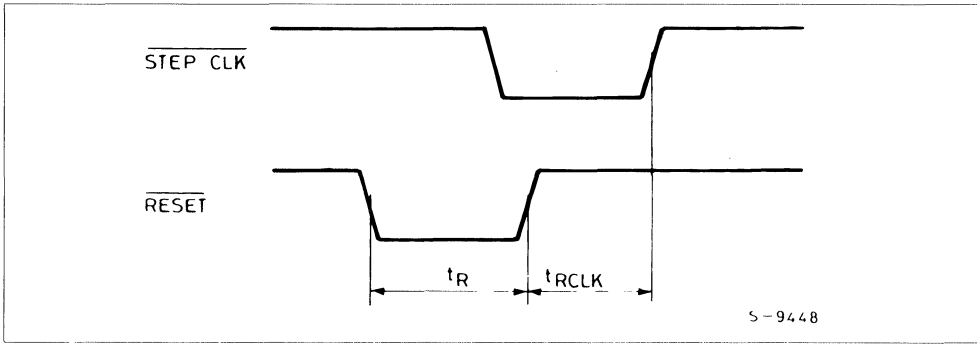


Figure b.



MODULE OPERATION

The GS-D200 is a complete bipolar stepper motor driver that incorporates all the small signal and power functions to directly interface a microprocessor and a two phase permanent magnet motor (see the typical application). Very few information must be delivered by the microprocessor to the module :

- step clock
- direction (clockwise or counterclockwise)
- mode (half or full step)
- reset and enable
- current decay (slow or fast)

Based on this information, the module generates the proper four phases sequence to directly drive a two phase bipolar motor. Therefore the GS-D200 greatly simplifies the task of the microprocessor and of the system programmer.

No external component is needed to operate the GS-D200. However, to add flexibility in use, some internally set functions can be modified externally, like the maximum current flowing through the motor windings and the switching frequency of the current chopper, by addition of few inexpensive passive components (resistor and capacitor).

If any of logic input is left open, the module forces them to high level.

The GS-D200 is housed in a metal case that provides heatsink and shielding against radiated EMI. The thermal resistance case to ambient is about 5 °C/W. This means that for each watt of internal power dissipation the case temperature is + 5 °C above ambient temperature. It is recommended to keep the case temperature below 85 °C in operating conditions.

According to ambient temperature and / or to power dissipation, an additional heatsink may be required : the mounting of optional heatsink is made easy by the four holes provided on the top of the metal case.

The GS-D200 incorporates a thermal protection that switches off the power stages when the junction temperature of active components reaches 150 °C.

To keep the power dissipation to a minimum, two level supply voltages must be applied to the module : 5 V for logic functions and V_S from 10 to 46 V for power section.

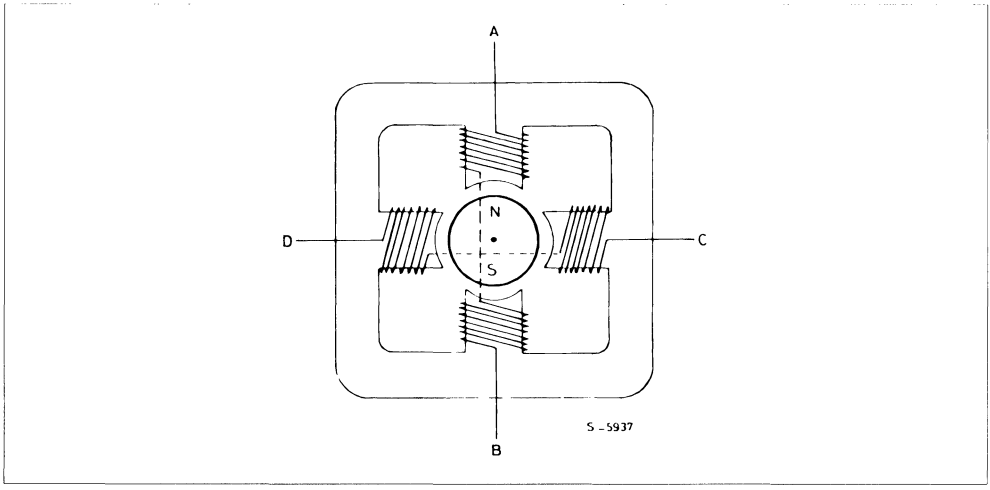
A. BIPOLAR STEPPER MOTOR BASICS

Simplified to the bare essentials, a bipolar permanent magnet motor consists of a rotating-permanent magnet surrounded by stator poles carrying the windings (fig. 1).

Bidirectional drive current is imposed on windings A-B and C-D and the motor is stepped by commutating the voltage applied to the windings in sequence.

For a motor of this type there are three possible drive sequences.

Figure 1 : Simplified Bipolar Two Phase Motor.



A. 1. ONE-PHASE-ON OR WAVE DRIVE

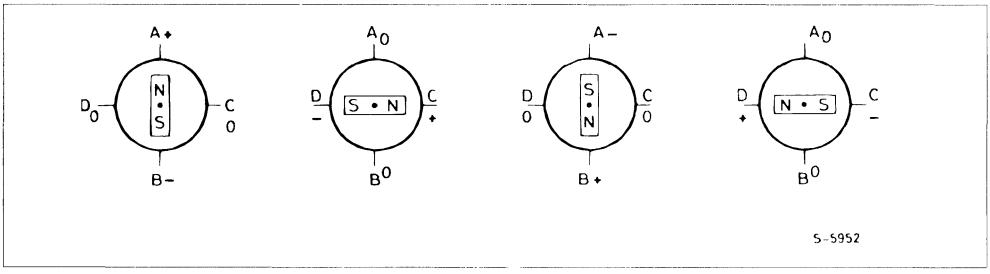
Only one winding is energized at any given time according to the sequence :

AB - CD - BA - DC

(BA means that the current is flowing from B to A).

Fig. 2 shows the sequence for a clockwise rotation and the corresponding rotor position.

Figure 2 : One-phase-on (wave mode) drive.



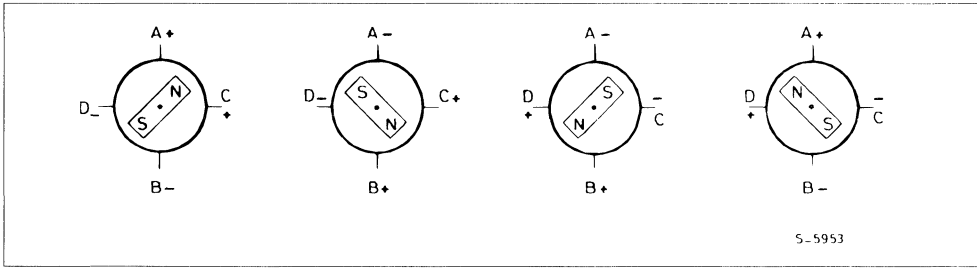
A. 2. TWO-PHASE-ON OR NORMAL DRIVE

This mode gives the highest torque since two windings are energized at any given time according to the sequence (for clockwise rotation).

AB & CD ; CD & BA ; BA & DC ; DC & AB

Fig. 3 shows the sequence and the corresponding position of the rotor.

Figure 3 : Two-phase-on (normal mode) drive.



A. 3. HALF STEP DRIVE

This sequence halves the effective step angle of the motor but gives a less regular torque being one winding or two windings alternatively energized. Eight steps are required for a complete revolution of the rotor.

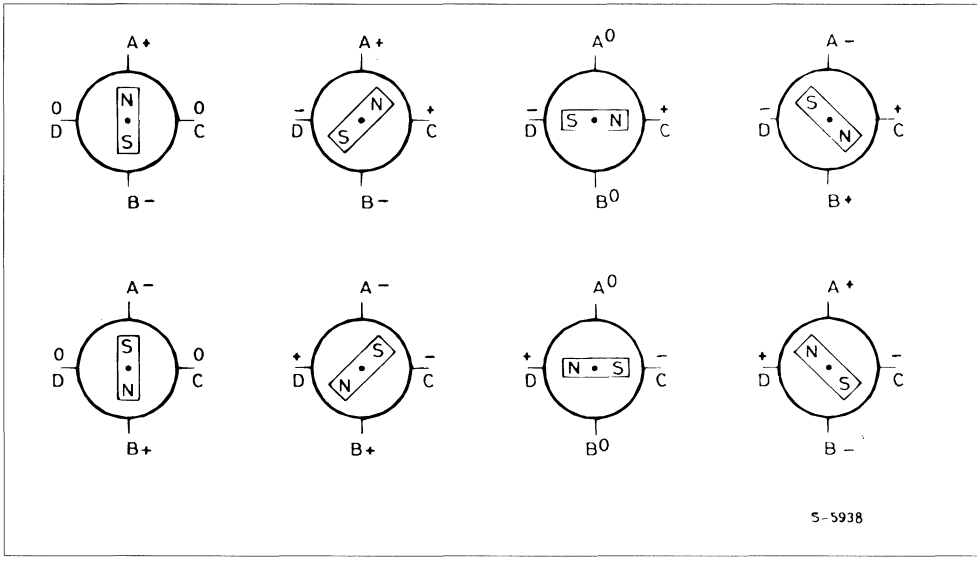
The sequence is :

AB ; AB & CD ; CD ; CD & BA ; BA ; BA & DC ; DC ; DC & AB

as shown in fig. 4.

By the configurations of fig. 2, 3, 4 the motor would have a step angle of 90 ° (or 45 ° in half step). Real motors have multiple poles pairs to reduce the step angle to a few degrees but the number of windings (two) and the drive sequence are unchanged.

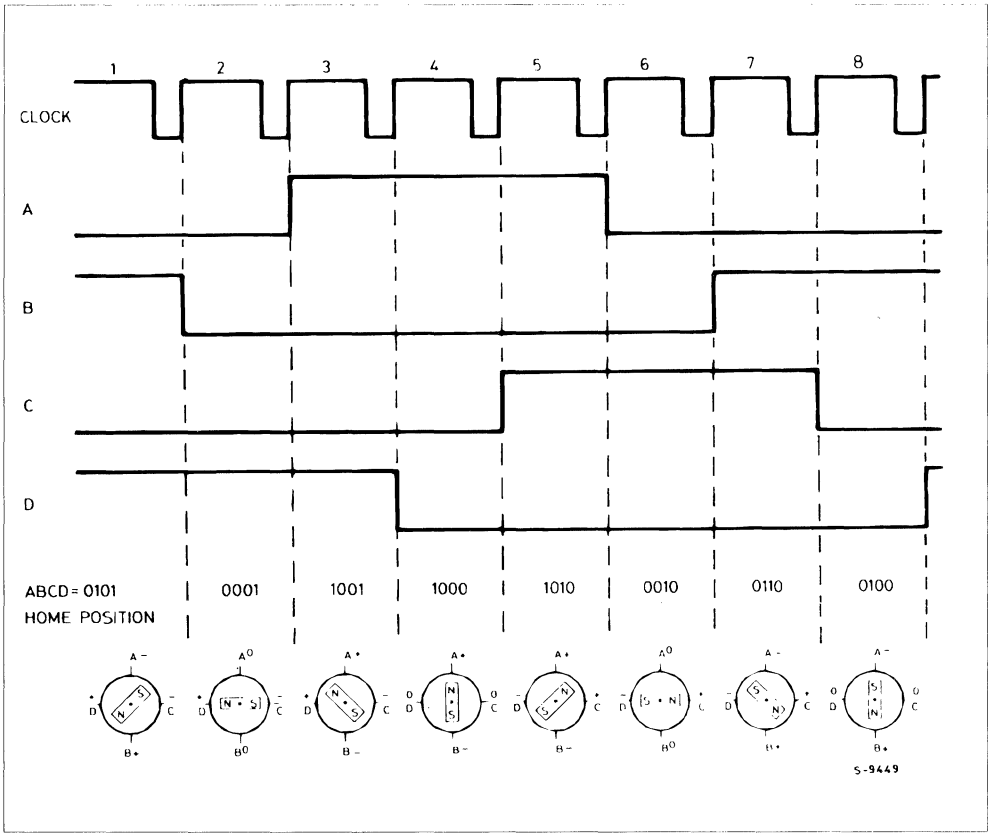
Figure 4 : Half Step Sequence.



B. PHASE SEQUENCE GENERATION INSIDE THE GS-D200

The GS-D200 contains a three bit counter plus some combinational logic which generate suitable phase sequences for half step, wave and normal full step drive. This 3 bit counter generates a basic eight-step Gray code master sequence as shown in fig. 5. To select this sequence, that corresponds to half step mode, the HALF/FULL input (pin 4) must be kept high or left open.

Figure 5 : The Eight Step Master Sequence Corresponding to Half Step Mode.



The full step mode (normal and wave drive) are both obtained from the eight step master sequence by skipping alternate states. This is achieved by forcing the step clock to bypass the first stage of the 3 bit counter. The least significant bit of this counter is not affected and therefore the generated sequence depends on the state of the counter when full step mode is selected by forcing pin 4 (HALF/FULL) low.

If full step is selected when the counter is at any odd-numbered state, the two-phase-on (normal mode) is implemented (see fig. 6).

On the contrary, if the full mode is selected when the counter is at an even-numbered state, the one-phase-on (wave drive) is implemented (see fig. 7).

Figure 6 : Two-phase-on (normal mode) drive.

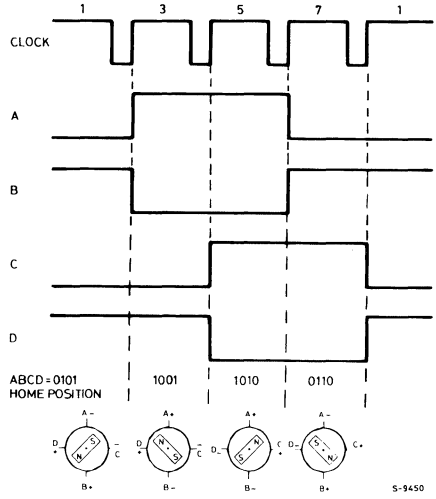
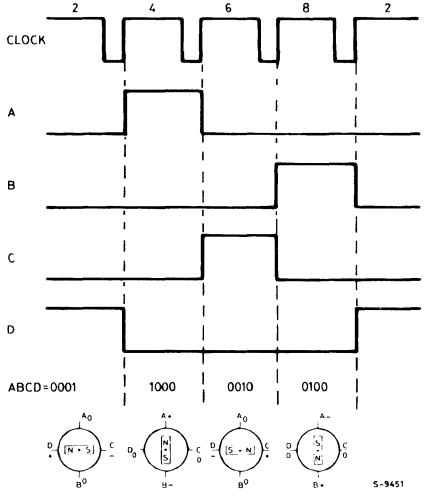


Figure 7 : One-phase-on (wave mode) drive.



C. RESET, ENABLE AND HOME SIGNALS

The $\overline{\text{RESET}}$ is an asynchronous reset input which restores the module to the home position (state 1 : ABCD = 0101). Reset is active when low.

The $\overline{\text{HOME}}$ output signals this condition and it is intended to be ANDed with the output of a mechanical home position sensor.

The ENABLE input is used to start up the module after the system initialization. ENABLE is active when high or open.

D. MOTOR CURRENT REGULATION

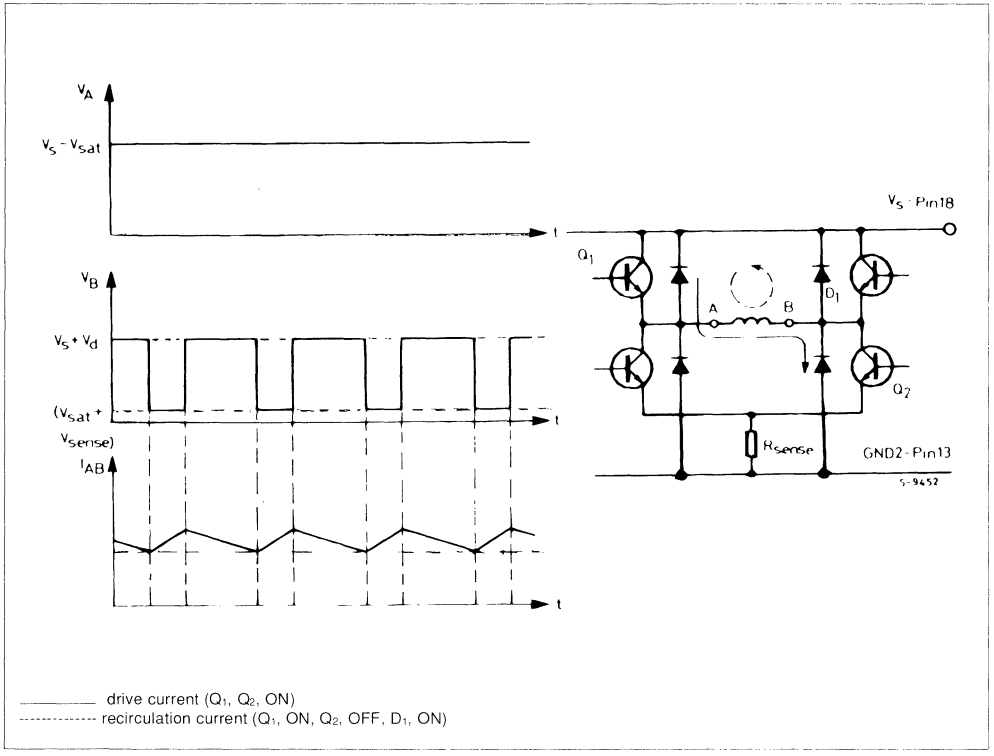
The two bipolar winding currents are controlled by two internal choppers in a PWM mode to obtain good speed and torque characteristics.

An internal oscillator supplies pulses at the chopper frequency to both choppers.

When the outputs are enabled, the current through the windings raises until a peak value set by I_0SET and R_{sense} (see the equivalent block diagram) is reached. At this moment the outputs are disabled and the current decays until the next oscillator pulse arrives.

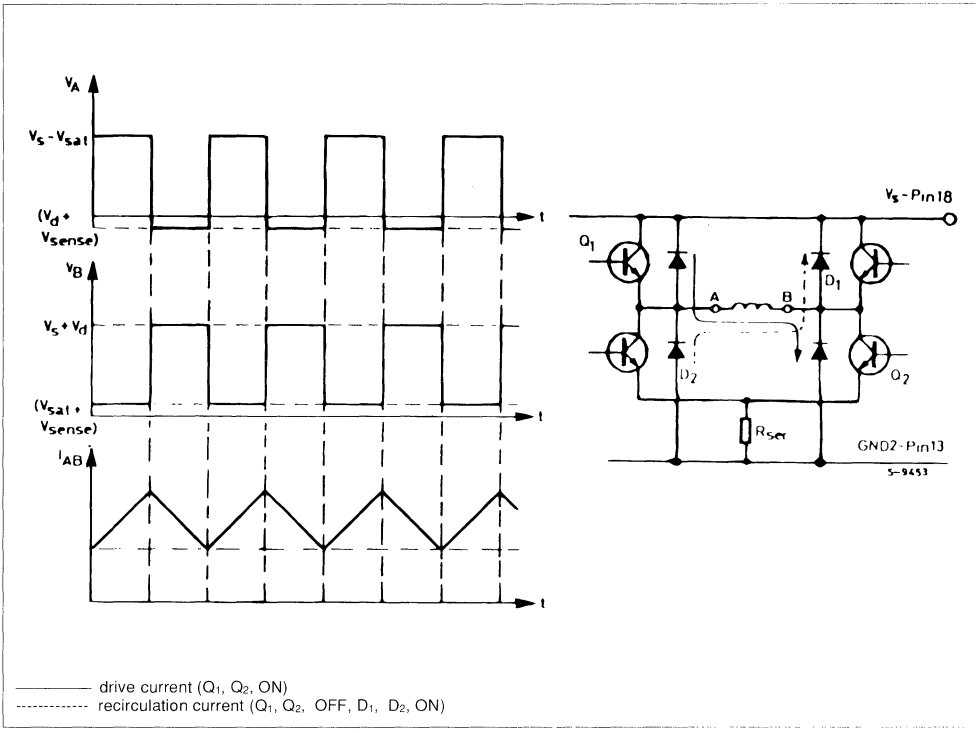
The decay time of the current can be selected by the CONTROL input (pin 10). If the CONTROL input is kept high or open the decay is slow, as shown in fig. 8, where the equivalent power stage of GS-D200, the voltages on A and B are shown as well as the current waveform on winding AB.

Figure 8 : Chopper Control with Slow Decay.



When the CONTROL input is forced low, the decay is fast as shown in fig. 9.

Figure 9 : Chopper Control with Fast Decay.



The CONTROL input is provided on GS-D200 to allow maximum flexibility in application.

If the GS-D200 must drive a large motor that does not store much energy in the windings, the chopper frequency must be decreased : this is easily obtained by connecting an external capacitor between OSC pin and GND1.

In these conditions a fast decay (CONTROL LOW) would impose a low average current and the torque could be inadequate. By selecting CONTROL HIGH, the average current is increased thanks to the slow decay

E. MODULE PROGRAMMING

When no external component is used, the GS-D200 is set at the following conditions :

$I_{outpeak} \cong 1$ A

f_c chopper frequency $\cong$ 17 KHz

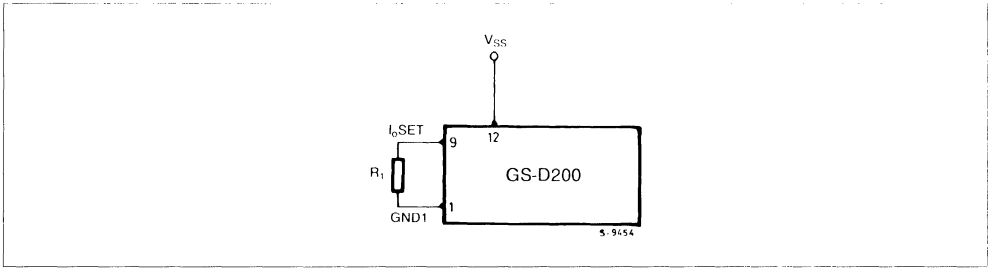
By addition of inexpensive passive components the working conditions can be modified as follows.

E.1. OUTPUT CURRENT PROGRAMMING

The output peak current (initially set at 1 A) can be re-programmed by addition of an external resistor.

If a lower peak current is desired, a resistor R1 must be connected between I_oSET and GND1 as shown in fig. 10.

Figure 10 : Peak Current Reduction.



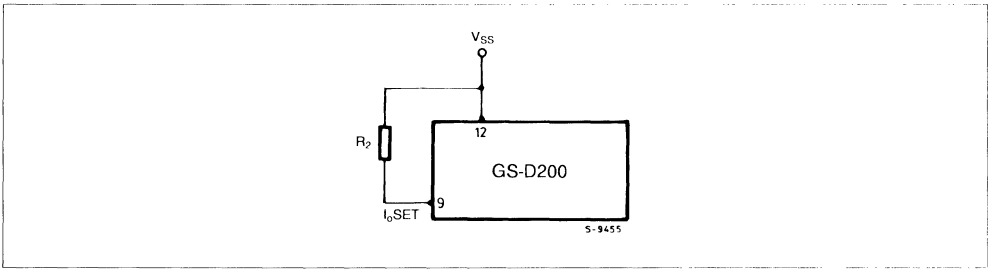
The value of output current, for V_{SS} = 5 V, is related to the value of R1 by

$$I_{out} = \frac{11.2}{11.2 + \frac{12}{R1}} \text{ A where R1 is in K}\Omega$$

For example, for R1 = 1 KΩ $I_{out} \cong 0.5$ A.

If a higher peak current is needed, a resistor R2 must be connected between I_{oSET} and V_{SS} as shown in fig. 11.

Figure 11 : Peak Current Increase.



The output current, for V_{SS} = 5 V, is related to the value of R2 by

$$I_{out} = \frac{120 + 12 \bullet R2}{12 + 11.2 \bullet R2} \text{ A where R2 is in K}\Omega$$

For example, for R2 = 24 KΩ $I_{out} \cong 1.45$ A

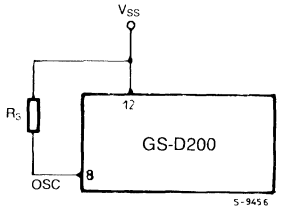
Minimum value of R2 is 10 kΩ. This current programmability can be used in half step sequence to increase the current when only one phase is on : a more regulator torque is so obtained.

E.2. CHOPPER FREQUENCY PROGRAMMING

The chopper frequency is internally set at about 17 KHz. This frequency can be changed by addition of external components as follows.

To increase the chopper frequency a resistor R3 must be connected between OSC pin and V_{SS} as shown in fig. 12.

Figure 12 : Chopper Frequency Increase.



The new chopper frequency is given by :

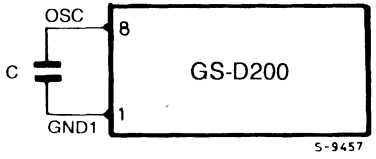
$f_C = 17\ (1 + \frac{18}{R3})$ KHz where R3 is in KΩ

For example, if V_{SS} = 5 V and R3 = 18 KΩ

$f_C \cong 34$ KHz

To decrease the chopper frequency a capacitor C must be connected between OSC pin and GND1 as shown in fig. 13.

Figure 13 : Chopper Frequency Decrease.



The new chopper frequency is given by :

$$f_C = \frac{80.5}{4.7 + C}$$ KHz where C is in nF

For example, if V_{SS} = 5 V and C = 4.7 nF, $f_C \cong 8.5$ KHz.

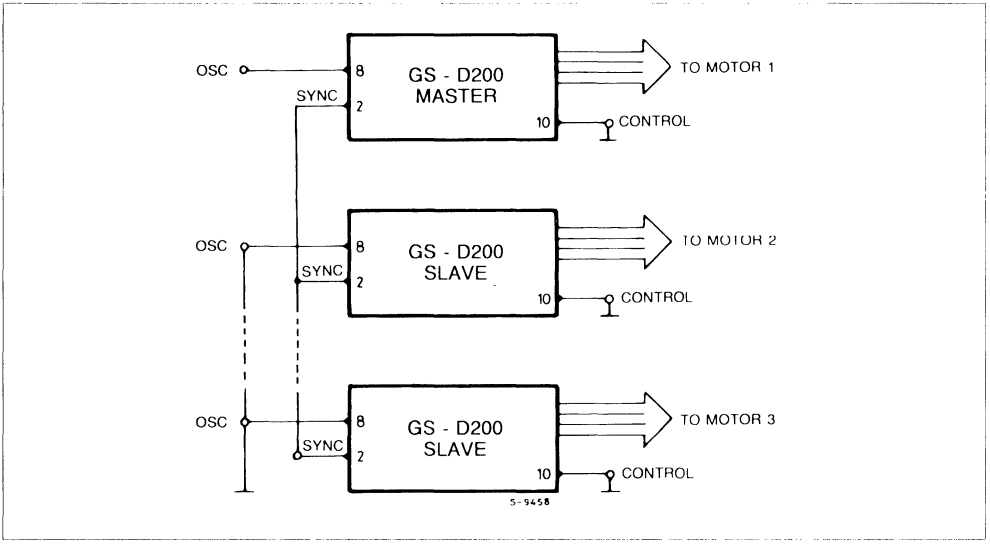
F. MULTI MODULES APPLICATION

In complex systems, many motors must be controlled and driven. In such a case more than one GS-D200 must be used.

To avoid chopper frequencies noise and beats, all the GS-D200 should be synchronized.

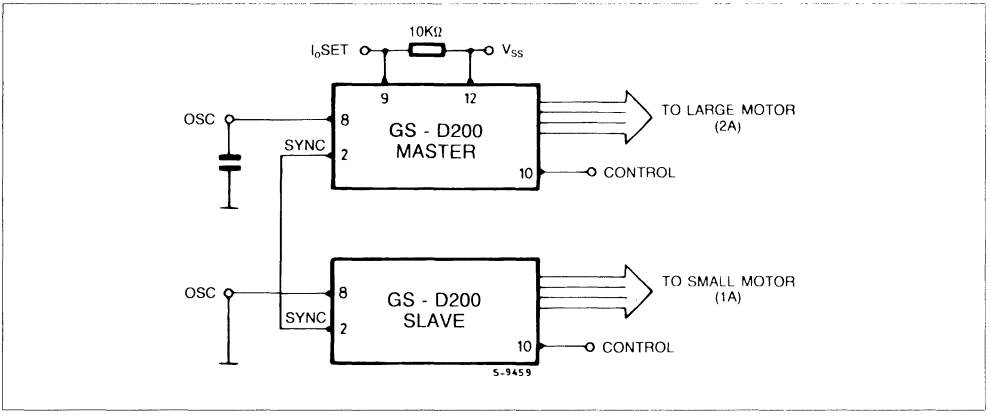
If all the motors are relatively small, the fast decay may be used, the chopper frequency does not need any adjustement and fig. 14 shows how to synchronize several modules.

Figure 14 : Multimotor Sybchronization. Small Motor and Fast Current Decay.



When at least one motor is relatively large a lower chopper frequency and a slow decay may be required. In such a case the overall system chopper frequency is determined by the largest motor in the system as shown in fig. 15.

Figure 15 : Multimotor Synchronization. Large and Small Motor. Slow Current Decay.



G.THERMAL OPERATING CONDITIONS

In many cases the GS-D200 module does not require any additional cooling because the dimensions and the shape of the metal box are studied to offer the minimum possible thermal resistance case-to-ambient for a given volume.

It should be remembered that the GS-D200 module is a power device and, depending on ambient temperature, an additional heath-sink or forced ventilation or both may be required to keep the unit within safe temperature range. ($T_{case_{max}}$ < 85 °C during operation).

The concept of maximum operating ambient temperature is totally meaningless when dealing with power components because the maximum operating

ambient temperature depends on how a power device is used.

What can be unambiguously defined is the case temperature of the GS-D200 module.

To calculate the maximum case temperature of the module in a particular applicative environment the designer must know the following data :

- Input voltage
- Motor phase current
- Motor phase resistance
- Maximum ambient temperature

From these data it is easy to determine whether an additional heath-sink is required or not, and the relevant size i.e. the thermal resistance.

The step by step calculation is shown for the following example :

V_{in} = 40 V, I_{phase} = 1 A, Rph Phase resistance = 10 Ω, Max. T_{amb} = 50 °C

G1. Calculate the power dissipated from the indexer logic and the level shifter (see electrical characteristics) :

$$P_{logic} = (5\ V\ .\ 60\ mA) + (40\ V\ .\ 20\ mA) = 1.1\ W$$

G2. Calculate the average voltage across the winding resistance :

$$V_{out} = (Rph\ .\ I_{out}) = 10\ \Omega\ .\ 1\ A = 10\ V$$

G3. Calculate the required ON duty cycle (D.C.) of the output stage to obtain the average voltage (this D.C. is automatically adjusted by the GS-D200) :

$$D.C. = \frac{V_{out}}{V_{in}} = \frac{10}{40} = 0.25$$

G4. Calculate the power dissipation of the GS-D200 output power stage. The power dissipation depends on two main factors :

- the selected operating mode (FAST or SLOW DECAY)
- the selected drive sequence (WAVE, NORMAL, HALF STEP)

G4.1 FAST DECAY. For this mode of operation, the internal voltage drop is $Vsat_{source}$ + $Vsat_{sink}$ during the ON period i.e. for 25 % of the time.

During the recirculation period (75 % of the time), the current recirculates on two internal diodes that have a voltage drop V_d = 1 V, and the internal sense resistor (0.5 Ω). For this example, by assuming maximum values for conservative calculations, the power dissipation during one cycle is :

$P_{pw} = 1.1 \bullet [2\ V_{sat} \bullet Iph \bullet DC + 2\ V_d \bullet I_{ph} \bullet (1 - DC) + 0.5 \bullet I_{ph}]$

$P_{pw} = 1.1 \bullet [2 \bullet 1.8 \bullet 1 \bullet 0.25 + 2 \bullet 1 \bullet 1 \bullet 0.75 + 0.5 \bullet 1]$

$P_{pw} = 1.1 \bullet [0.9 + 1.5 + 0.5] = 3.19\ W$

The factor 1.1 takes into account the power dissipation during the switching transient.

G4.2 SLOW DECAY. The power dissipation during the ON period is the same. The RECIRCULATION is made internally through a power transistor ($Vsat_{sink}$) and a diode. The power dissipation is, therefore :

$P_{pw} = 1.1 \bullet [2\ V_{sat} \bullet I_{ph} \bullet DC + (V_{sat} + V_d) \bullet I_{ph} \bullet (1\text{-}DC)]$

$P_{pw} = 1.1 \bullet [2 \bullet 1.8 \bullet 1 \bullet 0.25 + (1.8 + 1) \bullet 1 \bullet 0.75]$

$P_{pw} = 1.1 \bullet [0.9 + 2.1] = 3.3\ W$

G4.3 WAVE MODE. When operating in this mode the power dissipation is given by values of 4.1 or 4.2 paragraphes, because one phase is energized at any given time.

G4.4 NORMAL MODE. At any given time, two windings are always energized. The power dissipation of the power output stage is therefore multiplied by a factor 2.

G4.5 HALF STEP. The power sequence, one phase ON, two phase ON forces the power dissipation to be 1.5 times higher than in WAVE MODE when the motor is running. In stall condition the worst case for power dissipation is with two phase ON i.e. a power dissipation as in NORMAL MODE.

The following table summarizes the power dissipations of the output power stage of the GS-D200 when running for this example :

	Wave	Normal	Half Step
Fast Decay	3.19 W	6.38 W	6.38 W
Slow Decay	3.30 W	6.60 W	6.60 W

G5. Calculate the total power dissipation for the GS-D200 :

$$P_{tot} = P_{logic} + P_{pw}$$

In this example, for slow decay and normal mode

$$P_{tot} = 1.1 + 6.6 = 7.7\ W$$

G6. The case temperature can now be calculated :

$T_{case} = Tamb + (P_{tot} \bullet R_{th}) = 55 + (7.7 \bullet 5) = 93.5\ °C$

G7. If the calculated case temperature exceeds the maximum allowed case temperature, as in this example, an external heat-sink is required and the thermal resistance can be calculated according to :

$$Rth_{tot} = \frac{T_{cmax} - Tamb}{P_{tot}} = \frac{85 - 55}{7.7} = 3.9\ °C/W$$

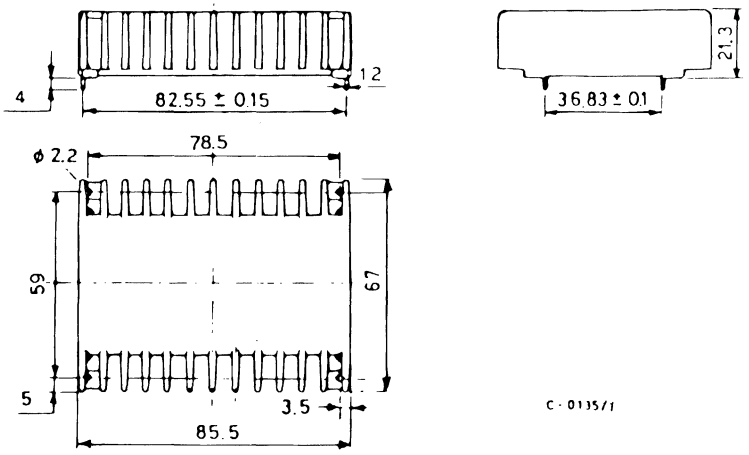
and then

$$Rth_{hs} = \frac{Rth - Rth_{tot}}{Rth - Rth_{tot}} = \frac{5 \bullet 3.9}{5 - 3.9} = 17.7\ °C/W$$

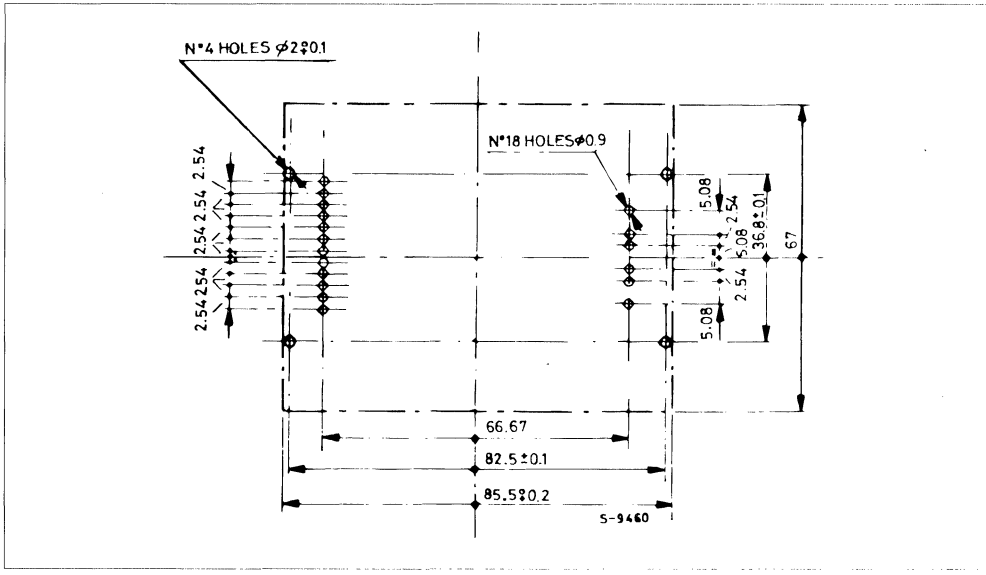
The following table gives the thermal resistance of some commercially available heath-sinks that fit on the GS-D200 module.

Manufacturer	Part Number	R_{th} (°C/W)	Mounting
Thermalloy	6177	3	Horizontal
Thermalloy	6152	4	Vertical
Thermalloy	6111	10	Vertical
Fischer	SK18	3	Vertical
Assman	V5440	4	Vertical
Assman	V5382	4	Horizontal

MECHANICAL DATA (dimensions in mm)



MOTHER BOARD LAYOUT

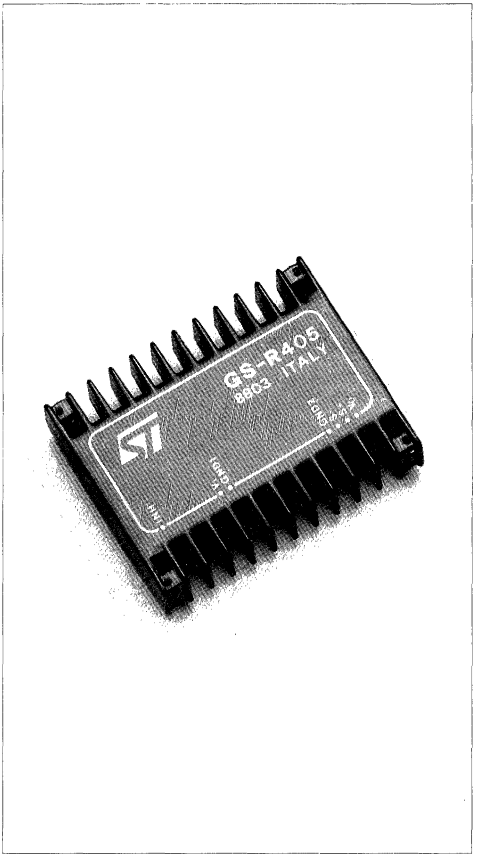


SGS-THOMSON MICROELECTRONICS

GS-R400 FAMILY

140W SWITCHING VOLTAGE REGULATOR MODULES

- MTBF IN EXCESS OF 200.000 HOURS
- NO EXTERNAL COMPONENTS REQUIRED
- PC CARD OR CHASSIS MOUNTABLE
- HIGH OUTPUT CURRENT (4 A)
- HIGH INPUT VOLTAGE (48 V)
- FIXED OR ADJUSTABLE OUTPUT VOLTAGE
- HIGH EFFICIENCY (UP TO 90%)
- SOFT START
- REMOTE INHIBIT/ENABLE
- REMOTE OUTPUT VOLTAGE SENSE
- RESET OUTPUT (GS–R405S ONLY)
- NON-LATCHING SHORT CIRCUIT PROTECTION
- THERMAL PROTECTION
- CROW BAR PROTECTION FOR THE LOAD



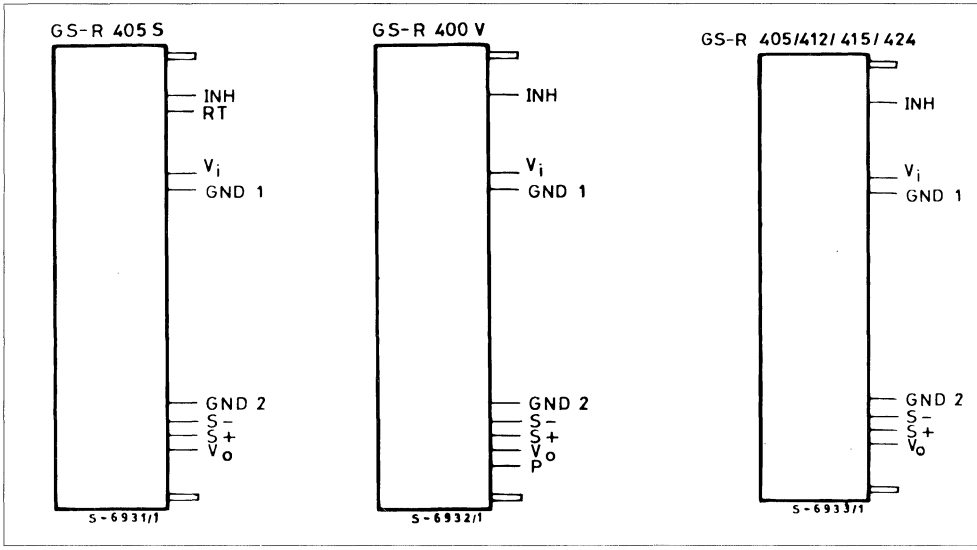
DESCRIPTION

The GS–R400 series is a complete family of HIGH CURRENT HIGH VOLTAGE SWITCHING VOLTAGE REGULATORS available in several output voltages from 5.1 to 40 V.
These step down regulators shielded for EMI, can provide local on-card regulation, or be used in central power supply systems, in both professional and industrial applications.

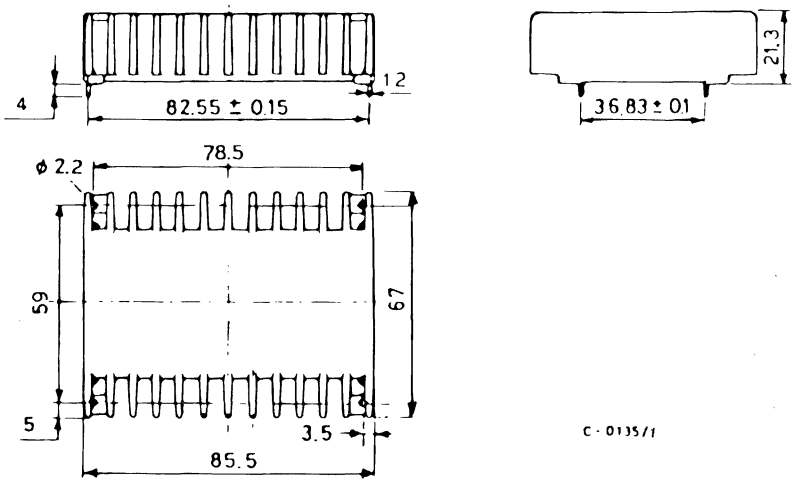
PRODUCTS FAMILY

Order Number	Output Voltage	Reset Output
GS-R405S	5.1 V	Yes
GS-R405	5.1 V	—
GS-R412	12 V	—
GS-R415	15 V	—
GS-R424	24 V	—
GS-R400V	Adjustable 5.1 to 40 V	—

CONNECTION DIAGRAM (side view)



MECHANICAL DATA (dimensions in mm)



PIN FUNCTIONS

Symbol	Pin	Function
INH	- Inhibit	TTL compatible input. A logic high level signal applied to this pin disables the module. To be connected to GND_2 when not used.
RT	- Reset Output	Available on GS-R405S only. Reset voltage is high (5.1 V) when output voltage reaches nominal value (5.1 V) and it is generated with a fixed 100 ms delay.
V_i	- Input Voltage	Unregulated DC voltage input. Maximum voltage must not exceed 48 V. Recommended maximum operating voltage is 46 V.
GND_1	- Ground	Common ground for input voltage.
GND_2	- Ground	Common ground of high current path.
S^-	- Sensing Negative	For connection to remote load, this pin senses the actual ground of the load itself. To be connected to GND_2 when not used. This pin is connected to case.
S+	- Sensing Positive	For connection to remote loads this pin allows voltage sensing on the load itself.To be connected to V_0 when not used.
V_o	- Output Voltage	Regulated and stabilized DC voltage is available on this pin. Max output current is 4 A. The device is protected against short circuit of this pin to ground or to supply.
P	- Output Voltage Programming	Available on GS-R400V only. A variable resistor (18 KΩ max) connected between this pin and S^- adjusts the output voltage.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC input voltage	48	V
I_{RT}	Reset output sink current	20	mA
V_{INH}	Inhibit voltage	15	V
T_{stg}	Storage temperature range	– 40 to + 105	°C
T_{cop}	Operating case temperature range	– 20 to + 85	°C

Recommended maximum operating input voltage is 46V.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Type			GS-R 405 S			GS-R 405			GS-R 4012 V			Unit
Symbol	Parameter	Test Condit.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage	V_i = V_O + 8V, I_O = 1A	5	5.1	5.2	5	5.1	5.2	11.5	12	12.5	V
V_O	Temperature Stability	V_i = V_O + 8V, I_O = 1A		0.2			0.2			0.5		$\frac{mV}{°C}$
V_i	Input Voltage	I_O = 1A	8		46	8		46	15		46	V
I_O	Output Current	V_i = V_O + 8V	0.2		4	0.2		4	0.2		4	A
I_{OL}	Current Limit	V_i = V_O + 8V		5	8		5	8		5	8	A
I_{isc}	Average Input Current	Vi = 46V Output Shorted		0.1	0.2		0.1	0.2		0.1	0.2	A
f_s	Switching Frequency	I_O = 1A		100			100			100		KHz
η	Efficiency	V_i = V_O + 8V I_O = 1A		75			75			85		%
ΔV_O	Line Regulation	I_O = 1A V_i = V_O + 3V to 46V		2			2			2		mV/V
SVR	Supply Voltage Rejection	f = 100Hz I_O = 1A		4			4			6		mV/V
ΔV_O	Load Regulation	ΔI_O = 2A (1 to 3 A)		20			20			40		mV/A
V_r	Ripple Voltage	I_{out} = 2A		25			25			50		mV
t_{ss}	Soft Start Time	V_{in} = V_{out} + 10V		15			15			25		ms
V_{INHL}	Low Inhibit Voltage				0.8			0.8			0.8	V
V_{INHH}	High Inhibit Voltage		2.0		5.5	2.0		5.5	2.0		5.5	V
I_{INH}	Input Current High	V_{INH} = 5V			500			500			500	µA
t_{CB}	Crow Bar Delay Time			5			5			5		µS
V_{RH}	Reset High Level			5			–			–		V
V_{RL}	Reset Low Level	I_{RL} = 5mA I_{RL} = 15mA			0.2 0.4			–			–	V V
t_R	Reset Delay Time			100			–			–		ms
V_{SD}	Max Differential Sense Voltage	S^- – GND2 V_O – S^+			100			100			100	mV

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Type			GS-R 415			GS-R 424			GS-R 400 V			Unit
Symbol	Parameter	Test Condit.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output Voltage	$V_i = V_O + 8V$	14.3	15	15.6	23	24	25	5.1	–	40*	V
V_O	Temperature Stability	$V_i = V_O + 8V$, I_O = 1A		0.2			0.6			0.2/1.6		$\frac{mV}{°C}$
V_i	Input Voltage	I_O = 1A	18		46	27		46	8		46	V
I_O	Output Current	$V_i = V_O + 8V$	0.2		4	0.2		4	0.2		4*	A
I_{OL}	Current Limit	$V_i = V_O + 8V$		5	8		5	8		5	8	A
I_{isc}	Average Input Current	Vi = 46V Output Shorted		0.1	0.2		0.1	0.2		0.1	0.2	A
f_s	Switching Frequency	I_O = 1A		100			100			100		KHz
η	Efficiency	$V_i = V_O + 8V$ I_O = 1A		90			90			75/90		%
ΔV_O	Line Regulation	I_O = 1A $V_i = V_O + 3V$ to 46V		5			6			6		mV/V
SVR	Supply Voltage Rejection	f = 100Hz I_O = 1A		8			12			12		mV/V
ΔV_O	Load Regulation	ΔI_O = 2A (1 to 3A)		60			90			20/90		mV/A
V_r	Ripple Voltage	I_{out} = 2A		60			100			25/150		mV
t_{ss}	Soft Start Time	$V_{in} = V_{out} + 10V$		25			35			15/35		ms
V_{INHL}	Low Inhibit Voltage				0.8			0.8			0.8	V
V_{INHH}	High Inhibit Voltage		2.0		5.5	2.0		5.5	2.0		5.5	V
I_{INH}	Input Current High	V_{INH} = 5V			500			500			500	µA
t_{CB}	Crow Bar Delay Time			5			5			5		µS
V_{RH}	Reset High Level			–			–			–		V
V_{RL}	Reset Low Level				– –			– –			– –	V V
t_R	Reset Delay Time			–			–			–		ms
V_{SD}	Max Differential Sense Voltage	S^- – GND2 $V_O - S^+$			100			100			100	mV

* Maximum Output Current is guaranteed up to V_o = 36V and derated linearly to 3A at V_o = 40V.

MODULE OPERATION

The GSR400 series is a family of step down switching mode voltage regulators.

Unregulated DC input voltage must be higher than nominal output voltage by, at least, 3 V. Minimum input voltage is therefore 8 V for GS-R405S and GS-R405; maximum input voltage is 48 V for all types.

Output voltage is fixed or adjustable (GS-R400V). The maximum current delivered by the output pin is 4 A. A minimum output current of 200 mA is required for proper module operation. In no-load condition, the module still works, but the electrical characteristics are slightly modified vs. specifications.

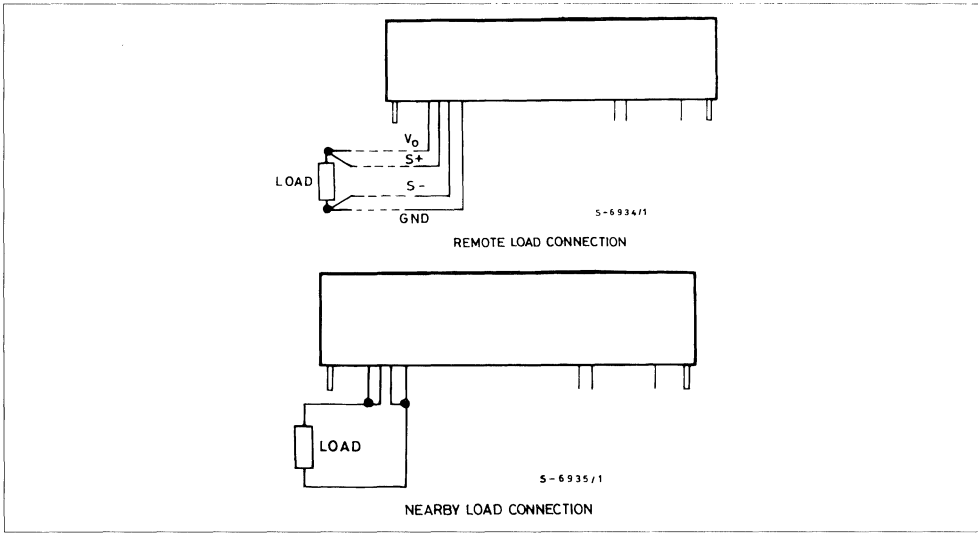
To prevent excessive over current at switch on, a soft start function is provided. Nominal output voltage is approached gradually in about 15 ms.

The module can be inhibited by a TTL, N MOS or C MOS compatible voltage applied to the INH pin. When this voltage is at high level, the module is switched off : if the inhibit signal goes from high to low level, the module restarts softly. Maximum DC voltage applicable to this pin is 15 V. When remote control (inhibit) of the module is not used, the INH pin must be connected to GND_2.

The remote load sensing is another feature provided in all the models.

This function is performed by two pins (S^+, S–) that can monitor the voltage directly across the load when this load is connected to the module by long wires : voltage drop on these wires is automatically compensated. Maximum drop compensation must not exceed 100mV. The case of the module is internally connected to S–. Therefore, the case must be always isolated from ground if the sensing function is used. The switching frequency of the module is 100 KHz. To prevent EMI, the module is contained in a metal box that provides shielding and heatsink.

Figure 1 : Module connection to remote or nearby loads.

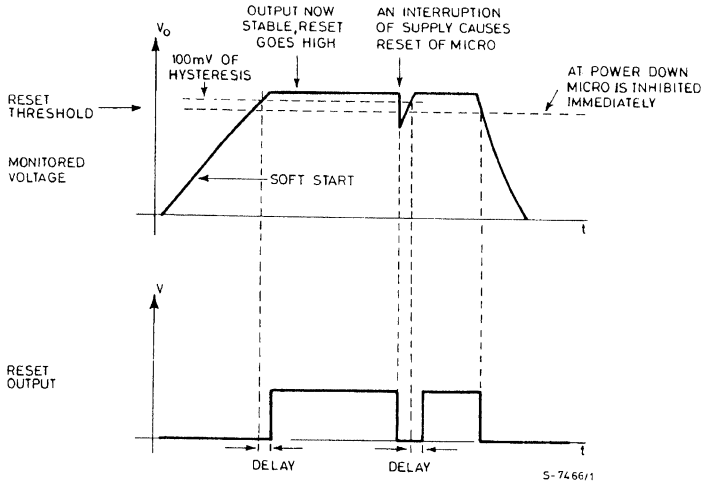


GS-R405S

The RESET output is provided on GS-R405S only as an auxiliary function to reset or inhibit microprocessors when the output voltage, at switch on and off, reaches a prefixed value of 4.9 to 5.1 V or when the output voltage, for any reason, drops below nominal value by more than 100 mV. In any case the minimum falling threshold value is 4.75 V or higher and the reset output voltage is generated with a fixed delay of 100 ms.

Time delay of the reset function also rejects wrong information caused by occasional spikes generated during switch on and off.

Figure 2 : Output voltages reset as a function of output voltage and time.



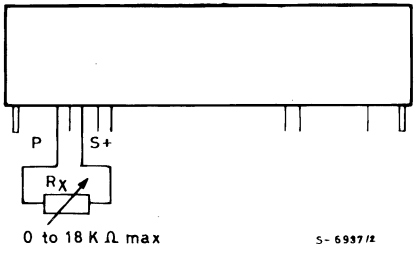
GS-R400V

The output voltage of this model can be adjusted in a range from 5.1 to 40 V by use of an external variable resistor as shown in Fig.3.
The variable resistor can be substituted by a fixed value Rx to obtain a fixed output voltage V_O according to the formula :

$$Rx = 2.67 \cdot \left(\frac{V_O}{5.1} - 1 \right) K\Omega$$

where V_O can vary from 5.1 to 40 V.

Figure 3 : Output voltage adjustment on GS-R400V.



MODULE PROTECTIONS

THERMAL PROTECTION

The module has inside a thermal protection. When ambient temperature reaches prohibitive values, so that internal junction temperature of active components reaches 150 °C, the module is switched off. Normal operation is restored when internal junction temperature falls below 130 °C : this large hysteresis allows an extremely low frequency intermittent operation (ON - OFF) caused by thermal overload.

SHORT CIRCUIT PROTECTION

The module is protected against occasional and permanent short circuits of the output pin to ground or against output current overloads.
When output current exceeds the maximum allowed value for safe operation, the output is automaticaly disabled. After a fixed time, the module starts again in a soft mode : if the overload is still present, the module switches off and the cycle is repeated until the overload condition is removed. The average overload current is limited to a safe value for the module itself. Input current during output short circuit is always lower than in regular operation.

LOAD PROTECTION

The module protects, by a crow bar circuit, the load connected to its output against overvoltages.
This circuit senses continuously the output voltage : if, for any reason,the output voltage of the module exceeds by + 20 % the nominal value (fixed or adjustable), the crow bar protection is activated and it short circuits the output pin to ground. This protection prevents also damages to module if output pin is wrongly connected to supply voltage.

THERMAL DATA

The thermal resistance module to ambient is about 5 °C/W. This means that if the internal power dissipation is 10 W, the temperature on the surface of the module is about 50°C over ambient temperature.

According to ambient temperature and/or to power dissipation, an additional heatsink may be required.

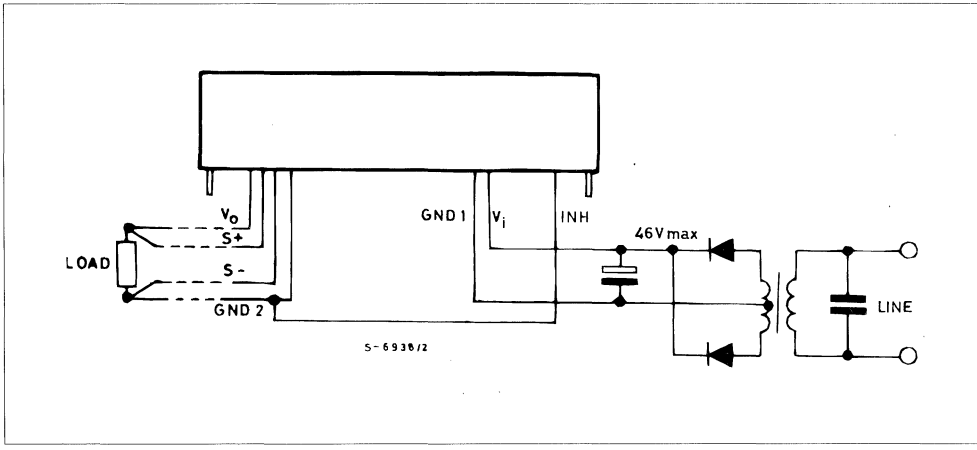
Four holes are provided on the metal box of the module to allow the mounting of this optional external heatsink.

It is recommended to keep the metal box temperature below 85 °C.

TYPICAL APPLICATIONS

The high input voltage range allows both cost saving on 50/60 Hz transformer when the module is supplied from the main and the possibility to supply the module with batteries that, according to their charge status, can show large spread on voltage.

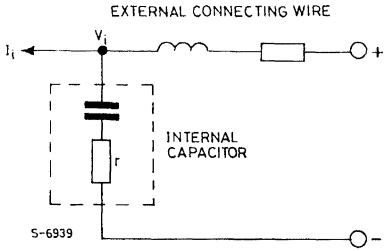
Figure 4 : A typical application of GS-R400 family.



TYPICAL APPLICATIONS (continued)

The module has, internally, an input filtering capacitor between pin V_I and GND_1. At the switching frequency therefore the equivalent input circuit is as shown in Fig. 5.

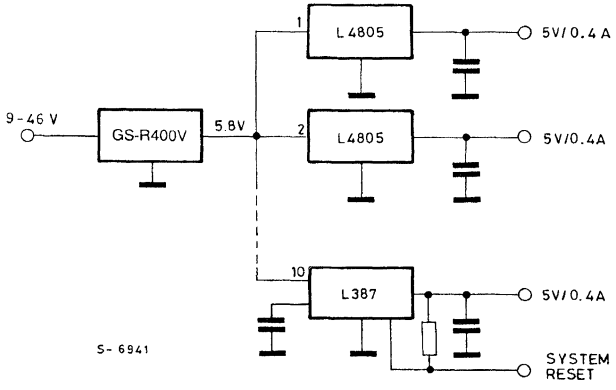
Figure 5 : Equivalent input circuit of GS-R400 voltage regulator.



Since I_i is a high frequency alternating current, the inductance associated to long input connecting wire can cause a voltage ripple on point V_I that produces a ripple current across internal capacitor and a power dissipation on r.

When very long connecting wires are used, the input capacitor may be damaged by this power dissipation. For this reason it is suggested to keep input connecting wires as short as possible.

Figure 6 : Preregulators for Distributed Supplies.



The fixed voltage regulators shown on Fig.6 are available from SGS-THOMSON Microelectronics. An over-all low power dissipation is achieved due to the high efficiency of the GS-R400V and inherent low voltage drop of fixed regulators. Up to 10 different points can be supplied, using L4805 or L387.

TYPICAL APPLICATIONS (continued)

Figure 7 : 24 V to 12 V Power Conversion for Trucks.

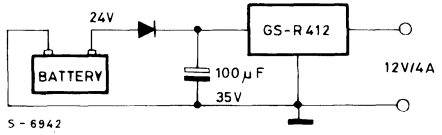


Figure 8 : Multiple output supply using preregulator.

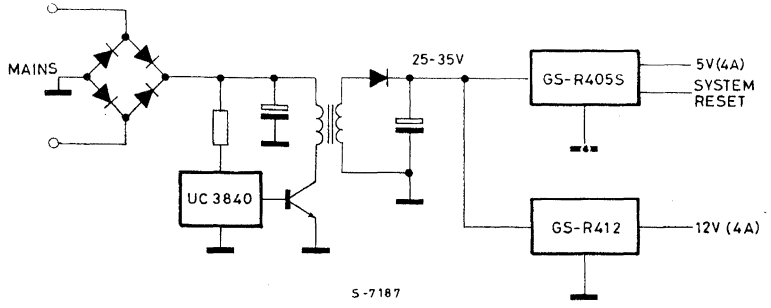
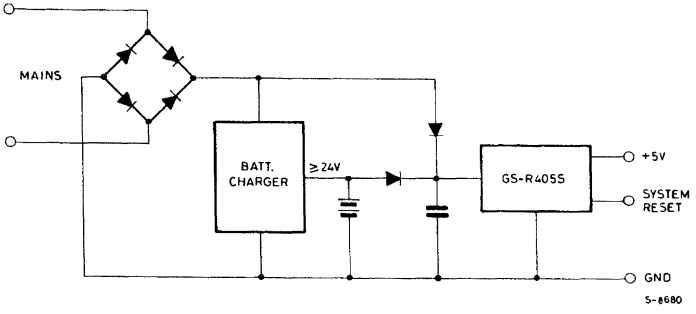
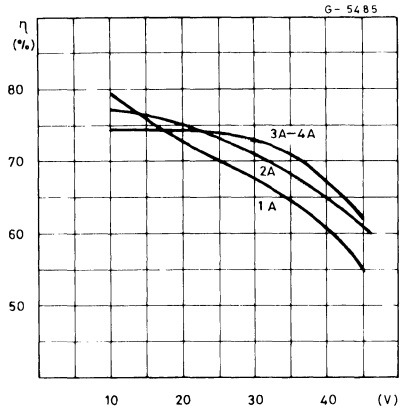


Figure 9 : Uninterruptable power supply.

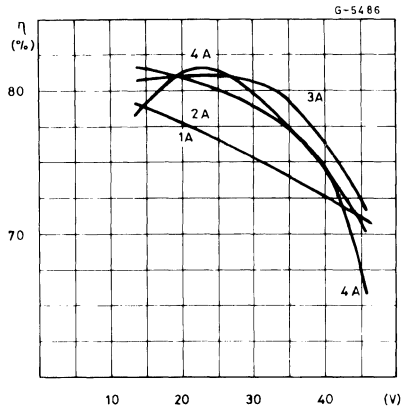


EFFICIENCY VS. INPUT VOLTAGE & OUTPUT CURRENT

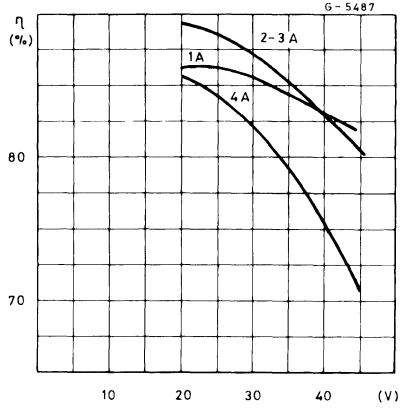
GS-R405



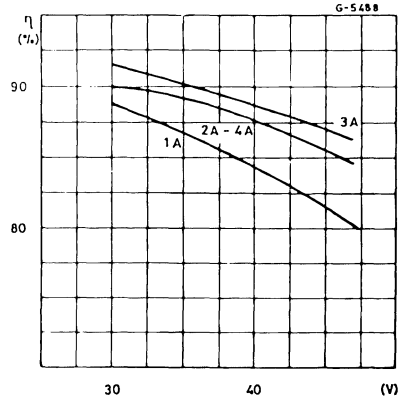
GS-R412



GS-R415

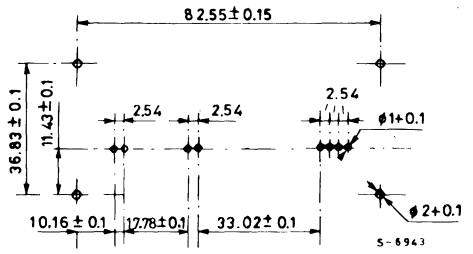


GS-R424

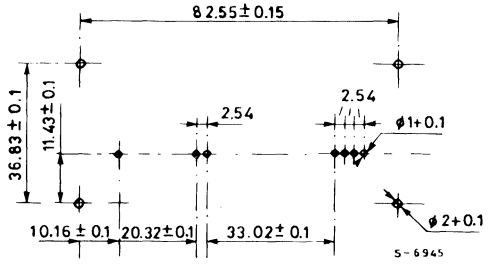


MOTHER BOARD LAYOUT

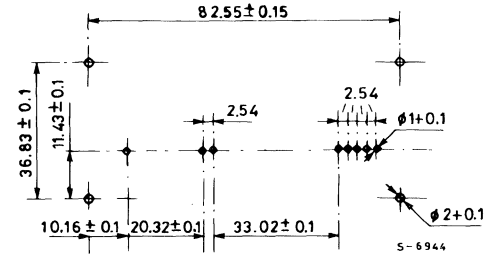
GS-R405S



GS-R405
GS-R412
GS-R415
GS-R424



GS-R400V



Printed Circuit Driling (Components side)

Required holes pattern to be drilled on the mother boards to allow correct mounting.

DESIGN HINTS

The hints provide a pratical guideline for the selection of the transformer, the rectifying diodes and the filtering capacitor of a power supply based on GS-R400 family.

Let's consider the application shown in the Figure 10. The rectifier circuit configurations suitable for medium to high current applications, are the Full Wave Center Tapped and the Full Wave Bridge. (See fig.11)

Both configurations offer the advantage of a smaller surge current in the winding of the transformer and the doubling of ripple frequency that allows the filtering capacitor reduction.

In the following we will consider the full wave bridge only, that allows the best transformed utilization.

The output power of the power supply is, respectively :

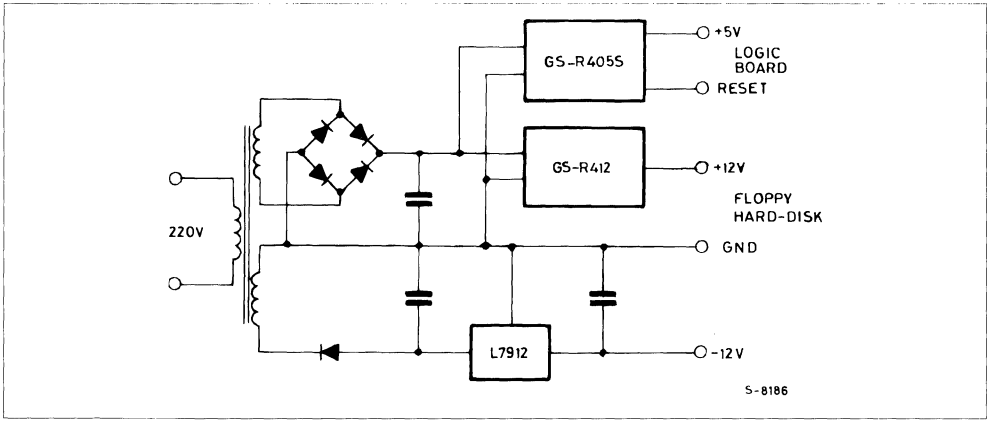
5 V · 4 A = 20 W for GS-R405S
12 V · 2.5 A = 30 W for GS-R412.

The total input power is, therefore

$$P_i = \frac{P_0}{Eff.} = \frac{20}{.75} + \frac{30}{.85} = 62W$$

The two values for efficiency are derived from GS-R electrical characteristics.

Figure 10 : Microcomputer supply using GS-R400.



The maximum input voltage to the module is set up to 40 V to work well below the Absolute Maximum Rating (48V).

$$V_i (pk) = 40 V$$

The minimum input voltage is set uo to 16 V to allow a minimum drop-out of 4 V on the GS-R412.

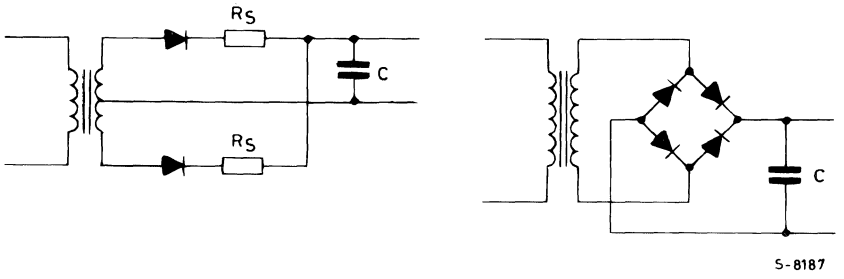
$$V_i (min) = 16 V$$

The nominal input voltage is set up at the middle of this range to allow a larger input ripple voltage and line voltage variations.

$$V_i (DC) = \frac{40 - 16}{2} + 16 = 28 V$$

DESIGN HINTS (continued)

Figure 11 : Rectifying circuits.



Let's assume a maximum 100 (120) Hz output ripple of the two regulators of 20 mVpp. Since the ripple rejection of the two modules is, at least 50 dB (316 times), the maximum allowed input ripple is

$$20\ mV \cdot 316 = 6.32\ V_{ripple(pp)}$$

Let's definite rf(in) as the ratio of RMS ripple to DC voltage

$$rf(in) = \frac{6.32}{2 \cdot \sqrt{2} \cdot 28} \cdot 100 = 8\ \%$$

The input current is calculated from the input power and voltage :

$$I_i = \frac{P_i}{V_i(DC)} = \frac{62W}{28\ V} = 2.2\ A$$

The equivalent load for the transformer + rectifier + capacitor is therefore

$$R_L = \frac{28V}{2.2A} = 12.73\ Ohm$$

$V_i(pk)$ must correspond to the nominal value of the mains plus the allowed variations. Let's assume that the AC voltage at the primary of the transformer may vary of $\pm 15\ \%$.
At nominal AC voltage the corresponding secondary maximum DC voltage is :

$$V_i(pk)nom = 40 - 15\ \% = 34\ V$$

Then we calculate

$$\frac{V_i(DC)}{V_i(pk)} = \frac{28V}{34V} = 0.82$$

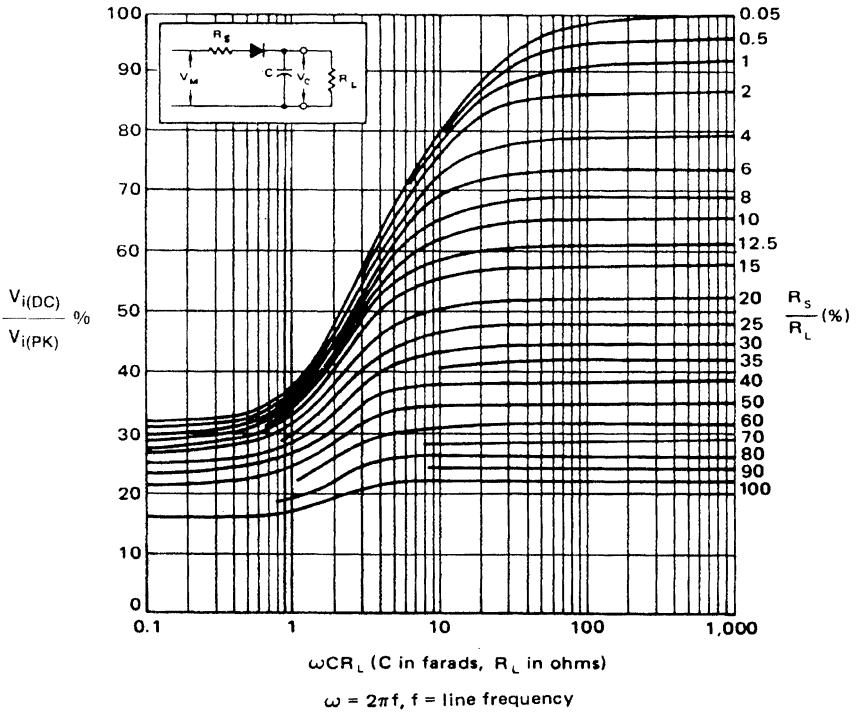
From the graph of fig. 12b we obtain,

$$\text{for } \frac{V_i(DC)}{V_i(pk)} = 0.82$$

$$\omega C R_L = 8 \text{ and } \frac{Rs}{R_L} = 4\%$$

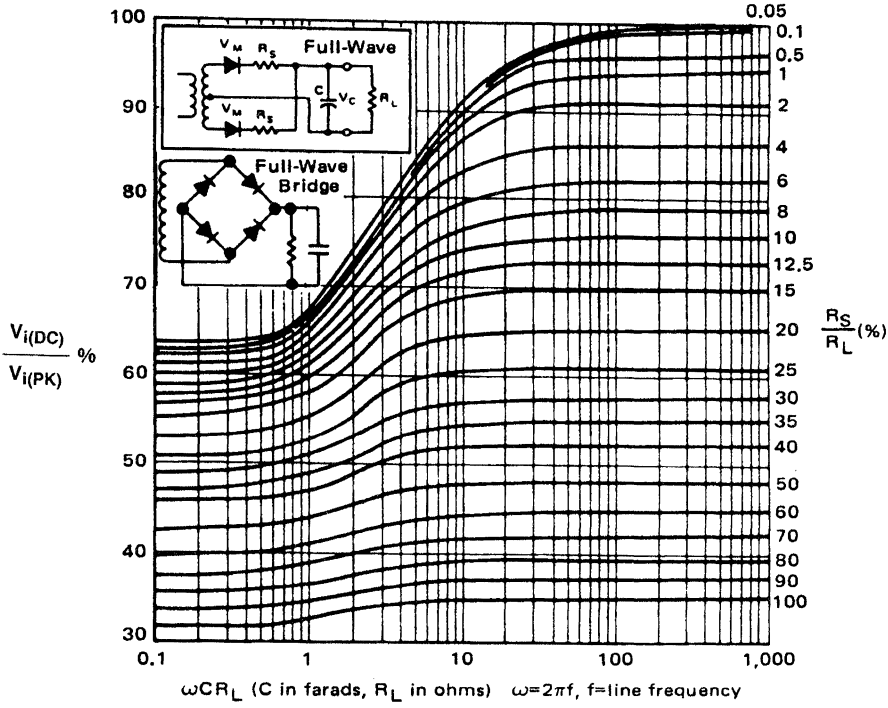
DESIGN HINTS (continued)

Figure 12a : Input Voltage (DC/pk) Ratio Half Wave.



DESIGN HINTS (continued)

Figure 12b : Input Voltage (DC/pk) Ratio Full Wave.



Therefore

$$C = \frac{8}{2\pi f \cdot R_L} = \frac{8}{6.28 \cdot 100 \cdot 12.73} = 1000\ \mu F$$

To take into account the spread of commercially available capacitors, this value is doubled : 2200 µF / 50 V.

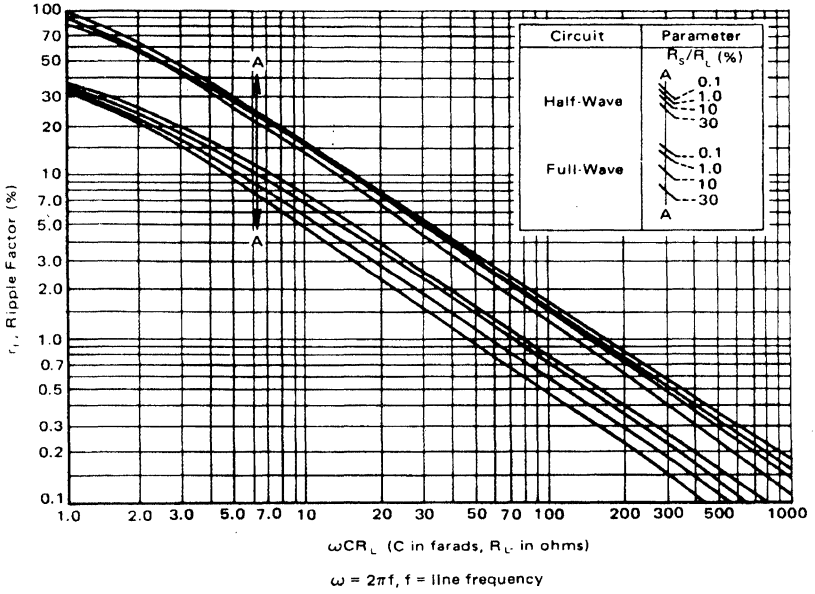
We procede now assuming that :

$$R_S = 4\ \%\ R_L = 0.04 \cdot 12.73 = 0.51\ \text{Ohm}$$

It represents the total series resistance of the transformer and the rectifying bridge.

DESIGN HINTS (continued)

Figure 13 : Ripple Voltage vs. Input Capacitance and R_S/R_L.



From the figure 13 for $\omega CR_L = 8$ and $R_S/R_L = 4$ % it results :

$$rf = 7.5\ \%$$

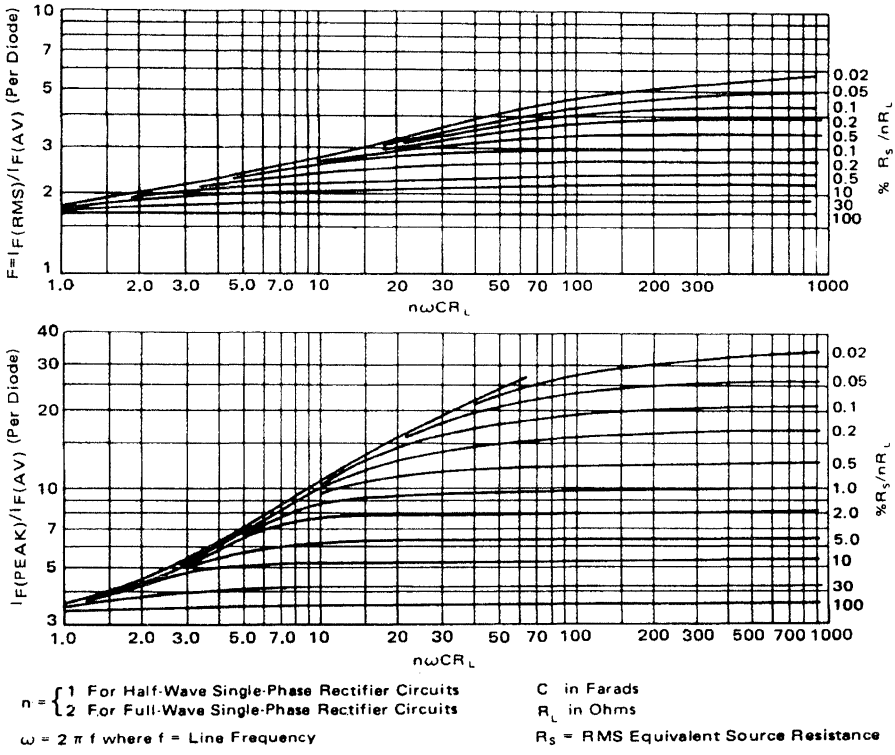
Therefore the peak to peak value of the resulting input ripple will be :

$$V_{ripple(pp)} = 2\sqrt{2} \cdot rf \cdot V_i(DC) = 5.9\ V_{pp}$$

This value is lower than the maximum allowed (6.32 V_{pp}).

DESIGN HINTS (continued)

Figure 14 : RMS/Average Peak/Average Diode Current relation.



n = { 1 For Half-Wave Single-Phase Rectifier Circuits
n = { 2 For Full-Wave Single-Phase Rectifier Circuits

ω = 2 π f where f = Line Frequency

C in Farads

R_L in Ohms

R_S = RMS Equivalent Source Resistance

The minimum input DC voltage will correspond to the minimum input AC voltage, i.e. the nominal value minus 15 %, therefore

$$V_i(DC)min = V_i(DC)nom - 15\%$$
$$= 28 - 15\% = 23.8\ V$$

The minimum peak voltage present at the input of the regulators will be the minimum DC voltage minus the peak of ripple voltage :

$$V_i(pk)min = 23.8 - \frac{5.9}{2} = 20.85V$$

well above the minimum allowed (16 V).

As shown on figure 14 for $2\omega CR_L = 16$ and $R_S/2R_L = 2\ \%$ we obtain :

$$\frac{If(RMS)}{If(Av)} = 2$$

Therefore :

$$Isec\ (RMS) = \frac{I_i(DC) \cdot 2}{\sqrt{2}}$$
$$= \frac{2.2 \cdot 2}{\sqrt{2}} = 3.12\ A\ (RMS)$$

DESIGN HINTS (continued)

The secondary voltage must be :

$$Vsec\ (RMS) = \frac{V_i(pk) + 1.4}{\sqrt{2}} = 25.1\ V\ (RMS)$$

where 1.4V takes into account the voltage drop on diodes.

Then the transformer rating is calculated :

$$VA = 25.1 \cdot 3.12 = 78.3\ VA$$

To select the rectifying bridge of diodes, the following considerations applies.

The forward average current is one half the total input DC current since the configuration is a bridge :

$$If(Av) = \frac{I_i(DC)}{2} = \frac{2.2}{2} = 1.1\ A$$

As shown on figure 13 for $2\omega CR_L = 2 \cdot 8 = 16$ and $R_S/2R_L = 1/2 \cdot 4\% = 2\%$ we get

$$\frac{If\ (pk)}{If\ (Av)} = 8 \quad \text{i.e. } If\ (pk) = 8 \cdot If\ (Av) = 8.8\ A$$

and

$$\frac{If\ (RMS)}{if\ (Avg)} = 2 \quad \text{i.e. } If\ (RMS) = 2 \cdot If\ (Av) = 2.2\ A$$

The surge current occurs at the maximum secondary voltage

$$Isurge = \frac{V_i\ (pk)}{R_S} = \frac{40}{0.51} = 78.4\ A$$

HOW TO CHOOSE THE HEAT SINK

Sometimes the GS-R400 requires an external heat sink depending both operating temperature conditions and power.
Before entering into calculation details, some basic concepts will be explained to better understand the problem.

The thermal resistance between two points is represented by their temperature difference in front of a specified dissipated power, and it is expressed in Degree Centigrade per Watt.

For GS-R400 the thermal resistance case to ambient is 5 °C/W. This means that an internal power dissipation of 1 Watt will bring the case temperature at 5 °C above the ambient temperature.

The maximum allowed case temperature of the module is 85 °C.
Let's suppose to have a GS-R412 that delivers a load current of 4 A at an ambient temperature of 40 °C.

The dissipated power in this operating condition is about 13W, and the case temperature of the module will be :

$$T_{case} = T_{amb} + Pd \cdot Rth = 40 + 13 \cdot 5 = 105\ °C$$

This value exceeds the maximum allowed temperature and an external heat sink must be added. To this purpose four holes are provided on top of the case.

To calculate this heat sink, let's first determine what the total thermal resistance should be.

$$Rth = \frac{T_{case(max)} - T_{amb}}{Pd} = \frac{85 - 40}{13} = 3.46°C/W$$

This value is the resulting value of the parallel connection of the GS-R thermal resistance and of the additional heatsink thermal resistance.

$$\frac{R_{th}(GSR) \cdot R_{th}(Heatsink)}{R_{th}(GSR) + R_{th}(Heatsink)} = 3.46°C/W$$

To calculate the thermal resistance of the additional heat sink the following equation may be used :

$$R_{th}(Hs) = \frac{3.46 \cdot R_{th}(GSR)}{R_{th}(GSR) - 3.46} = \frac{3.46 \cdot 5}{5 - 3.46} = 10.54°C/W$$

HOW TO CHOOSE THE HEAT SINK (continued)

The following list may help the designer to select the proper commercially available heat sink.
Sometimes it can be more convenient to use a custom made heat sink that can be experimently designed and tested.

Manufacturers	Type	Rth	Mounting	Fastening
Thermalloy	6177	3	Horiz.	Screw
	6152	4	Vert.	Screw
	6111	10	Vert.	Adhes.
Fischer	SK18	3	Vert.	Screw
	SK48	3	Vert.	Screw
	SK07	4	Vert.	Adhes.
SGE Borsari	SR50	6	Vert.	Adhes.
Assmann	V5440	4	Vert.	Adhes.
	V5382	4	Horiz.	Screw
	V5460	3	Vert.	Screw
	V5510	3	Vert.	Screw

HOW TO CHOOSE THE PROTECTING FUSE

The GS-R400 family protects the load against overvoltage, by an internal crow-bar that continuously senses the output voltage and fires a thyristor when the voltage is higher than the nominal + 20%. Thyristor current capability is 150 A.

The crowbar can be activated either by an overvoltage generated by an external injected voltage, or by a failure of the module itself.

In the first case the module provides to limit the input current to a safe value, and to recover the normal operations it is sufficient to switch off the input voltage for a time greater than the discharge time of the input filter capacitor.

In the second case the failure is pratically a module input-output short circuit, the input current is no more limited by the module, and it is necessary to provide a method for disconnecting the module from the input voltage in a very short time to avoid failures of the board where the module is mounted.

The simplest method foresees the use of a fuse in the input path to limit the fault current to a safe value.

The proper fuse should be selected with some criteria :

- the fuse must handle the steady state current
- the fuse must handle the inrush current that occurs at turn-on
- the fuse must blow if the module has an input to output short circuit.

To this purpose, it is usual to select a fuse whose rated current is between 150 and 250 % of the rated full-load input current.

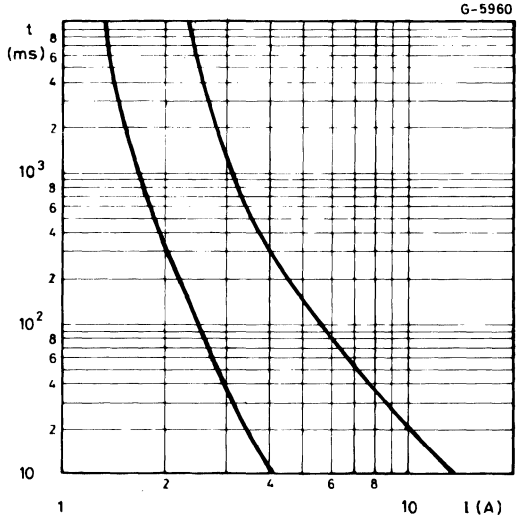
This usually provides enough overload capability to prevent fuse blowing from aging and fatigue due to repeated turn-on overload.

It is also necessary to examine the opening time versus the fuse overload characteristics, and the best choice is the high reliability, low cost, standard commercial units like 3AG, 3AB or DIN41661.

All the units must be of the fast type with fusing characteristics as depicted in dashed area of fig. 15.

HOW TO CHOOSE THE PROTECTING FUSE (continued)

Figure 15 : Fast fusing intervention curve.



As an example, for a GS-R405 unit supplied by a 24 Volt minimum input voltage, the fuse rating can be calculated as follows.

At a maximum delivered power of 20 Watt, assuming a 70 % efficiency, the input power will be 28.5 Watt and the input current 1.2 A.

The fuse rating will be 2A that guarantees a maximum fusing time of 20 ms (typical 2 ms) for a current of 20A that can be generally accepted without board problem.

SGS-THOMSON MICROELECTRONICS

GS-R400VB

140W SWITCHING VOLTAGE REGULATOR MODULE

- MTBF IN EXCESS OF 200.000 HOURS
- PC CARD OR CHASSIS MOUNTABLE
- HIGH OUTPUT CURRENT (4 A)
- HIGH INPUT VOLTAGE (48 V)
- ADJUSTABLE OUTPUT VOLTAGE (5.1 to 40 V)
- HIGH EFFICIENCY (up to 90%)
- SOFT START
- EXTERNAL SYNCHRONIZATION
- REMOTE INHIBIT/ENABLE
- REMOTE OUTPUT VOLTAGE SENSE
- NON-LATCHING SHORT CIRCUIT PROTECTION
- THERMAL PROTECTION
- CROW BAR PROTECTION FOR THE LOAD
- MAXIMUM CURRENT LIMITING

ORDER CODE : GS-R400VB

DESCRIPTION

The GS-R400VB is a HIGH CURRENT HIGH VOLTAGE SWITCHING VOLTAGE REGULATOR particularly suited for designing multiple outputs power supplies.

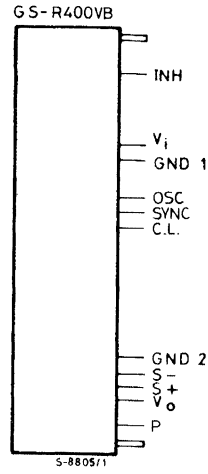
This step down regulator shielded for EMI, can provide local on-card regulation, or be used in central power supply systems, in both professional and industrial applications.

ABSOLUTE MAXIMUM RATINGS

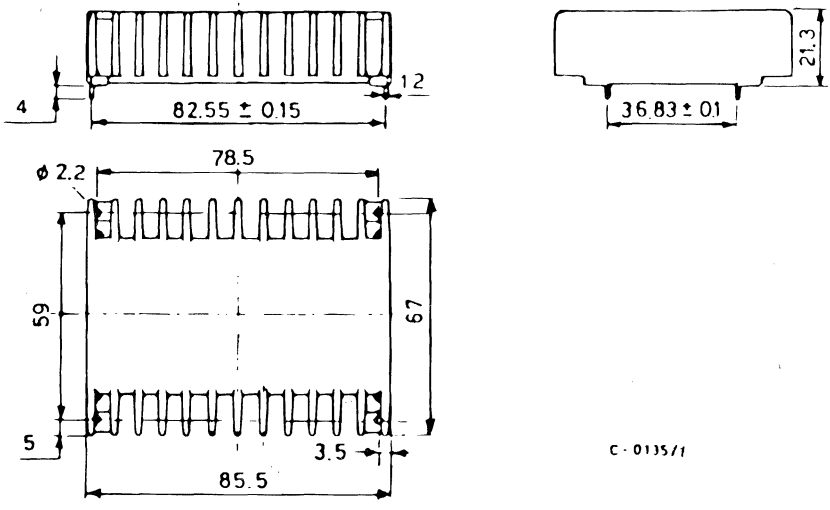
Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	48	V
I	Output Current	4	A
V_{INH}	Inhibit Voltage	15	V
T_{stg}	Storage Temperature Range	– 40 to + 105	°C
T_{cop}	Operating Case Temperatrure Range	– 20 to + 85	°C

Recommended maximum operating input voltage is 46 V.

CONNECTION DIAGRAM (side view)



MECHANICAL DATA (dimension in mm)



PIN FUNCTIONS

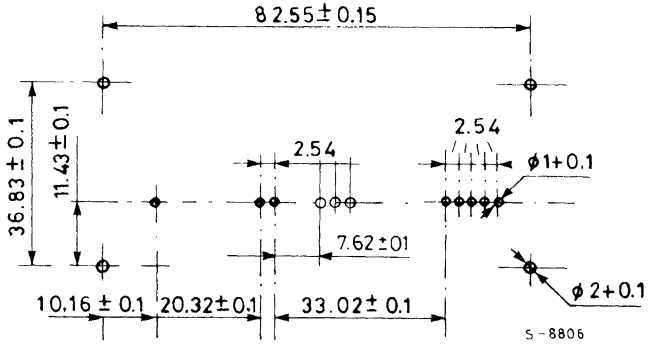
	PIN	FUNCTION
INH	– Inhibit	TTL compatible input. A logic high level signal applied to this pin disables the module. To be connected to GND_2 when not used.
V_i	– Input Voltage	Unregulated DC voltage input. Maximum voltage must not exceed 48 V. Recommended maximum operating voltage is 46 V.
GND_1	– Ground	Common ground for input voltage.
OSC	– Oscillator Output Pin	An internal RC network determines the 100 KHz PWM switching frequency. This pin must be connected SYNC if the unit is a Master.
SYNC	– Synchronization Input Pin	This pin must be connected to SYNC pin of the Master unit.
C.L.	– Current Limit	An external resistor connected between this pin and S – fixes the maximum output current (2,2 KΩ min). To be left open when current set is not used.
GND_2	– Ground	Common ground of high current path.
S –	– Sensing Negative	For connection to remote load, this pin senses the actual ground of the load itself. To be connected to GND_2 when not used. This pin is connected to case.
S +	– Sensing Positive	For connection to remote loads this pin allows voltage sensing on the load itself. To be connected to V_o when not used.
V_o	– Output Voltage	Regulated and stabilized DC voltage is available on this pin. Max output current is 4 A. The device is protected against short circuit of this pin to ground or to supply.
P	– Output Voltage Programming	A variable resistor (18 KΩ max) connected between this pin and S + sets the output voltage.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

	PARAMETER	Test Conditions	Min	Typ	Max	Unit
V_o	Output Voltage	$V_i = V_o + 8V$	5.1	–	40*	V
V_o	Temperature Stability	I_o = 1A $V_i = V_o + 8V$		0.2/1.6		mV/°C
V_i	Input Voltage	I_o = 1A	8		46	V
I_o	Output Current	$V_i = V_o + 8V$	0.2		4*	A
I_{OL}	Current Limit	$V_i = V_o + 8V$	0.5	5	8	A
I_{ISC}	Average Input Current	V_i = 46V Output shorted		0.2	0.4	A
f_S	Switching Frequency	I_o = 1A		100		KHz
η	Efficiency	$V_o = V_o + 8V$ I_o = 1A		75/90		%
ΔV_o	Line Regulation	I_o = 1A $V_i = V_o + 3V$ to 48V		2/6		mV/V
SVR	Supply Voltage Rejection	f_o = 100 Hz I_o = 1A		4/12	–	mV/V
ΔV_o	Load Regulation	ΔI_o = 2A (1 to 3A)		20/90	–	mV/A
V_r	Ripple Voltage	I_{OUT} = 2A		25/150		mV
t_{ss}	Soft Start Time	$V_{in} = V_{OUT} + 10V$		15	–	ms
V_{INHL}	Low Inhibit Voltage				0.8	V
V_{INHH}	High Inhibit Voltage		2.0		5.5	V
I_{INH}	Input Current High	V_{INH} = 5V			500	µA
t_{CB}	Crow bar Delay Time			5		µs
R_{CL}	Current Limit Resistor		2,2		∞	KΩ
R_{SET}	Voltage Setting Resistor		0		18	KΩ
V_{SD}	Max Differential Sense Voltage	V_o to S + S – to GND_2			100	mV

* Maximum Output Current is guaranteed up to V_o = 36V and derated linearly to 3A at V_o = 40V.

MOTHER BOARD LAYOUT



MODULE OPERATION

The GSR400VB is a step down switching mode voltage regulator.

Unregulated DC input voltage must be higher than nominal output voltage by, at least, 3 V. Minimum input voltage is therefore 8 V for 5.1 V output, while maximum input voltage is 48 V.

Output voltage is adjustable. The maximum current delivered by the output pin is 4 A and this value can be programmed by using an external resistor connected between C.L. pin and the S- pin. A minimum output current of 100 mA is required for proper module operation. In no-load condition, the module still works, but electrical characteristics are slightly modified vs. specifications. When external current limiting is not used, C.L. pin must be left open.

To prevent excessive over current at switch on, a soft start function is provided. Nominal output voltage is approached gradually in about 15 ms.

The module can be inhibited by a TTL, N MOS or C MOS compatible voltage applied to the INH pin. When this voltage is at high level, the module is switched off : if the inhibit signal goes from high to low level, the module restarts softly.

Maximum DC voltage applicable to this pin is 15 V. When remote control (inhibit) of the module is not used, the INH pin must be connected to GND_2.

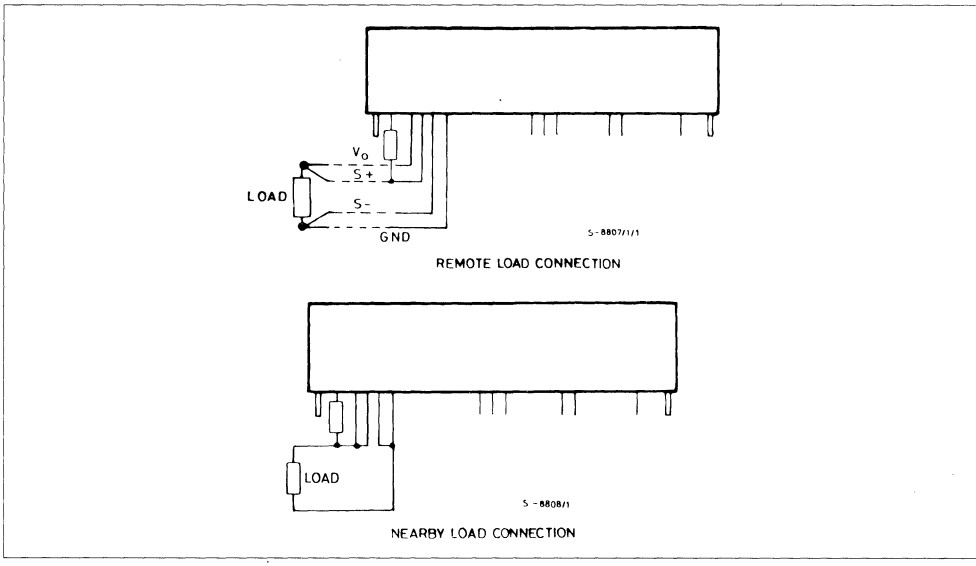
The remote load sensing is another feature provided by the GS–R400VB.

This function is performed by two pins (S+, S–) that can monitor the voltage directly across the load when this load is connected to the module by long wires : voltage drop on these wires is automatically compensated.

The case of the module is internally connected to S–. Therefore, the case must be always isolated from ground if S- is used.

The switching frequency of the module is 100 KHz. To prevent EMI, the module is contained in a metal box that provides shielding and heat-sink.

Figure 1 : Module connection to remote or nearby loads.



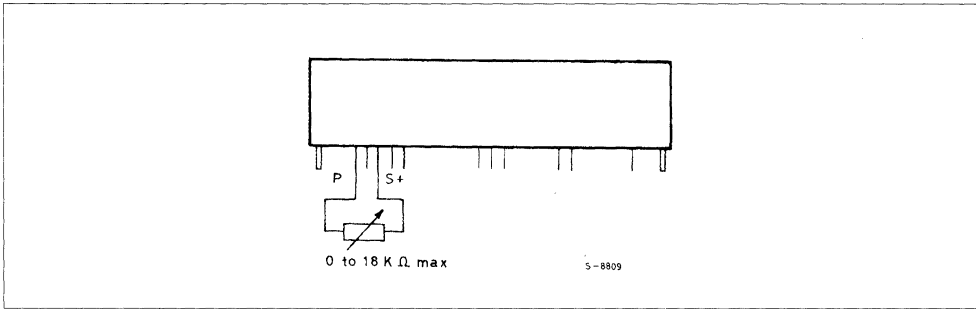
The output voltage can be adjusted in a range from 5.1 to 40 V by use of an external variable resistor as shown in Fig. 2.

The variable resistor can be substituted by a fixed resistor ; the value of Rx to obtain a fixed output voltage V_o is calculated according to the formula :

$$Rx = 2.67 \cdot \left(\frac{V_o}{5.1} - 1 \right) K\Omega$$

where V_o can vary from 5.1 to 40 V.

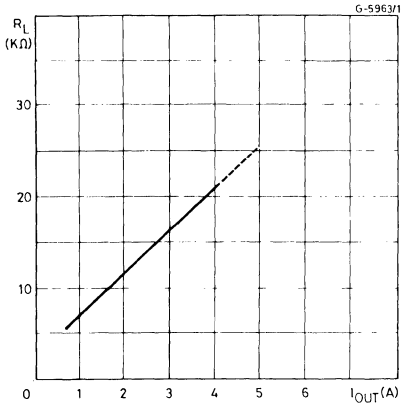
Figure 2 : Output voltage adjustment on GS–R400VB.



The output overcurrent protection limit can be programmed by using an external resistor R_L connected between to current limit C.L. pin and S –.

The value can be selected according to the curve shown in fig. 3.

Figure 3 : Current Limit vs programming resistor value.

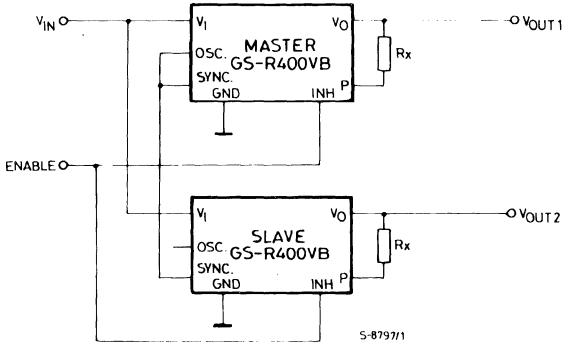


The GS–R400VB is designed for multiple outputs power supplies and to this purpose two pins, named OSCILLATOR and SYNCHRONIZATION are available.

When used in a stand alone application or as a master of a multiple outputs unit, these two pins must be tied together.

If the unit is a slave, the SYNC input must be connected to the OSC output of the master unit, and the OSC pin of the slave must be left open as shown in fig. 4.

Figure 4 : GS–R400VB multiple outputs connection.



The Oscillator output can drive up to four Synchronous inputs. The layout of the PCB must be accurately checked to avoid noise injection on the Oscillator output line, otherwise the overall power supply characteristics will be heavily impaired.

MODULE PROTECTIONS

Thermal Protection

The module has inside a thermal protection. When ambient temperature reaches prohibitive values, so that internal junction temperature of active components reaches 150C, the module is switched off. Normal operation is restored when internal junction temperature falls below 130C : this large hysteresis allows an extremely low frequency intermittent operation (ON - OFF) caused by thermal overload.

Short Circuit Protection

The module is protected against occasional and permanent short circuits of the output pin to ground or against output current overloads.

When output current exceeds the maximum programmed value the output is automatically disabled. After a fixed time, the module starts again in a soft mode : if the overload is still present, the module switches off and the cycle is repeated until the overload condition is removed. The average overload current is limited to a safe value for the module itself. Input current during output short circuit is always lower than in regular operation.

Load Protection

The module protects, by a crow bar circuit, the load connected to its output against overvoltages.

This circuit senses continuously the output volage : if, for any reason, the output voltage of the module exceeds by +20% the nominal value (fixed or adjustable), the crow bar protection is activated and it short circuits the output pin to ground. This protection prevents also damages to module if output pin is wrongly connected to supply voltage.

THERMAL DATA

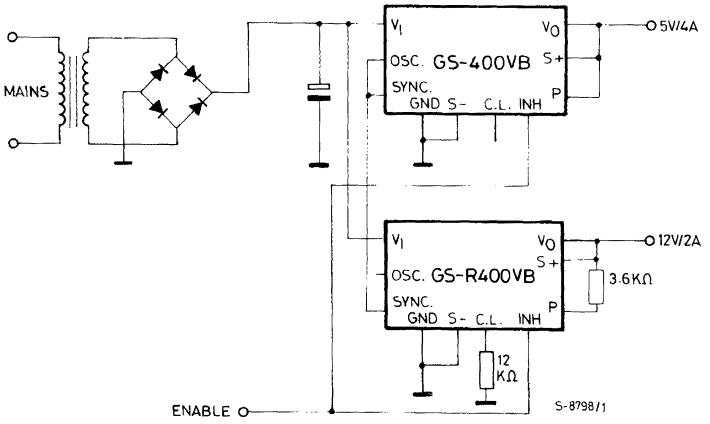
The thermal resistance module to ambient is about 5C/W. This means that if the internal power dissipation is 10 W, the temperature on the module surface is about 50C over ambient temperature.

According to ambient temperature and/or to power dissipation, an additional heatsink may be required.

Four holes are provided on the metal box of the module to allow the mounting of this optional external heat-sink.

TYPICAL APPLICATIONS

Figure 5 : Typical application on the GS–R400VB.



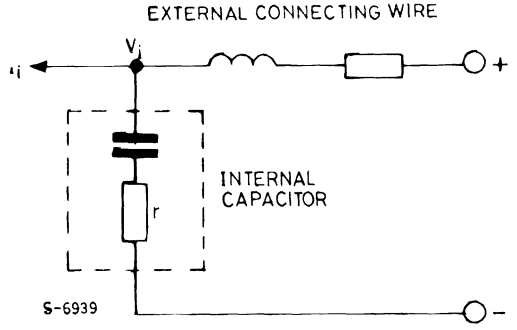
The high input voltage range allows both cost saving on 50/60 Hz transformer when the module is supplied from the main and the possibility to supply the module with batteries that, according to their charge status, can show large spread on voltage.

The module has, internally, an input filtering capacitor between pin V_I and GND_1. Therefore at the switching frequency the equivalent input circuit is as shown in fig. 6.

Since I_I is a high frequency alternating current, the inductance associated to long input connecting wire can cause a voltage ripple on point V_I that produces a ripple current across internal capacitor and a power dissipation on r.

When very long connecting wires are used, the input capacitor may be damaged by this power dissipation. For this reason it is suggested to keep input connecting wires as short as possible.

Figure 6 : Equivalent input circuit of GS–R400VB voltage regulator.



SWITCHING VOLTAGE REGULATOR MODULES

- MTBF IN EXCESS OF 500.000 HOURS
- NO EXTERNAL COMPONENTS REQUIRED
- PC CARD OR CHASSIS MOUNTABLE
- HIGH OUTPUT CURRENT (4 A)
- HIGH INPUT VOLTAGE (40 V)
- FIXED OUTPUT VOLTAGE (5.1 V; 12 V)
- HIGH EFFICIENCY (up to 85 %)
- SOFT START
- NON-LATCHING SHORT CIRCUIT PROTECTION
- THERMAL PROTECTION
- CROW BAR PROTECTION FOR THE LOAD
- HIGH POWER/VOLUME RATIO (24 Watt/cubic inch)

DESCRIPTION

The GS-R400/2 is a family of SMALL SIZE HIGH CURRENT HIGH VOLTAGE SWITCHING VOLTAGE REGULATORS.

These step down regulators, shielded for EMI, can provide local on-card regulation, or be used in central power supply systems, in both professional and industrial applications.

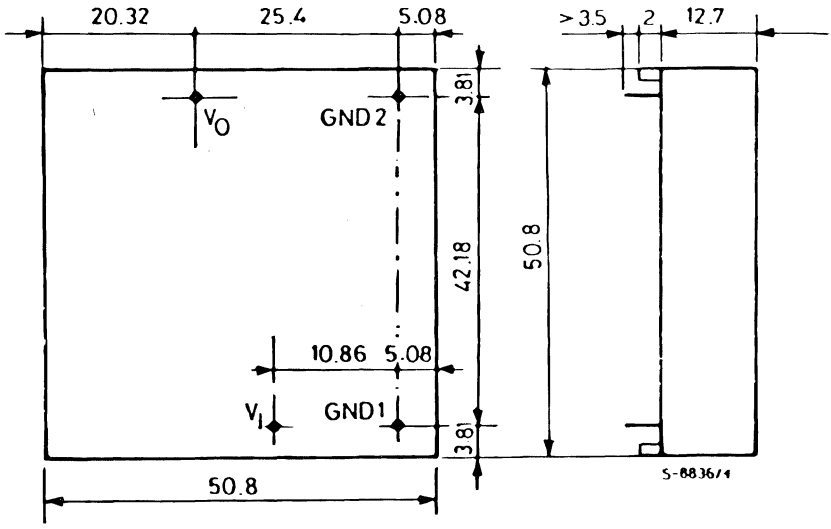
PRODUCTS FAMILY

Order Number	Output Voltage
GS-R405/2	5.1 V
GS-R412/2	12 V

ABSOLUTE MAXIMUN RATINGS

V_I	DC input voltage	40 V
I_O	Output Current	4 A
T_{stg}	Storage temperature range	- 40 to + 105°C
T_{cop}	Operating case temperature range	- 20 to + 85°C

MECHANICAL DIMENSIONS AND CONNECTION DIAGRAM (Bottom view)



PIN FUNCTIONS

	PIN	FUNCTION
V_i	- Input Voltage	Unregulated DC voltage input. Maximum voltage must not exceed 40 V.
GND_1	- Ground	Common ground for input voltage.
GND_2	- Ground	Common ground of high current path.
V_o	- Output Voltage	Regulated and stabilized DC voltage is available on this pin. Max output current is 4 A. The device is protected against short circuit of this pin to ground or to supply.

The case is electrically connected to GND.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C Unless otherwise specified)

TYPE			GS-R 405/2			GS-R 412/2			UNIT
PARAMETER		Test Condit.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_o	Output Voltage	V_i = 24 V I_o = 1 A	5	5.1	5.2	11.5	12	12.5	V
V_o	Temperature Stability	V_i = 24 V I_o = 1 A		0.2			0.5		mv °C
V_i	Input Voltage	I_o = 1 A	9		40	16		40	V
I_O	Output Current*	V_i = 24 V	0.1		4	0.1		4	A
I_{OL}	Current Limit	V_i = V_o + 8 V		5	8		5	8	A
I_{isc}	Average Input Current	V_i = 40 V Output shorted		0.1	0.2		0.1	0.2	A
f_s	Switching Frequency			100			100		kHz
η	Efficiency	V_i = 24 V I_o = 2 A		80			85		%
ΔV_o	Line Regulation	I_o = 1 A V_i = 16 to 26 V		2			2		mV/V
SVR	Supply Voltage rejection	f = 100 Hz I_o = 1 A		4			6		mV/V
ΔV_o	Load Regulation	V_i = 24 V I_o = 0.5 to 1.5 A		20			40		mV/A
V_r	Ripple Voltage	I_{out} = 2 A		25			50		mV
V_n	Noise Voltage	I_{out} = 2 A		25			35		mV
I_r	Reflected I_{in}	V_i = 24 V I_o = 1 A		60			120		mA
T_{r1}	Line Transient recovery time	I_o = 1 A V_i = 16 to 26 V		500			500		ms
T_{r2}	Load Transient recovery time	V_i = 24 V V_i = 0.5 to 1.5		100			100		ms
R_{th}	Thermal resistance			8			8		°C/W
t_{ss}	Soft start time	V_{in} = V_{out} + 10 V		15			25		ms
t_{CB}	Crow bar Delay Time			5			5		ms
V_{CB}	Crow bar Delay Threshold			6			14.5		V

* The maximum current can be delivered when t_{case} < 85°C. Forced ventilation or additional heat-sink may be required to keep T_{case} < 85°C.

MODULE OPERATION

The GSR400/2 series is a family of step down switching mode voltage regulators.
Unregulated DC input voltage must be higher than nominal output voltage by, at least, 4 V.
Minimum input voltage is therefore 9 V for GS-R405/2 and maximum input voltage is 40 V for all the types.
The output voltage is fixed and the maximum current delivered by the output pin is 4A. A minimum output current of 100 mA is required for proper module operation. In no-load condition, the module still works, but the electrical characteristics are slightly modified vs. specifications.
To prevent excessive over current at switch on, a soft start function is provided. Nominal output voltage is approached gradually in about 15 to 25 ms.
The switching frequency of the module is 100 KHz. To prevent EMI, the module is contained in a metal box that provides shielding and heat-sink.

MODULE PROTECTIONS

Thermal Protection

The module is provided with a thermal protection. When ambient temperature reaches prohibitive values, so that internal junction temperature of active components reaches 150 °C, the module is switched off. Normal operation is restored when internal junction temperature falls below 130°C : this large hysteresis allows an extremely low frequency intermittent operation (ON - OFF) caused by thermal overload.

Short Circuit Protection

The module is protected against occasional and permanent short circuits of the output pin to ground or against output current overloads.
When the output current exceeds the maximun allowed value for safe operation, the output is automatically disabled. After a fixed time, the module starts again in a soft mode : if the overload is still present, the module switches off and the cycle is repeated until the overload condition is removed.The average overload current is limited to a safe value for the module itself. Input current during output short circuit is always lower than in regular operation.

Load Protection

The module protects, by a crow bar circuit, the load connected to its output against overvoltages. This circuit senses continuously the outpout voltage : if, for any reason, the output voltage of the module exceeds by + 20 % the nominal value, the crow bar protection is activated and it short circuits the output pin to ground. This protection prevents also damages to the module if the output pin is wrongly connected to the supply voltage.

OPERATING AMBIENT TEMPERATURE RANGE

The GS-R400/2 modules are power devices, i.e. devices that deliver and dissipate power. The power dissipation is related to the delivered output power by

$$P_d = P_o \left(\frac{1}{\eta} - 1\right)$$

where η = efficiency = $\frac{P_o}{P_{IN}}$

The operating ambient temperature range cannot be simply defined by numbers because it depends on many conditions that must be previously defined.
On the contrary, the operating case temperature is well defined and it ranges from - 20 to + 85 °C.
The two extremes are imposed by reliable operation of aluminium electrolytic capacitors that are housed inside the modules.
From these data, the maximun ambient temperature range can be easily calculated, as show in the following example :

V_{IN} = 24V V_{OUT} = 5 V ; 12V I_{OUT} = 3A.

The dissipated powers of GS-R405/2 and GS-R412/2 are respectively :

$P_{d\ 5V}$ = 3.75W $P_{d\ 12V}$ = 6.4W

By knowing the thermal resistance case to ambient R_{TH} = 8°C / W for natural convection condition, the maximun ambient temperature for a case maximum temperature of 85°C will be

$$T_{amb\ max} = T_{case\ max} - P_d \cdot R_{TH}$$

i.e.

$$T_{amb\ 5v} = 85 - 3.75 \cdot 8 = 55°C \text{ max}$$

$$T_{amb\ 12V} = 85 - 8 \cdot 64 = 34°C \text{ max}$$

This ambient temperature can be increased by lowering the thermal resistance case to ambient. Various methods can be adopted such as addition of external heat-sink on forced ventilation or both.
If an external heat-sink with R_{TH} = 10°C/W is used, the values are modified as follows.
The total thermal resistance case to ambient is the parallel of the two thermal resistances

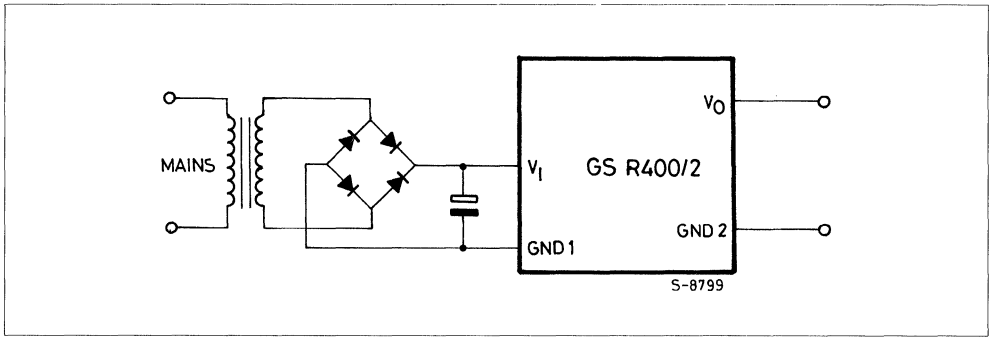
$$R_{TH\ TOT} = \frac{R_{TH\ CASE} \cdot R_{TH\ HEAT\text{-}SINK}}{R_{TH\ CASE} + R_{TH\ HEAT\text{-}SINK}} = 4.5°C/W$$

$T_{amb\ 5V}$ = 68°C max $T_{amb\ 12V}$ = 56°C max

TYPICAL APPLICATIONS

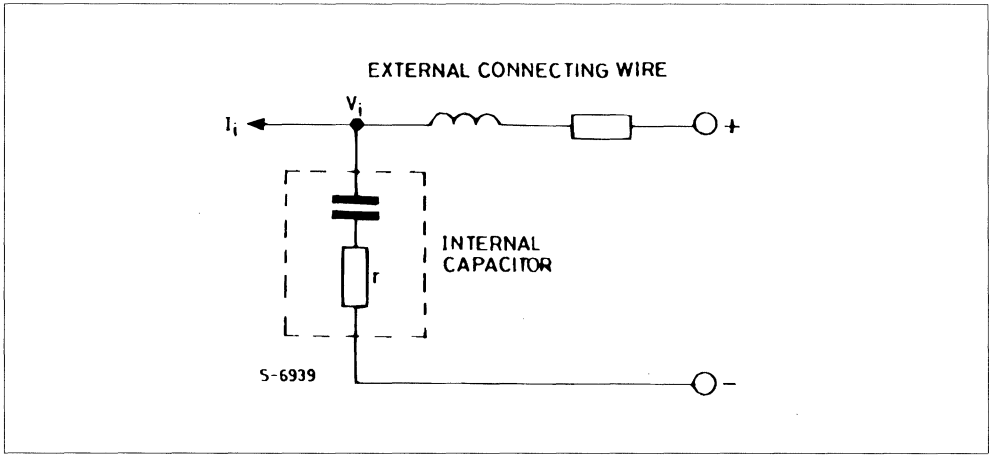
The high input voltage range allows both cost saving on 50/60 Hz transformer when the module is supplied from the mains, and the possibility to supply the module with batteries that, according to their charge status, can show large spread on voltage.

Figure 1 - A Typical Application of GS-R400/2 Voltage Regulator



The module has, internally, an input filtering capacitor between pin V_I and GND_1. Therefore, at the switching frequency the equivalent input circuit is as shown in fig. 2.

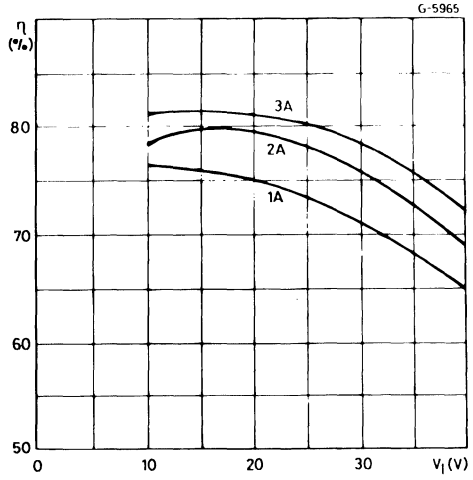
Figure 2 - Equivalent Input Circuit of GS-R400/2 Voltage Regulator



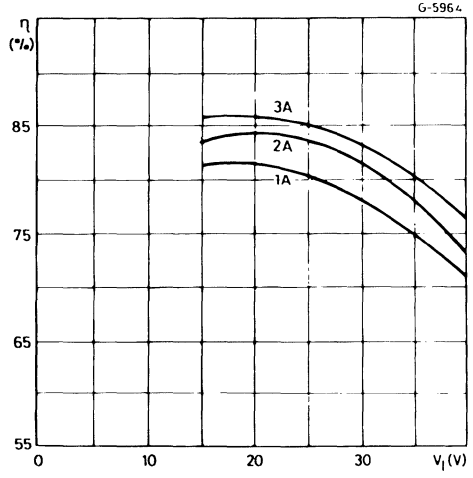
Since I_I is a high frequency alternating current, the inductance associated to long input connecting wire can cause a voltage ripple on point V_I that produces a ripple current across internal capacitor and a power dissipation on r.

When very long connecting wires are used, the input capacitor may be damaged by this power dissipation. For this reason it is suggested to keep input connecting wires as short as possible.

EFFECIENCY VS. INPUT VOLTAGE & OUTPUT CURRENT



GS-R405/2



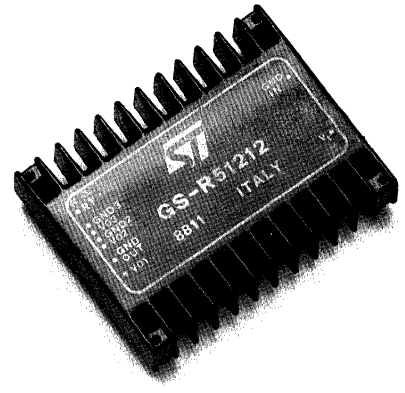
GS-R412/2

SGS-THOMSON
MICROELECTRONICS

GS-R51212

TRIPLE OUTPUT SWITCHING VOLTAGE REGULATOR MODULE

- MTBF IN EXCESS OF 200.000 HOURS
- NO EXTERNAL COMPONENTS REQUIRED
- PC CARD OR CHASSIS MOUNTABLE
- HIGH OUTPUT CURRENT (3.5 A on 5 V output)
- HIGH INPUT VOLTAGE (40 V)
- TWO 12 V ; 0.15 A ISOLATED OUTPUTS
- HIGH EFFICIENCY
- SOFT START
- RESET OUTPUT
- NON-LATCHING SHORT CIRCUIT PROTECTION
- THERMAL PROTECTION
- CROW BAR PROTECTION FOR THE LOAD



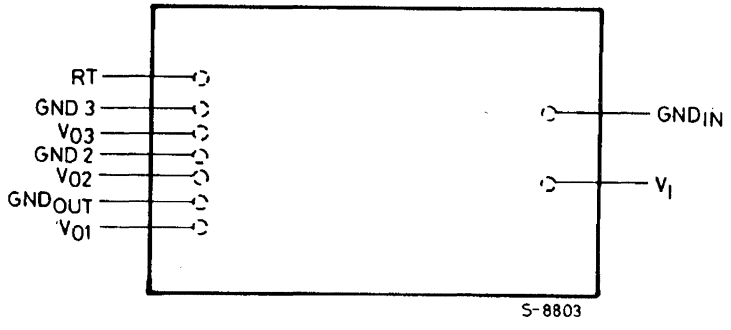
ORDER CODE : GS-R51212

DESCRIPTION

The GS-R51212 is a triple output HIGH CURRENT HIGH VOLTAGE SWITCHING VOLTAGE REGULATOR that provides +5 V and two isolated 12 V outputs.

This step down regulator shielded for EMI, provides local on-card regulation. The very large input voltage range allows flexibility in both professional and industrial applications.

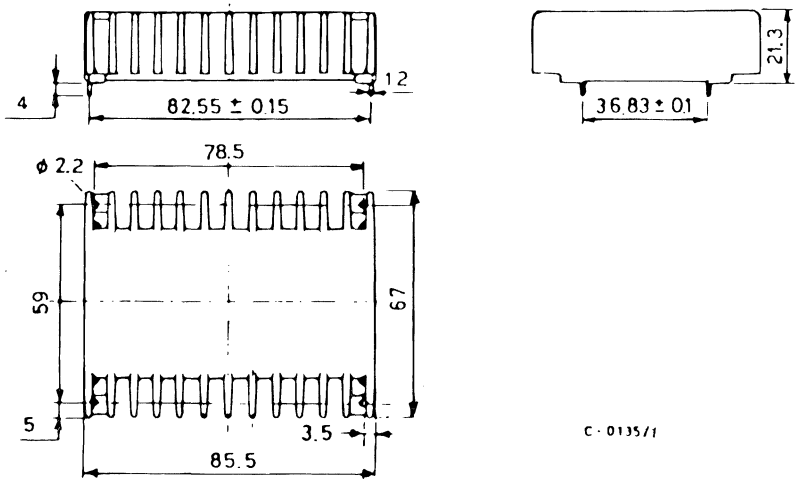
CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

V_i	DC input voltage	40 V
I_{RT}	Reset output sink current	20 mA
T_{stg}	Storage temperature range	– 40 to + 105°C
T_{cop}	Operating case temperature range	– 20 to + 85°C

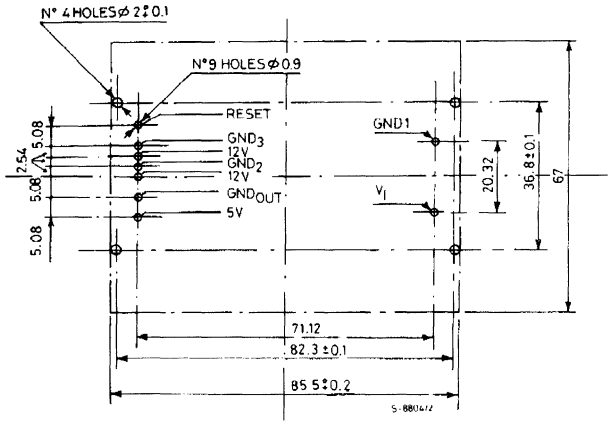
MECHANICAL DATA (dimensions in mm)



PIN FUNCTIONS

PIN		FUNCTION
RT	Reset Output	Reset output is high when output voltage reaches nominal value (5.1 V) and it is generated with a fixed 100 ms delay. A proper resistor (270 Ω min) must be connected between this pin and V_{O1}
V_i	Input Voltage	Unregulated DC voltage input. Maximum voltage must not exceed 40 V.
GND_{IN}	Ground	Common ground for input voltage.
GND_{OUT}	Ground	Common ground of high current path. The case of the module is connected to this pin.
V_{O1}	5 V Output Voltage	Regulated and stabilized DC voltage is available on this pin. Max output current is 3.5 A. The device is protected against short circuit of this pin to ground or to supply.
V_{O2}	12 V Output Voltage	Regulated and stabilized 12 V DC output at 150 mA max. current referred to GND_2. This output can float ± 200 V in respect to GND_{OUT} and GND_3.
GND_2	Ground	Reference ground for V_{O2} output.
V_{O3}	12 V Output Voltage	Regulated and stabilized 12 V DC output at 150 mA max. current referred to GND_3. This output can float ± 200 V in respect to GND_{OUT} and GND_2.
GND_3	Ground	Reference ground for V_{O3} output.

MOTHER BOARD LAYOUT Printed Circuit Drilling (components side).



Printed Circuit Drilling (component side).

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

PARAMETER		Test Conditions	Min	Typ	Max	Unit
V_{o1}	Output Voltage	V_i = 24 V I_{o1} = 2.5 A	4.95	5.1	5.2	V
V_{o2}	Output Voltage	V_i = 24 V I_{o2} = 0.1 A *	11.5		12.5	V
V_{o3}	Output Voltage	V_i = 24 V I_{o3} = 0.1 A *	11.5		12.5	V
V_o	Temperature Stability	All Outputs		0.2		mV/°C
V_i	Input Voltage		9.0		40	V
I_{o1}	Output Current	V_i = 24 V	0.5		3.5	A
I_{o2}	Output Current	V_i = 24 V *			.15	A
I_{o3}	Output Current	V_i = 24 V *			.15	A
I_{sc}	Average Input Current	V_i = 40 V V_{out1} = 0 V		0.2		A
I_{sc}	Average Input Current	V_i = 40 V $V_{out1/2/3}$ = 0 V		0.4		A
I_r	Reflected lin	V_i = 24 V I_{o1} = 2.5 A I_{o2} = 0.1A I_{o3} = 0.1 A		160		mA
f_s	Switching Frequency			100		KHz
η	Efficiency	V_i = 24 V I_{o1} = 2.5 A I_{o2} = 0.1 A I_{o3} = 0.1 A		75		%
ΔV_o	Line Regulation	I_{o1} = 2.5 A V_I = 15 to 25 V I_{o2} = 0.1 A I_{o3} = 0.1 A		2		mV/V
ΔV_o	Load Regulation	V_i = 24 V I_{o1} = .5 to 2.5 A V_i = 24 V I_{o2} = .05 to .1 A V_i = 24 V I_{o3} = .05 to .1 A		20 1 1		mV/A mV/A mV/A
SVR	Supply Rejection	50/60Hz		4		mV/V
V_r	Ripple Voltage	V_i = 24 V I_{o1} = 2.5 A		30		mV
V_n	Noise Voltage	V_i = 24 V I_{o1} = 2.5 A		40		mV
I_{rh}	Reset leakage Current				100	µA
V_{rl}	Reset Low Level	I_{reset} = 5mA		0.2		V
T_{rd}	Reset Delay Time			100		ms
T_{r1}	Line Transient Recovery Time	I_{o1} = 2.5 A V_i = 15 to 35 V		500		µs
T_{r2}	Load Transient Recovery Time	V_i = 24 V I_o = .5 to 2.5 A		200		µs
R_{th}	Thermal Resistance			5		°C/W

* I_{out1} = 0.5 A.

MODULE OPERATION

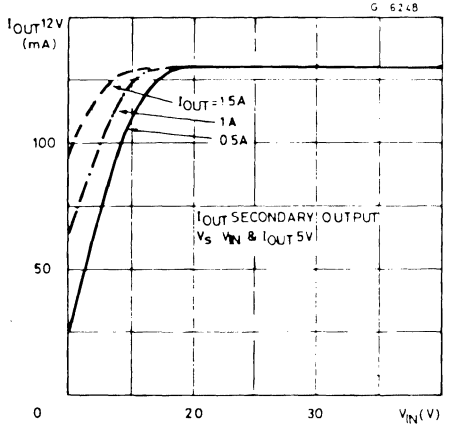
The GS-R51212 is a triple output switching mode voltage regulator.

Unregulated DC input voltage must be higher than nominal output voltage by, at least, 4V. Minimum input voltage is therefore 9 V while maximum input voltage is 40 V.

The main output voltage is 5V and the maximum current delivered is 3.5 A. A minimum output current of 500 mA is required for proper module operation.

The current available on the 12 Volt outputs depends on the current delivered by the main output and the value of the input voltage.

Figure 1 : Current available from 12 V output vs. input voltage and 5 V output current.



To prevent excessive over current at switch on, a soft start function is provided. Nominal output voltage is approached gradually in about 15 ms.

The switching frequency of the module is 100 KHz. To prevent EMI, the module is contained in a metal box that provides shielding and heat-sink.

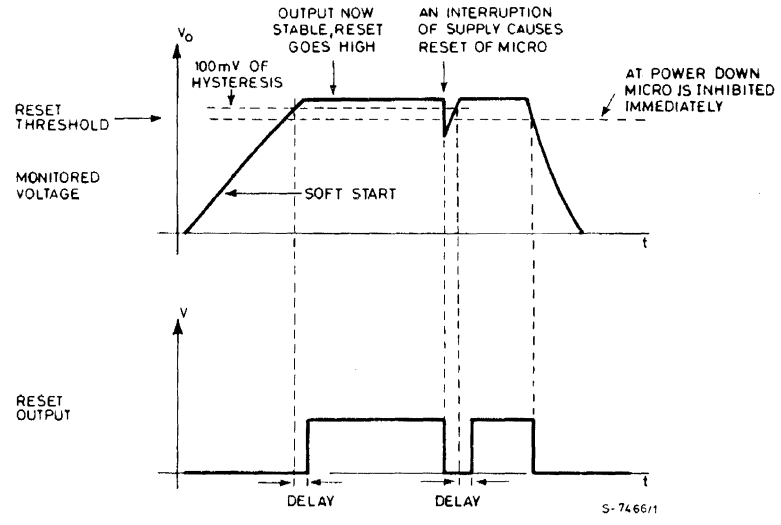
The RESET output is an auxiliary function useful to reset or inhibit microprocessors when the output voltage, at switch on and off, reaches a prefixed value of 4.9 to 5.1 V or when the output voltage, for any reason, drops below nominal value by more than 100 mV. In any case the minimum falling threshold value is 4.75 V or higher and the reset output voltage is generated with a fixed delay of 100 ms.

This is an open collector output to guarantee maximum flexibility.

Time delay of the reset function also rejects wrong information caused by occasional spikes generated during switch on and off.

MODULE OPERATION (continued)

Figure 2 : Reset as a function of output voltage and time.



MODULE PROTECTIONS

Thermal protection

The module has inside a thermal protection. When ambient temperature reaches prohibitive values, so that internal junction temperature to active components reaches 150°C, the module is switched off. Normal operation is restored when internal junction temperature falls below 130°C: this large hysteresis allows an extremely low frequency intermittent operation (ON-OFF) caused by thermal overload

Short circuit protection

The module is protected against occasional and permanent short circuits of the output pins to their respective grounds or against output current overloads.
When the 5 V output current exceed the maximum allowed value for safe operation, the output is automatically disabled. After a fixed time, the module starts again in a soft mode: if the overload is still present, the module switches off and the cycle is repeated until the overload condition is removed. The average overload current is limited to a safe value for the module itself. Input current during output short circuit is always lower than in regular operation.

Load protection

The module protects, by a crow bar circuit, the load connected to the 5 V output against overvoltages. This circuit senses continuously the output voltage: if, for any reason, the output voltage of the module exceeds 6 V, the crow bar protection is activated and it short circuits the output pin to ground.

THERMAL DATA

The thermal resistance module to ambient is about 5°C/W. This means that if the internal power dissipation is 10 W, the temperature of the module surface is about 50°C over ambient temperature. According to ambient temperature and/or to power dissipation, an additional heat-sink may be required. Four holes are provided on the metal box of the module to allow this mounting of this optional external heat-sink.

TYPICAL APPLICATION

The high input voltage range allows both cost saving on 50/60 Hz transformer when the module is supplied from the main and the possibility to supply the module with batteries that, according to their charge status, can show large spread on voltage.
The module has, internally, an input filtering capacitor between pin V_I and GND_1. At a high switching frequency the equivalent input circuit is as shown in Fig. 2.
Since I_I is a high frequency alternating current, the inductance associated to long input connecting wire can cause a voltage ripple on point. V_I that produces a ripple current across internal capacitor and a power dissipation on r.
When very long connecting wires are used, the input capacitor may be damaged by this power dissipation. For this reason it is suggested to keep input connecting wires as short as possible.

Figure 3 : Equivalent input circuit of GS-R51212 voltage regulator.

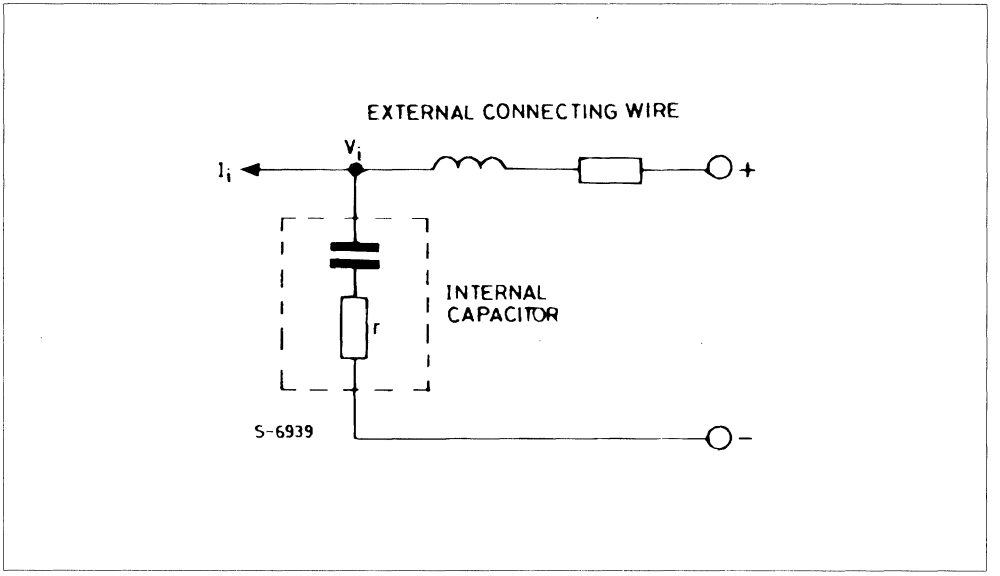
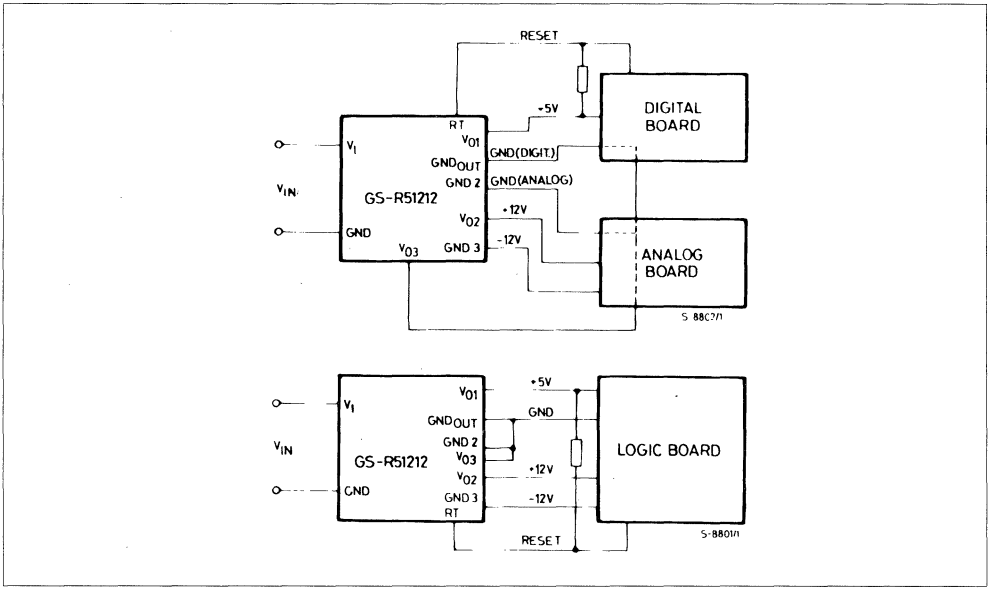
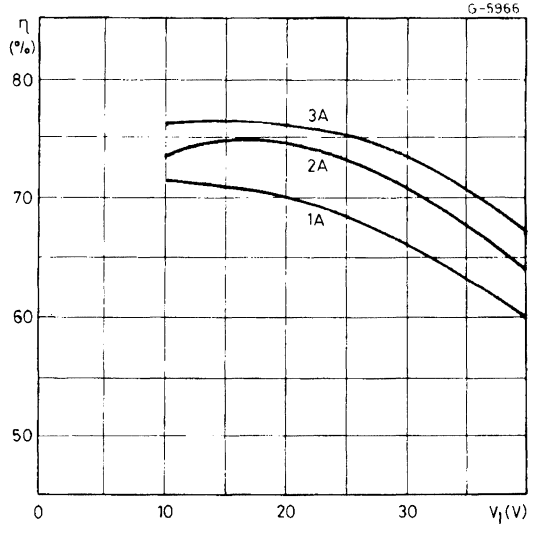


Figure 4 : GS-R51212 typical applications.



EFFICIENCY VS. INPUT VOLTAGE



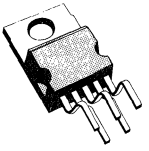
SGS-THOMSON MICROELECTRONICS

L149

4A LINEAR DRIVER

- HIGH OUTPUT CURRENT (4A peak)
- HIGH CURRENT GAIN (10.000 typ.)
- OPERATION UP TO ± 20 V
- THERMAL PROTECTION
- SHORT CIRCUIT PROTECTION
- OPERATION WITHIN SOA
- HIGH SLEW-RATE (30 V/ µs)

The L149 is a general purpose power booster in Pentawatt® package consisting of a quasi-complementary darlington output stage with the associated biasing system an inhibit facility.
The device is particularly suited for use with an operational amplifier inside a closed loop configuration to increase output current.



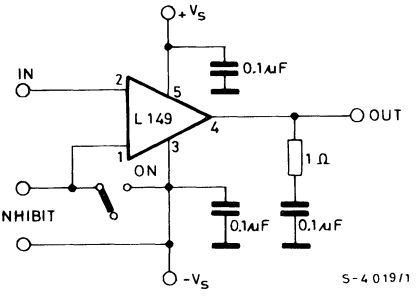
Pentawatt®

ORDER CODE : L149V

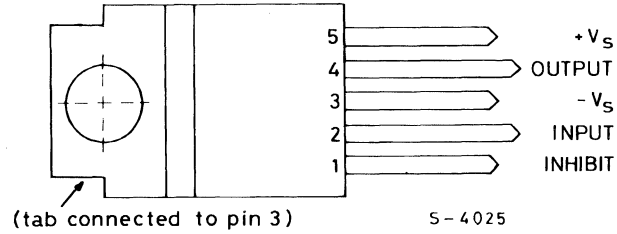
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 20	V
V_i	Input Voltage		V_s
$V_5 - V_4$	Upper Power Transistor V_{CE}	40	V
$V_4 - V_3$	Lower Power Transistor V_{CE}	40	V
I_o	DC Output Current	3	A
I_o	Peak Output Current (internally limited)	4	A
V_{INH}	Input Inhibit Voltage	$-V_s + 5$ $-V_s - 1.5$	V V
P_{tot}	Power Dissipation at T_{case} = 75 °C	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

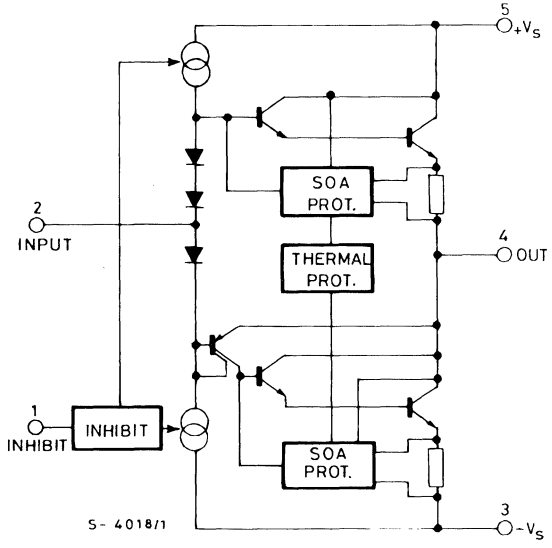
TEST CIRCUIT



CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, V_s = ± 16V)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage					± 20	V
I_d	Quiescent drain current	V_s = ± 16V			30		mA
I_{in}	Input current	V_s = ± 16V	V_i = OV		200	400	µA
h_{FE}	DC current gain	V_s = ± 16V	I_o = 3A	6000	10000		–
G_v	Voltage gain	V_s = ± 16V	I_o = 1.5A		1		–
V_{CEsat}	Saturation voltage (for each transistor)	I_o = 3A				3.5	V
V_{os}	Input offset voltage	V_s = ± 16V				0.3	V
V_{INH}	Inhibit input voltage (pins 1-3)	ON condition				± 0.3	V
		OFF condition		± 1.8			
R_{INH}	Inhibit input resistance				2.0		KΩ
SR	Slew rate				30		V/ µs
B	Power bandwidth	V_o = ± 10V, d = 1 %, R_L = 8Ω			200		KHz

APPLICATION INFORMATION

Figure 1 : High slew-rate power operational amplifier (SR = 13V/ µs).

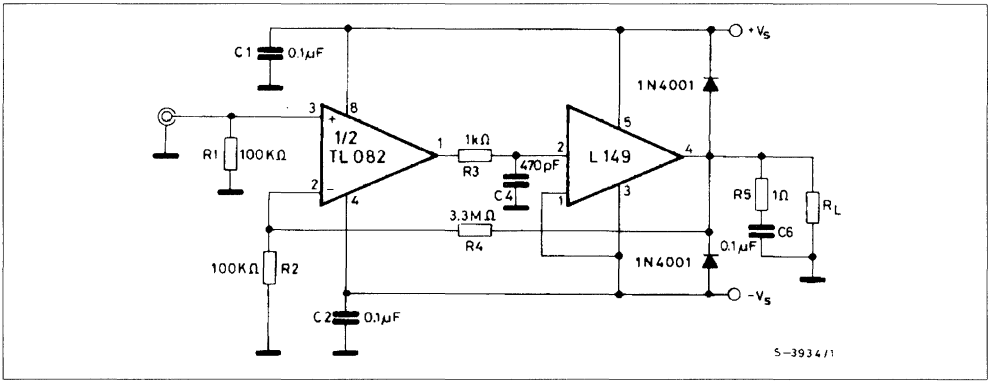


Figure 2 : Maximum saturation voltage vs. output current.

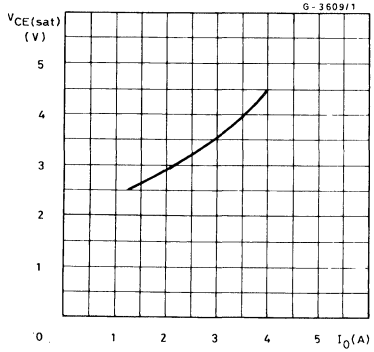


Figure 3 : Current limiting characteristics..

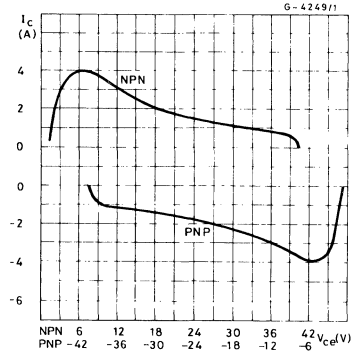


Figure 4 : Supply voltage rejection vs. frequency.

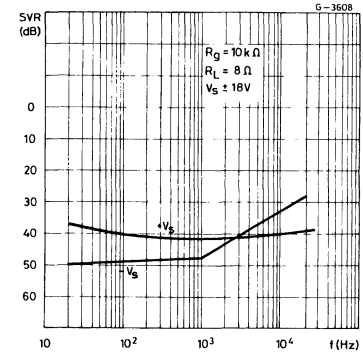


Figure 5 : Distortion vs. output power (f = 1 KHz).

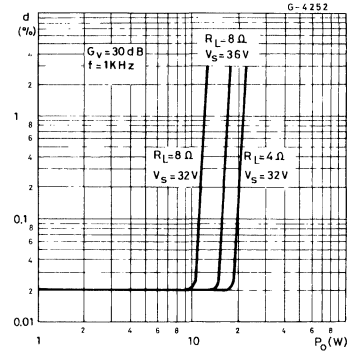


Figure 6 : Distortion vs. output power (f = 10 KHz).

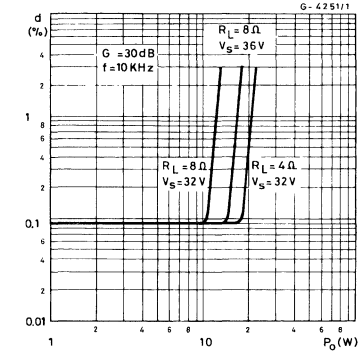
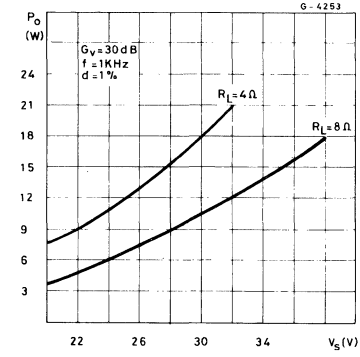


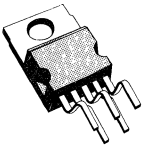
Figure 7 : Output power vs. supply voltage.



3A POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT UP TO 3A
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES
- SOA PROTECTION
- THERMAL PROTECTION
- ± 18V SUPPLY

The L165 is a monolithic integrated circuit in Pentawatt® package, intended for use as power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.



Pentawatt®

ORDER CODE : L165V

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 18	V
$V_5 - V_4$	Upper power transistor V_{CE}	36	V
$V_4 - V_3$	Lower power transistor V_{CE}	36	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Peak output current (internally limited)	3.5	A
P_{tot}	Power dissipation at T_{case} = 90°C	20	W
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

APPLICATION CIRCUITS

Figure 1 : Gain > 10.

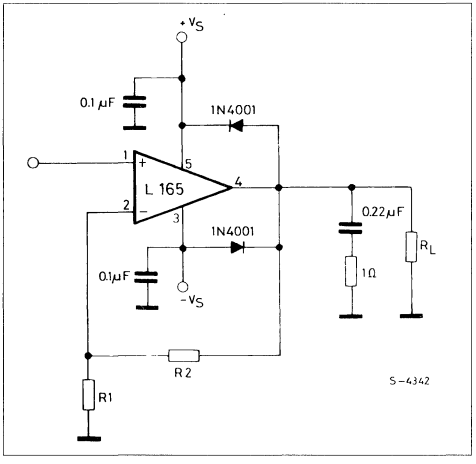
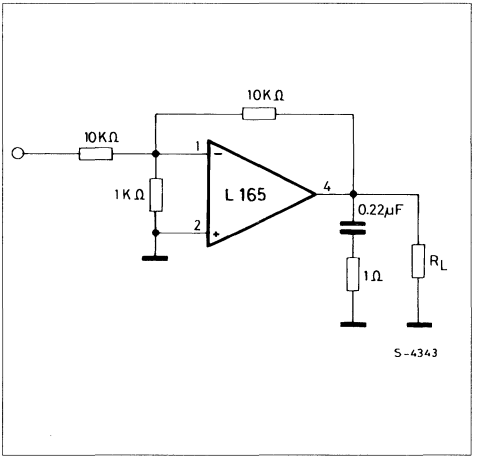
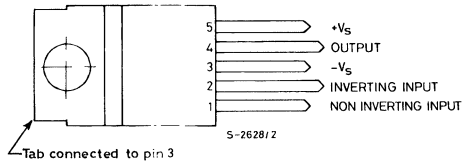


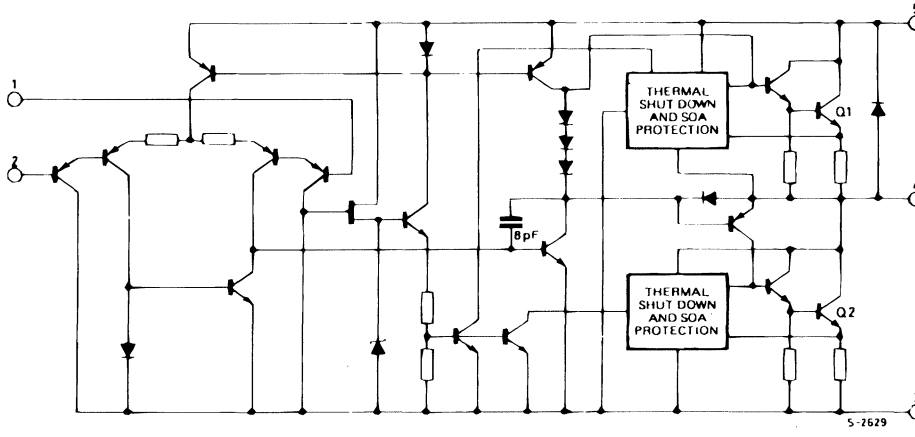
Figure 2 : Unity gain configuration.



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = ± 15 V, T_j = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 18	V
I_d	Quiescent Drain Current	V_s = ± 18 V		40	60	mA
I_b	Input Bias Current			0.2	1	µA
V_{os}	Input Offset Voltage			± 2	± 10	mV
I_{os}	Input Offset Current			± 20	± 200	nA
SR	Slew-rate	G_v = 10		8		V/µs
		G_v = 1 (°)		6		
V_o	Output Voltage Swing	f = 1 kHz I_p = 0.3 A		27		V_{pp}
		f = 1 kHz I_p = 3 A		24		V_{pp}
		f = 10 kHz I_P = 0.3 A		27		V_{PP}
		f = 10 kHz I_P = 3 A		23		V_{PP}
R	Input Resistance (pin 1)	f = 1 KHz	100	500		KΩ
G_v	Voltage Gain (open loop)			80		dB
e_N	Input Noise Voltage	B = 10 to 10 000 Hz		2		µV
i_N	Input Noise Current			100		pA
CMR	Common-mode Rejection	R_g ≤ 10 KΩ G_v = 30 dB		70		dB
SVR	Supply Voltage Rejection	R_g = 22 KΩ, V_{ripple} = 0.5 V_{rms}, f_{ripple} = 100 Hz, G_v = 10		60	dB	dB
		R_g = 22 KΩ, V_{ripple} = 0.5 V_{rms}, f_{ripple} = 100 Hz, dBG_v = 100		40		dB
	Efficiency	f = 1 kHz, I_p = 1.6 A ; P_o = 5 W		70		%
		R_L = 4 Ω, I_p = 3 A ; P_o = 18 W		60		%
T_{sd}	Thermal Shut-down Case Temperature	P_{tot} = 12 W		110		°C
		P_{tot} = 6 W		130		°C

Figure 3 : Open loop frequency response.

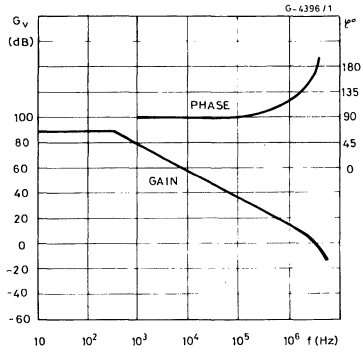


Figure 4 : Closed loop frequency response (circuit of figure 2).

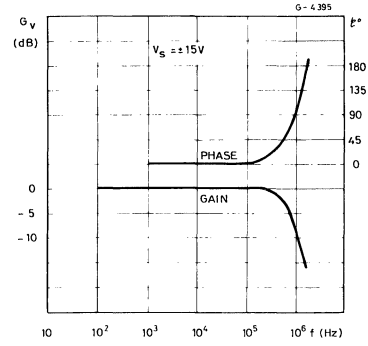


Figure 5 : Large signal frequency response.

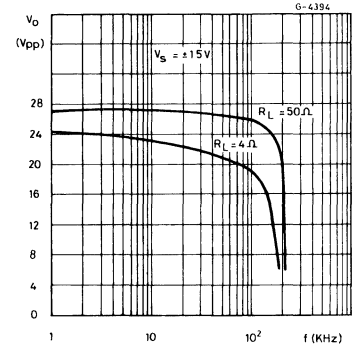


Figure 6 : Maximum output current vs. voltage [VCE] across each output transistor.

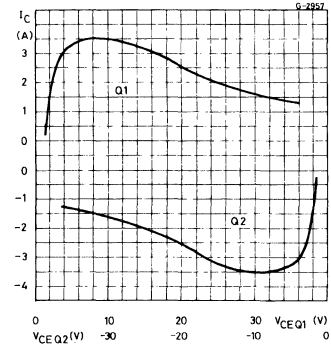


Figure 7 : Safe operating area and collector characteristics of the protected power transistor.

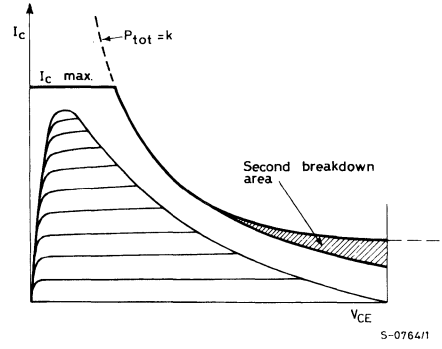


Figure 8 : Maximum allowable power dissipation vs. ambient temperature.

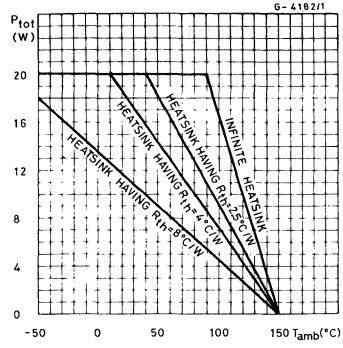
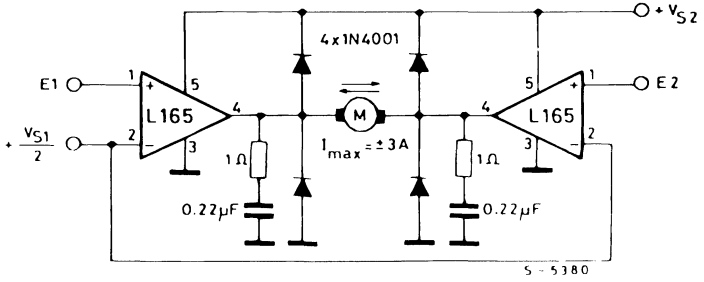
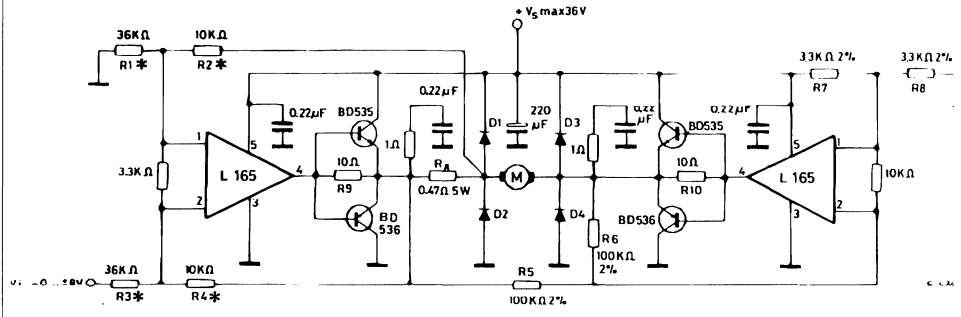


Figure 9 : Bidirectional DC motor control with TTL/CMOS/µP compatible inputs.



Must be $V_{S2} \geq V_{S1}$ E1, E2 = logic inputs
V_{S1} = logic supply voltage

Figure 10 : Motor current control circuit with external power transistors (I_{motor} > 3.5A).

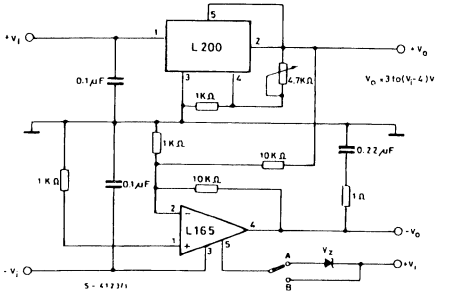


D1 to D4 : $V_F \leq 1.2$ @ I = 4A
trr ≤ 500 ns

Note : The input voltage level is compatible with L291 (5-BIT D/A converter).

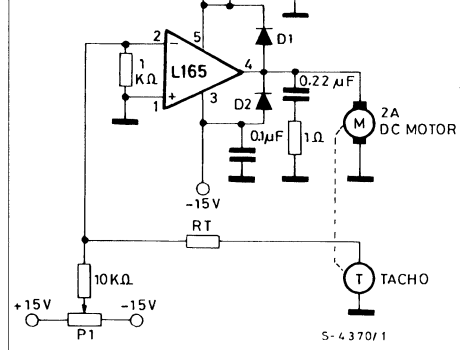
The transfer function is : $\frac{I_M}{V_i} = \frac{R4}{Rx\ R3}$

Figure 11 : High current tracking regulator.



A : for $\pm 18 \leq V_i \leq \pm 32$
Note : V_Z must be chosen in order to verify
$2\,V_i - V_Z \leq 36V$
B : for $V_i \leq \pm 18V$

Figure 12 : Bidirectional speed control of DC motor (Compensation networks not shown).



D1, D2 : VF ≤ 1.2V @ I = 2A
trr ≤ 500 ns

Figure 13 : Split power supply.

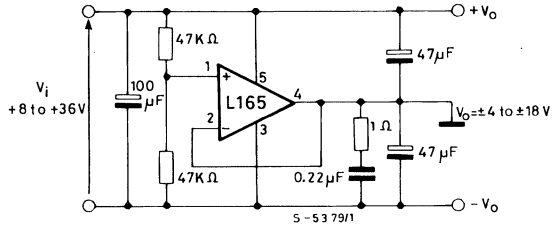
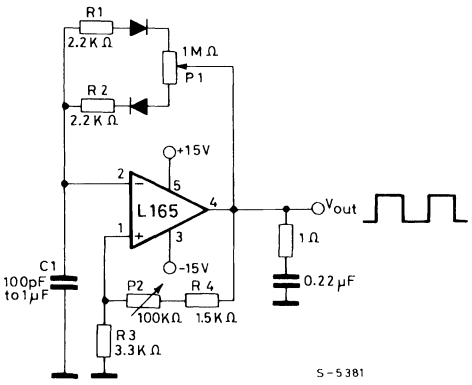


Figure 14 : Power squarewave oscillator with independent adjustments for frequency and duty-cycle.



P1 : duty-cycle adjust

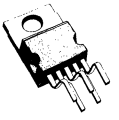
P2 : frequency adjust (f = 700 Hz with C1 = 10 nF, P2 = 100 KΩ, f = 25 Hz with C1 = 10 nF, P2 = 0)

ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

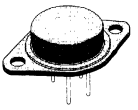
- ADJUSTABLE OUTPUT CURRENT UP TO 2 A (GUARANTEED UP TO T_j = 150 °C)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85 V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60 V, 10 ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

DESCRIPTION

The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in Pentawatt® package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60 V) make the L200 virtually blow-out proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.



Pentawatt®



TO–3 (4 lead)

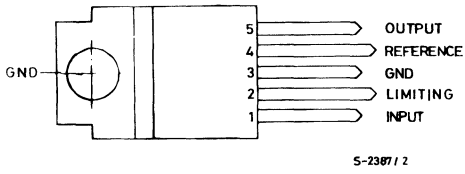
ABSOLUTE MAXIMUM RATINGS

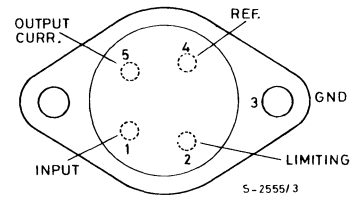
Symbol	Parameter	Value	Unit
V_i	DC Input Voltage	40	V
V_i	Peak Input Voltage (10 ms)	60	V
ΔV_{i-o}	Dropout Voltage	32	V
I_o	Output Current	internally limited	
P_{tot}	Power Dissipation	internally limited	
T_{stg}	Storage Temperature	– 55 to 150	°C
T_{op}	Operating Junction Temperature for L200C for L200	– 25 to 150 – 55 to 150	°C °C

THERMAL DATA

			TO–3	Pentawatt®
$R_{th\,j\text{-}case}$	Thermal Resistance Junction-case	Max	4 °C/W	3 °C/W
$R_{th\,j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35 °C/W	50 °C/W

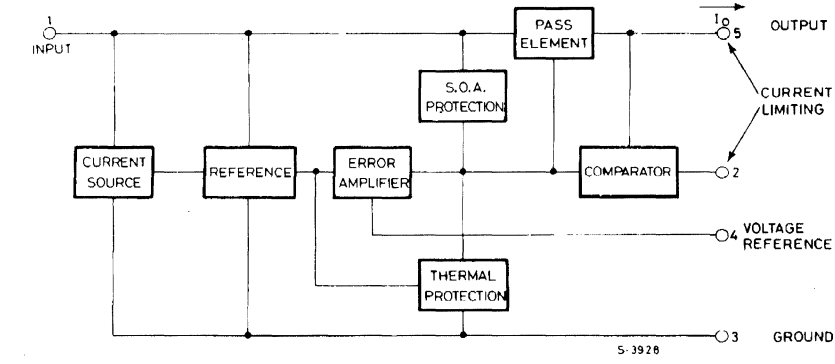
CONNECTION DIAGRAMS AND ORDER CODES (top views)





Type	Pentawatt®	TO–3
L200		L200 T
L200 C	L200 CH L200 CV	L200 CT

BLOCK DIAGRAM



APPLICATION CIRCUITS

Figure 1 : Programmable Voltage Regulator with Current Limiting.

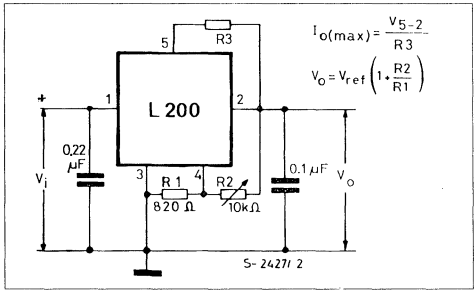
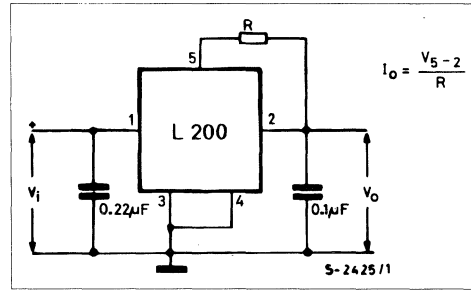
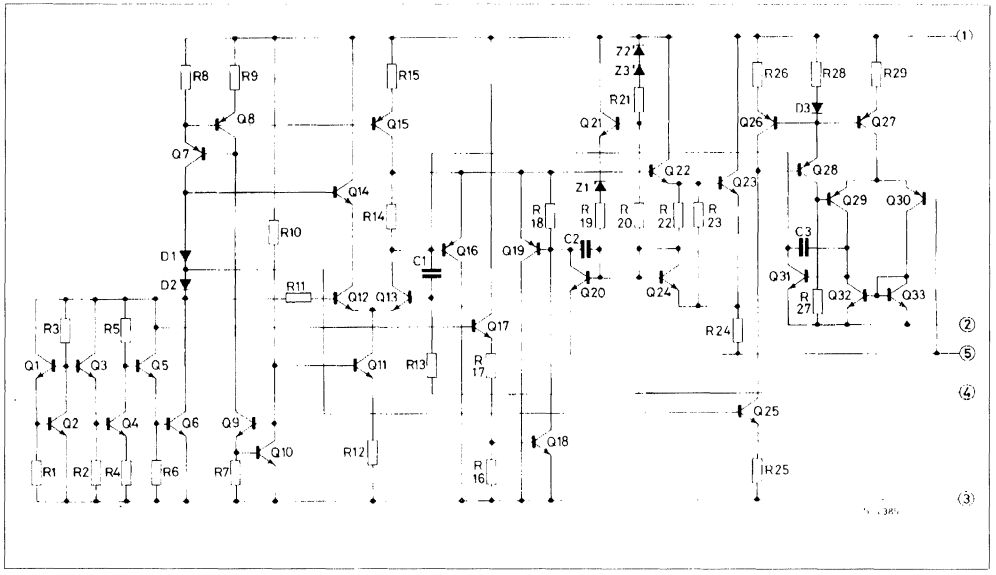


Figure 2 : Programmable Current Regulator.



SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VOLTAGE REGULATION LOOP						
I_d	Quiescent Drain Current (pin 3)	V_i = 20 V		4.2	9.2	mA
e_N	Output Noise Voltage	$V_o = V_{ref}$ I_o = 10 mA B = 1 MHz		80		μV
V_o	Output Voltage Range	I_o = 10 mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Voltage Load Regulation (note 1)	ΔI_o = 2 A ΔI_o = 1.5 A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line Regulation	V_o = 5 V V_i = 8 to 18 V	48	60		dB
SVR	Supply Voltage Rejection	V_o = 5 V I_o = 500 mA ΔV_i = 10 V_{pp} f = 100 Hz (note 2)	48	60		dB
ΔV_{i-o}	Droupout Voltage between Pins 1 and 5	I_o = 1.5 A $\Delta V_o \leq 2$ %		2	2.5	V
V_{ref}	Reference Voltage (pin 4)	V_i = 20 V I_o = 10 mA	2.64	2.77	2.86	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔV_{ref}	Average Temperature Coefficient of Reference Voltage	V_i = 20 V I_o = 10 mA for T_j = – 25 to 125 °C for T_j = 125 to 150 °C		– 0.25 – 1.5		mV/°C mV/°C
I_4	Bias Current at Pin 4			3	10	µA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$	Average Temperature Coefficient (pin 4)			– 0.5		%/°C
Z_o	Output Impedance	V_i = 10 V $V_o = V_{ref}$ I_o = 0.5 A f = 100 Hz		1.5		mΩ

CURRENT REGULATION LOOP

V_{SC}	Current Limit Sense Voltage between Pins 5 and 2	V_i = 10 V $V_o = V_{ref}$ I_5 = 100 mA	0.38	0.45	0.52	V
$\frac{\Delta V_{SC}}{\Delta T \cdot V_{SC}}$	Average Temperature Coefficient of V_{SC}			0.03		%/°C
$\frac{\Delta I_o}{I_o}$	Current Load Regulation	V_i = 10 V ΔV_o = 3 V I_o = 0.5 A I_o = 1 A I_o = 1.5 A		 1.4 1 0.9		 % % %
I_{SC}	Peak Short Circuit Current	$V_i - V_o$ = 14 V (pins 2 and 5 short circuited)			3.6	A

Note 1 : A load step of 2 A can be applied provided that input-output differential voltage is lower than 20 V (see Figure 3).

Note 2 : The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Figure 3 : Typical Safe Operating Area Protection.

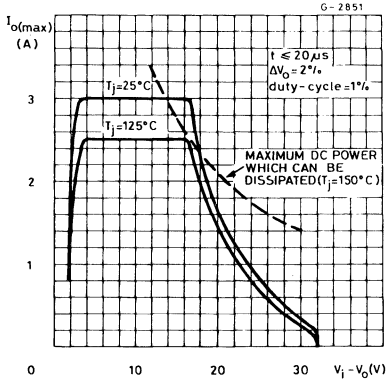


Figure 4 : Quiescent Current vs. Supply Voltage.

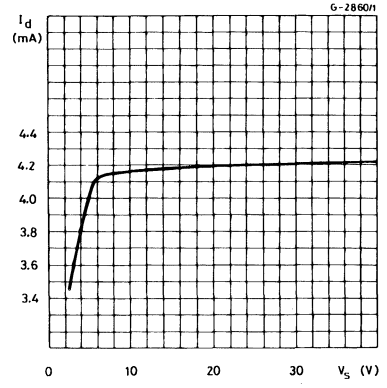


Figure 5 : Quiescent Current vs. Junction Voltage.

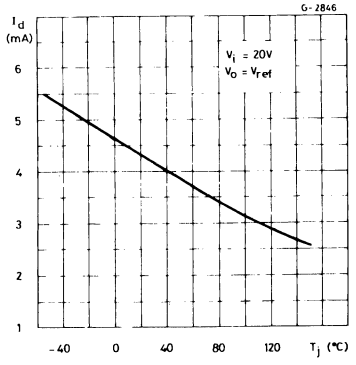


Figure 6 : Quiescent Current vs. Output Current.

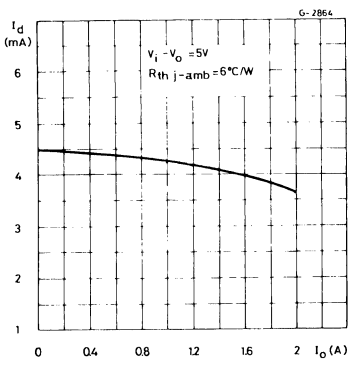


Figure 7 : Output Noise Voltage vs. Output Voltage.

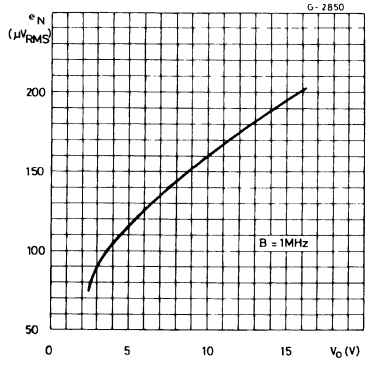


Figure 8 : Output Noise Voltage vs. Frequency.

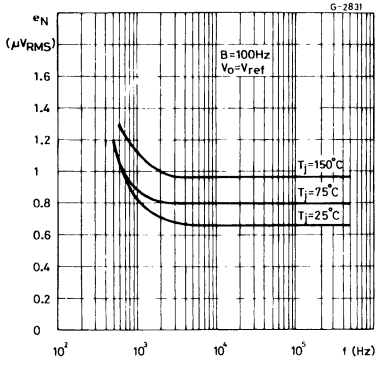


Figure 9 : Reference Voltage vs. Junction Temperature.

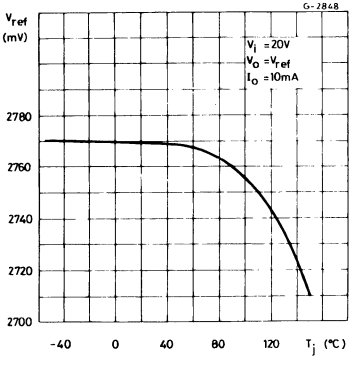


Figure 10 : Voltage Load Regulation vs. Junction Temperature.

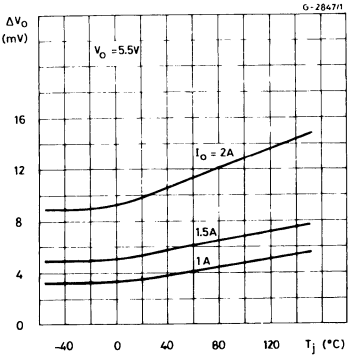


Figure 11 : Supply Voltage Rejection vs. Frequency.

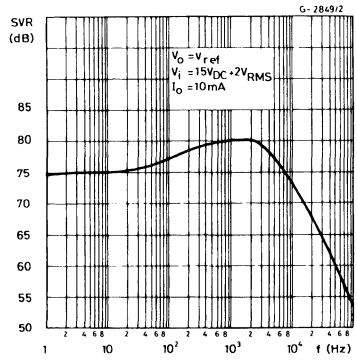


Figure 12 : Dropout Voltage vs. Junction Temperature.

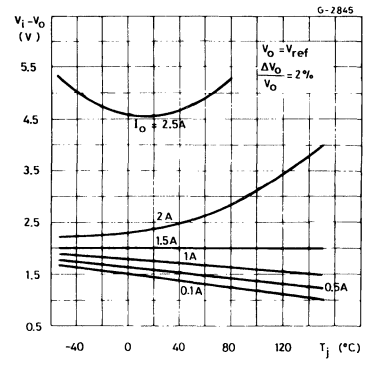


Figure 13 : Output Impedance vs. Frequency.

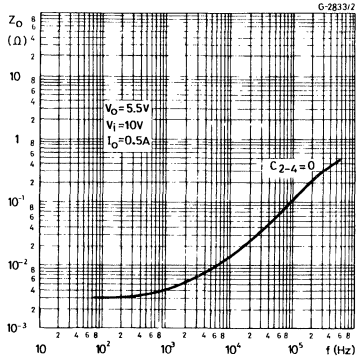


Figure 14 : Output Impedance vs. Output Current.

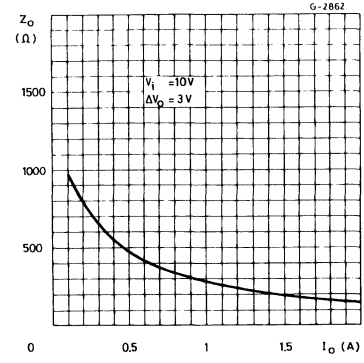


Figure 15 : Voltage Transient Response.

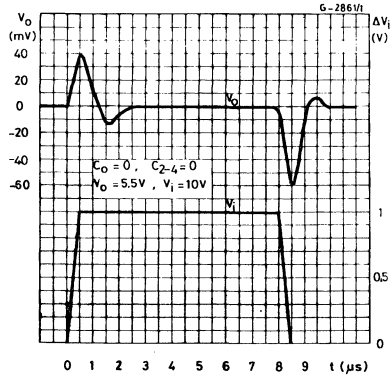


Figure 16 : Load Transient Response.

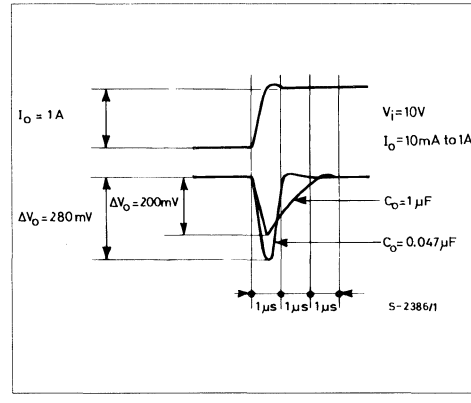


Figure 17 : Load Transient Response.

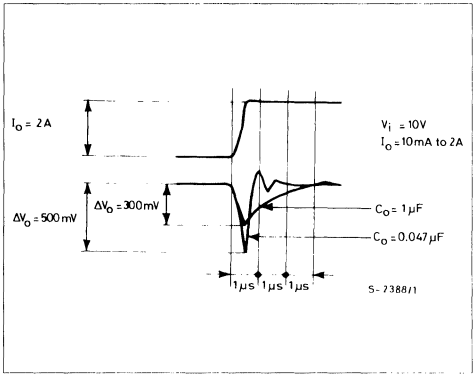
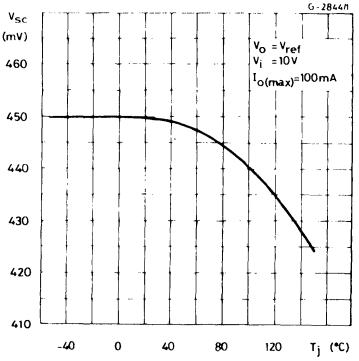


Figure 18 : Current Limit Sense Voltage vs. Junction Temperature.



APPLICATION CIRCUITS

Figure 19 : Programmable Voltage Regulator.

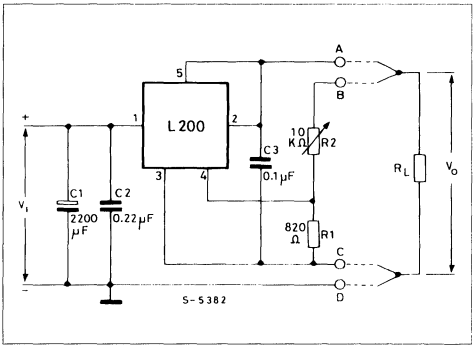


Figure 20 : P.C. Board and Components Layout of Figure 19.

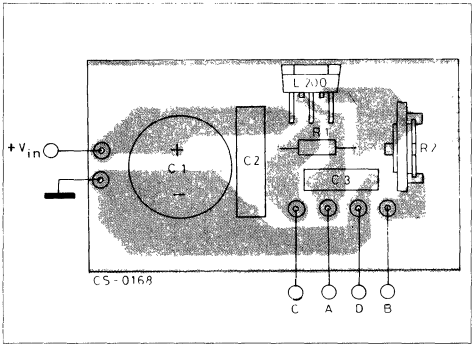


Figure 21 : High Current Voltage Regulator with Short Circuit Protection.

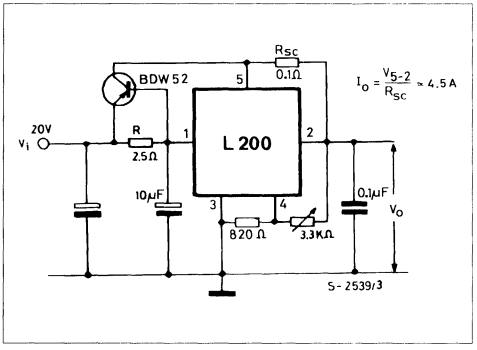


Figure 22 : Digitally Selected Regulator with Inhibit.

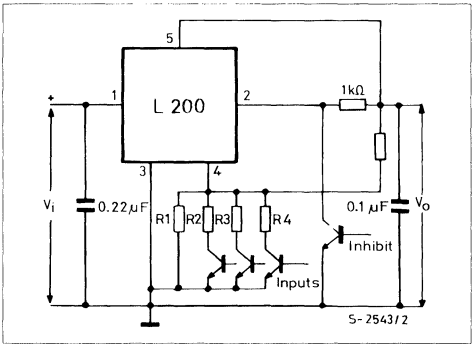
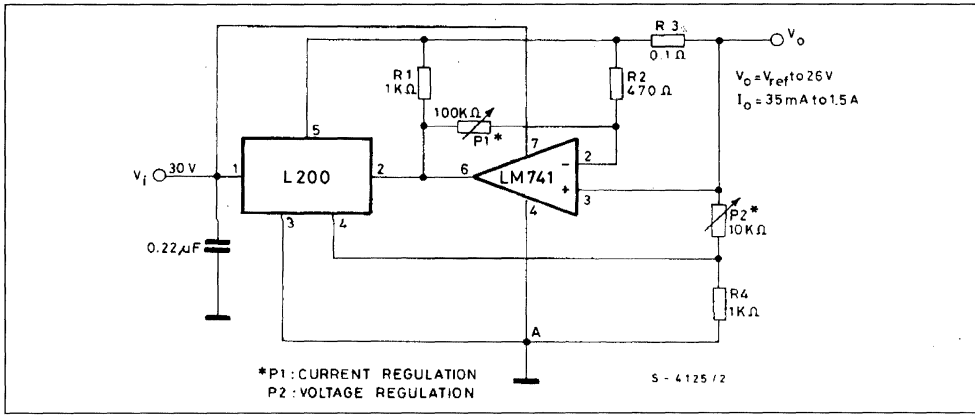


Figure 23 : Programmable Voltage and Current Regulator.



Note : Connecting point A to a negative voltage (for example – 3 V/10 mA) it is possible to extend the output voltage range down to 0 V and to obtain the current limiting down to this level (output short-circuit condition).

Figure 24 : High Current Regulator with NPN Pass Transistor.

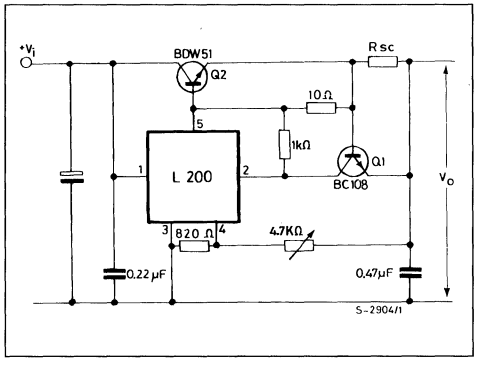
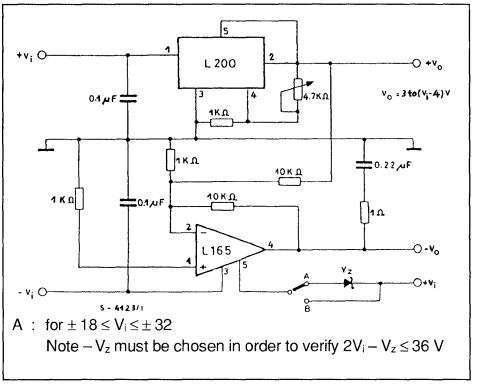


Figure 25 : High Current Tracking Regulator.



A : for $\pm 18 \leq V_i \leq \pm 32$

Note $-V_z$ must be chosen in order to verify $2V_i - V_z \leq 36$ V

Figure 26 : High Input and Output Voltage.

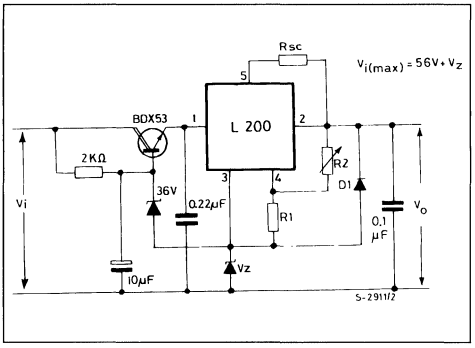
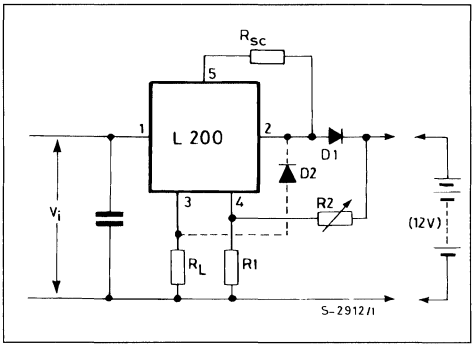


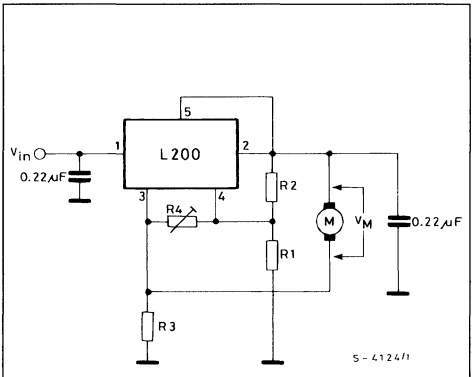
Figure 27 : Constant Current Battery Charger.



The resistors R_1 and R_2 determine the final charging voltage and R_{SC} the initial charging current. D_1 prevents discharge of the battery throught the regulator.

The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If R_L is in series with a bulb of 12 V/50 mA rating this will indicate incorrect connection.

Figure 28 : 30 W Motor Speed Control.



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot (1 + \frac{R_2}{R_1})$$

Figure 29 : Low Turn on.

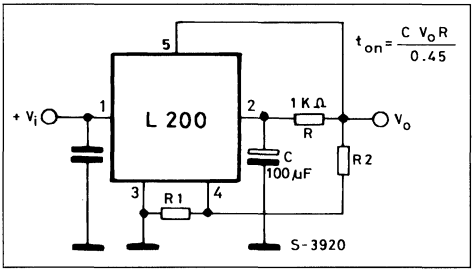
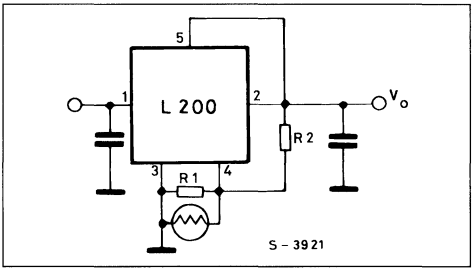


Figure 30 : Light Controller.

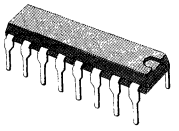


DUAL POWER OPERATIONAL AMPLIFIERS

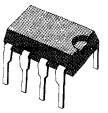
- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8)



Minidip Plastic

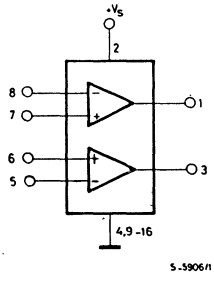
ORDERING NUMBERS:

L272 L272M

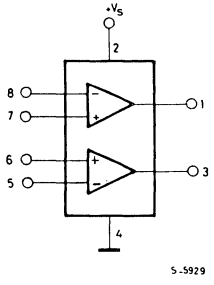
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 80°C$ **(L272)**, $T_{amb} = 50°C$ **(L272M)**	1	W
	$T_{case} = 75°C$ **(L272)**	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

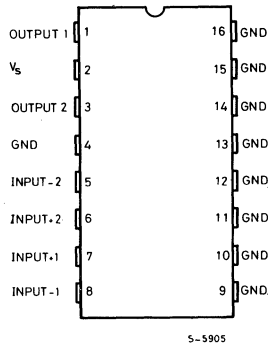


L272

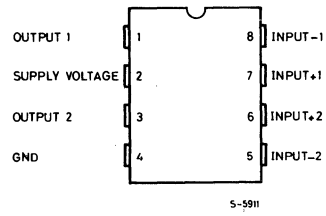


L272M

CONNECTION DIAGRAM
(Top view)

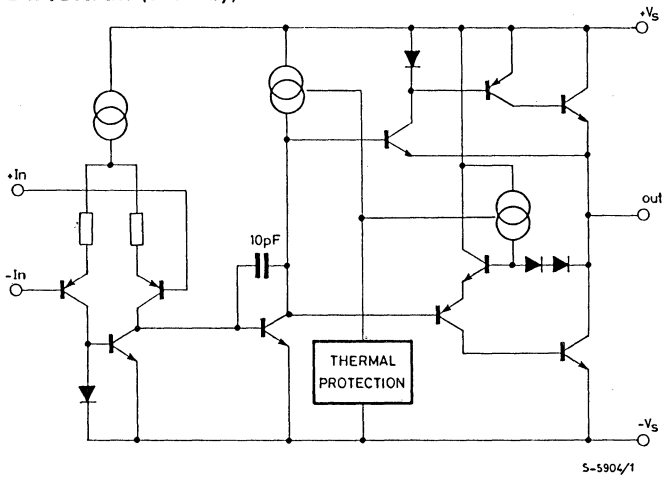


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_I	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

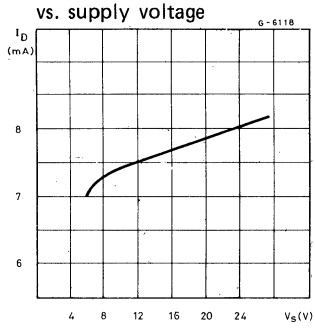


Fig. 2 - Quiescent drain current vs. temperature

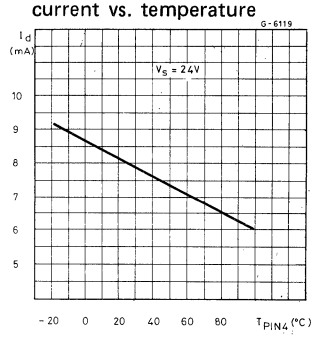


Fig. 3 - Open loop voltage gain

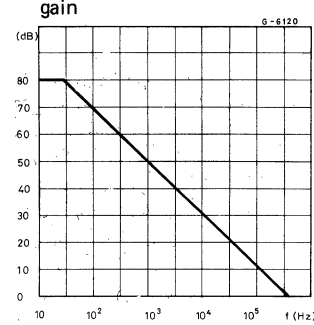


Fig. 4 - Output voltage swing vs. load current

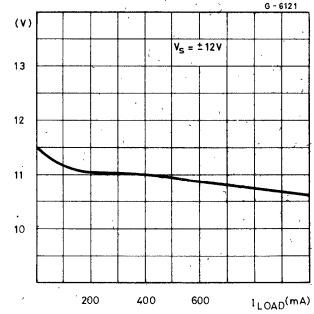


Fig. 5 - Output voltage swing vs. load current

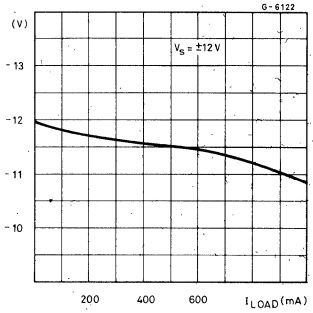


Fig. 6 - Supply voltage rejection vs. frequency

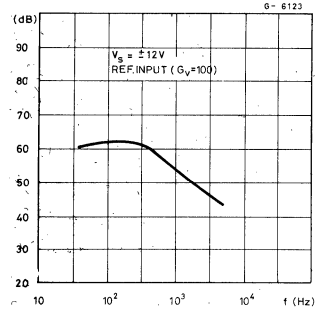


Fig. 7 - Channel separation vs. frequency

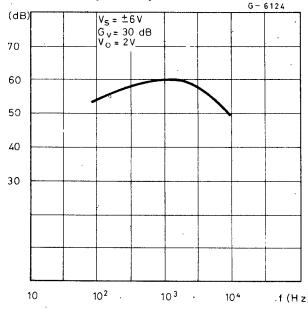
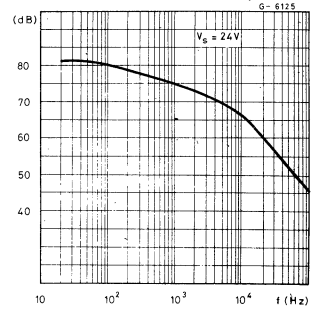


Fig. 8 - Common mode rejection vs. frequency



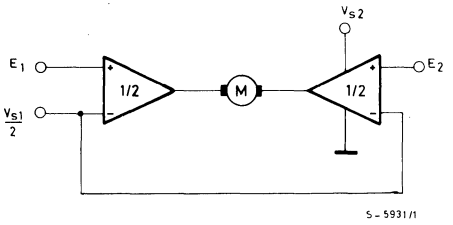
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

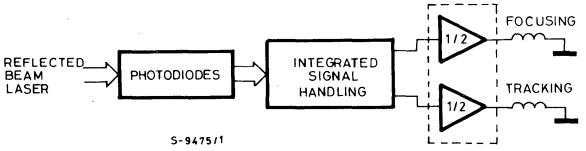


Fig. 11 - Capstan motor control in video recorders

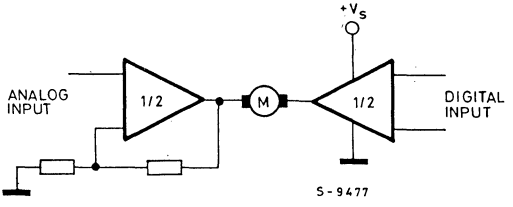
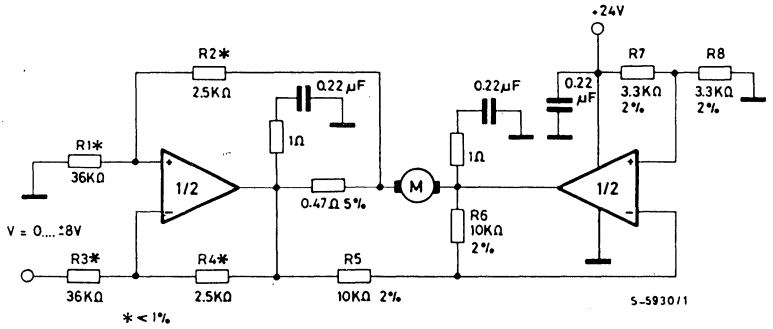


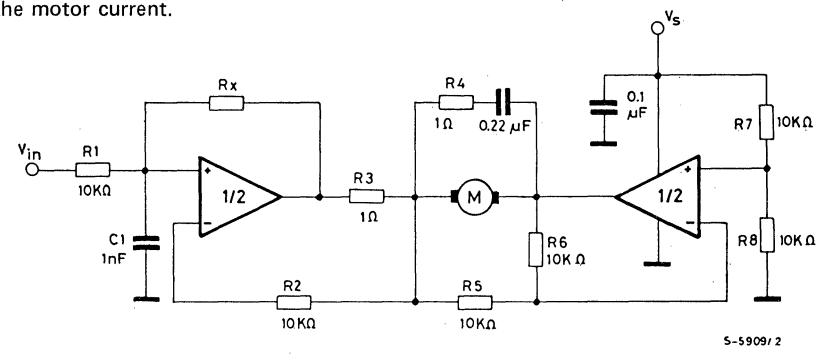
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_i - \frac{V_s}{2}\right) + |R_o|.\ I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.



SGS-THOMSON MICROELECTRONICS

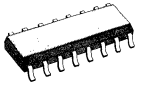
L272D

DUAL POWER OPERATIONAL AMPLIFIER

ADVANCE DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDWON

The L272D is a monolithic integrated circuit in SO-16 packages intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc. The high gain and high output power capability provide superior performance wheatever an operational amplifier/power booster combination is required.



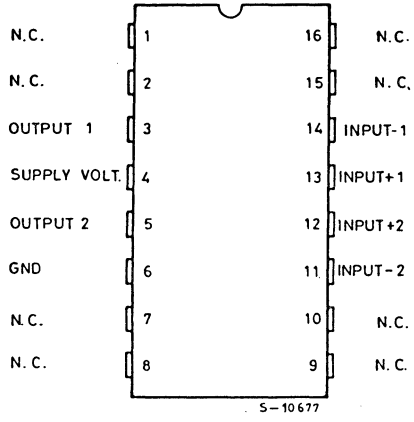
SO-16J

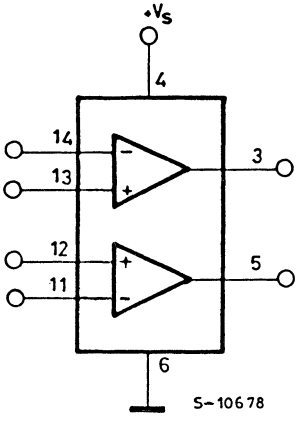
ORDERING NUMBER: L272D

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC Output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{case} = 90°C$	1.2	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

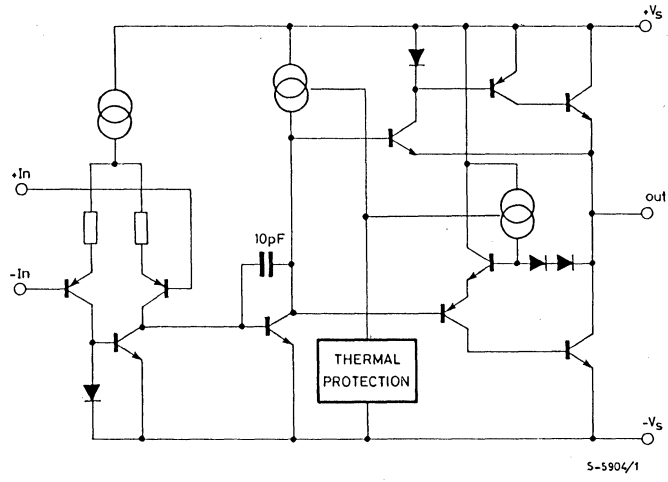
CONNECTION DIAGRAMS





This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

$R_{thj-alumina(*)}$	Thermal resistance junction-alumina	max 50	°C/W

(*) Thermal resistance junctions-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		8	12	mA
			V_s = 12V		7.5	11	mA
I_b	Input bias current				0.3	2.5	μA
V_{os}	Input offset voltage				15	60	mV
I_{os}	Input offset current				50	250	nA
SR	Slew rate				1		V/μs
B	Gain-bandwidth product				350		KHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		60	70		dB
		f = 1KHz			50		dB
e_N	Input noise voltage	B = 20KHz			10		μV
I_N	Input noise current	B = 20KHz			200		pA
CRR	Common Mode rejection	f = 1KHz		60	75		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	54	70 62 56		dB dB dB
V_o	Output voltage swing		I_p = 0.1A I_p = 0.5A	21	23 22.5		V V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB	V_s = 24V V_s = ± 6V		60 60		dB dB
d	Distortion	f = 1KHz V_s = 24V	G_v = 30dB R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

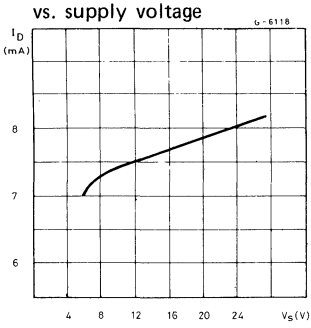


Fig. 2 - Quiescent drain current vs. temperature

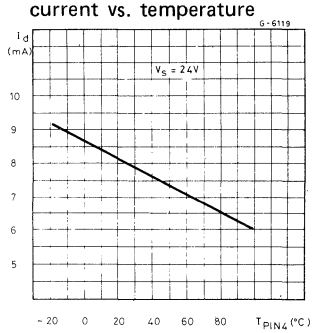


Fig. 3 - Open loop voltage gain

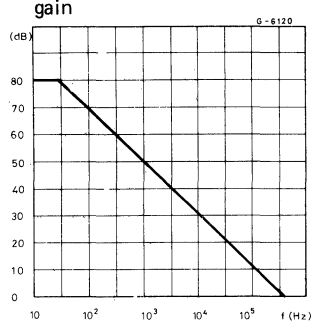


Fig. 4 - Output voltage swing vs. load current

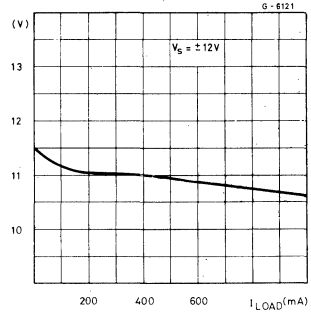


Fig. 5 - Output voltage swing vs. load current

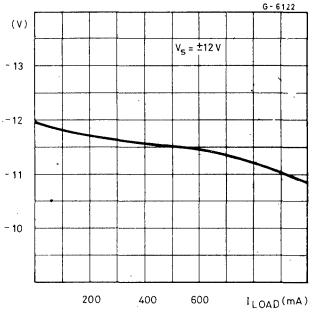


Fig. 6 - Supply voltage rejection vs. frequency

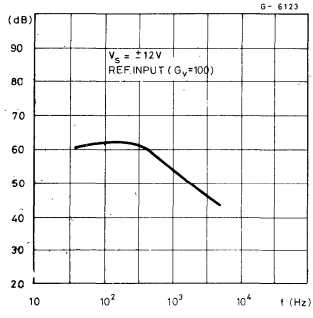


Fig. 7 - Channel separation vs. frequency

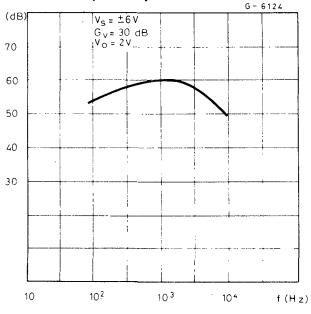
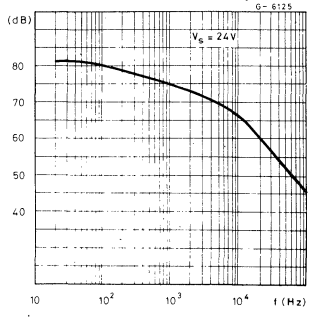


Fig. 8 - Common mode rejection vs. frequency



SGS-THOMSON MICROELECTRONICS

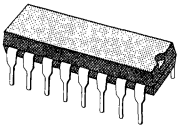
L290

TACHOMETER CONVERTER

The L290, a monolithic LSI circuit in a 16-lead dual inline plastic package, is intended for use with the L291 and L292 which together from a complete **3-chip DC motor positioning system** for applications such as carriage/daisy-wheel position control in typewriters.

The L290/1/2 system can be directly controlled by a microprocessor. The L290 integrates the following functions :

- tacho voltage generator (F/V converter)
- reference voltage generator
- position pulse generator



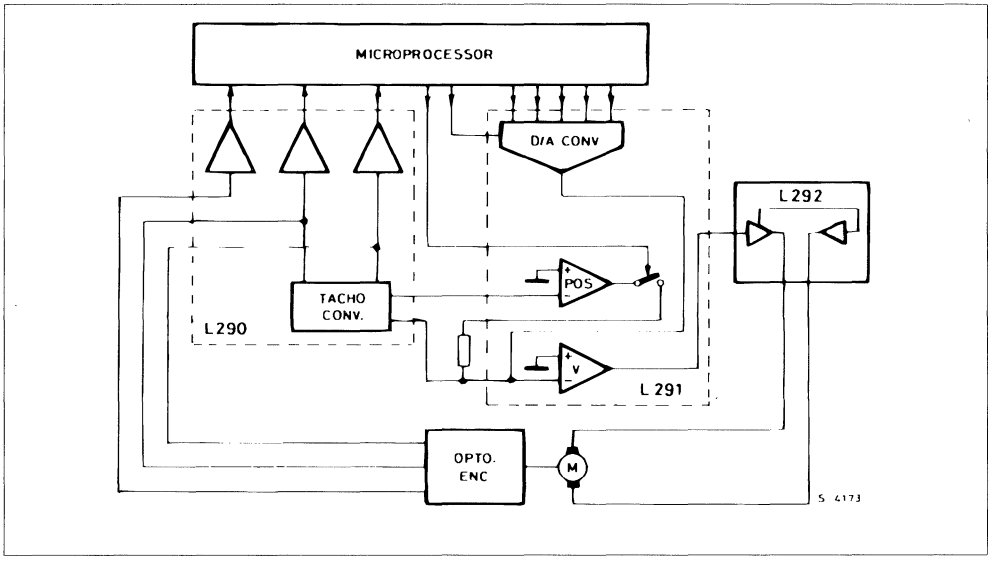
DIP-16 Plastic
(0.25)

ORDER CODE : L290B

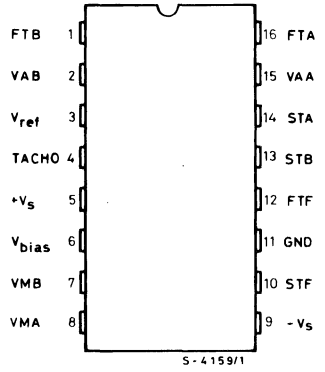
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 15	V
V_i (FTA, FTB, FTF)	Input Signals	± 7	V
P_{tot}	Total Power Dissipation T_{amb} = 70 °C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

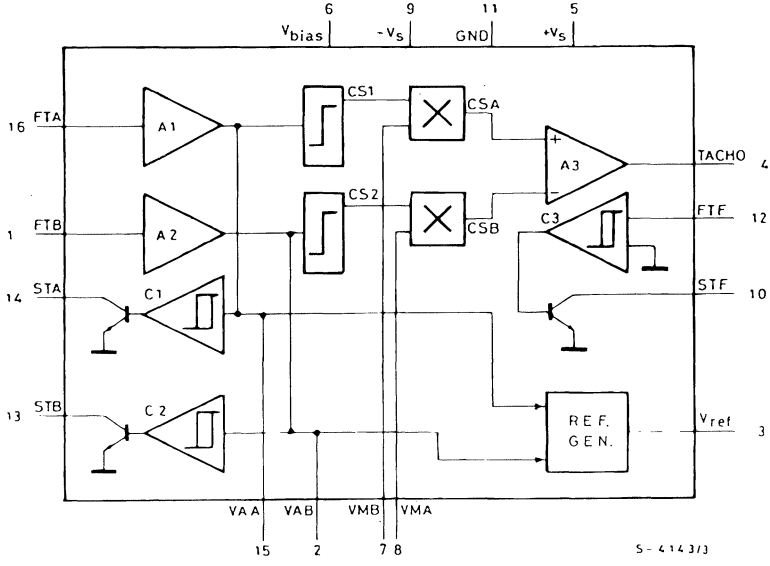
SYSTEM BLOCK DIAGRAM



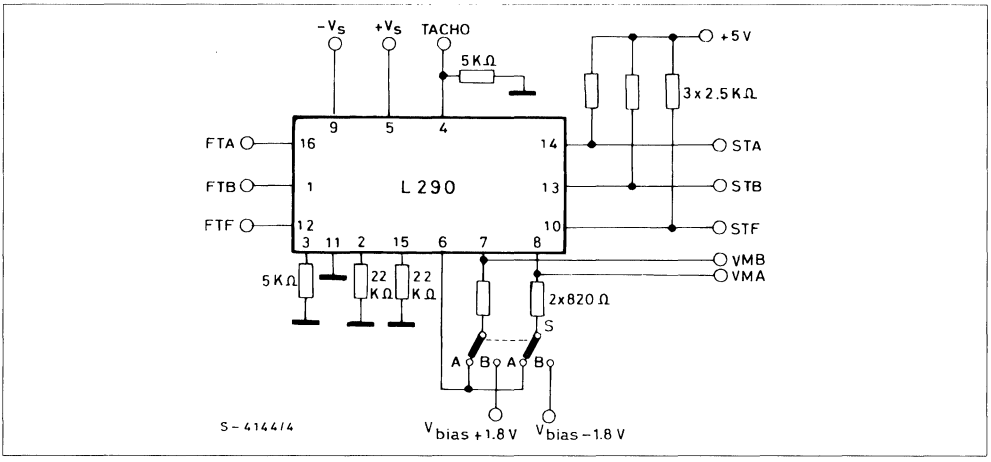
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, S in (A), $V_s = \pm 12$ V, $T_{amb} = 25$ °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 10		± 15	V
I_d	Quiescent Drain Current	$V_s = \pm 15$ V		13	20	mA

INPUT AMPLIFIERS (A_1 and A_2)

FTA, FTB	Input Signal from Encoder (pin 1, 16)	f_{max} = 20 KHz	± 0.4		± 0.6	V_p
V_{os}	Output Offset Voltage (pin 2, 15)	FTA = FTB = 0 V			± 55	mV
I_b	Input Bias Current (pin 1, 16)			0.15		µA
G_v	Voltage Gain	f = 10 KHz FTA = FTB = ± 0.6 V_p	22	23	24	dB
V_0	Output Voltage Swing (pin 2, 15)	FTA = FTB = ± 1V_p	± 9.5			V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
COMPARATORS WITH HYSTERESIS (C_1, C_2, and C_3)						
V_{THP} (°)	Positive Threshold Voltage (pin 2, 12, 15)	C_1 and C_2	550		850	mV
		C_3	700		900	mV
V_{THN} (°°)	Negative Threshold Voltage (pin 2, 12, 15)	C_1 and C_2	55		175	mV
		C_3	570		830	mV
ΔFTF	Threshold Hysteresis	C_3	72		120	mV
V_L	Output Voltage (low level) (pin 10, 13, 14)	I_0 = 2 mA FTA = FTB = FTF = 0 V		0.2	0.4	V
I_{leak}	(pins 10, 13, 14)	FTA = FTB = 0.5 V V_{CE} = 5 V FTF = 1 V			1	µA
REFERENCE GENERATOR						
V_{ref}	DC Reference Voltage (pin 3)	FTA = FTB = ± 0.5 V_p (*) I_{ref} = 1 mA	4.5	5	5.5	V
I_{ref}	Output Current (pin 3)				1.4	mA
"TACHO" AMPLIFIER (A_3)						
V_{os}	Output Offset Voltage (pin 4)	FTA = ± 15 mV FTB = 0.5 V			± 80	mV
V_o	DC Output Voltage (pin 4)	FTA = FTB = ± 0.5 V_p (**) V_{01}	5.4	6	6.6	V
		VMA = VMB = ± 1.25 V_p (***) V_{02}	− 5.4	− 6	− 6.6	
ΔV_0		V_{01} + V_{02}	− 150		+ 150	mV
V_0	Output Voltage Swing (pin 4)	FTA = FTB = 0.5 V	9			V
		Sin (B) FTA = FTB = − 0.5 V	− 9			
V_{MA} V_{MB}	Multiplier Input Voltage (pin 7, 8)			± 1.25	± 1.7	V_p
V_{bias}	Bias Voltage (pin 6)	FTA and FTB Floating	− 6.5		− 8	V

(*) : FTA = FTB = FTF = 0 / 1V

(**) : FTA = FTB = FTF = 1V \ 0

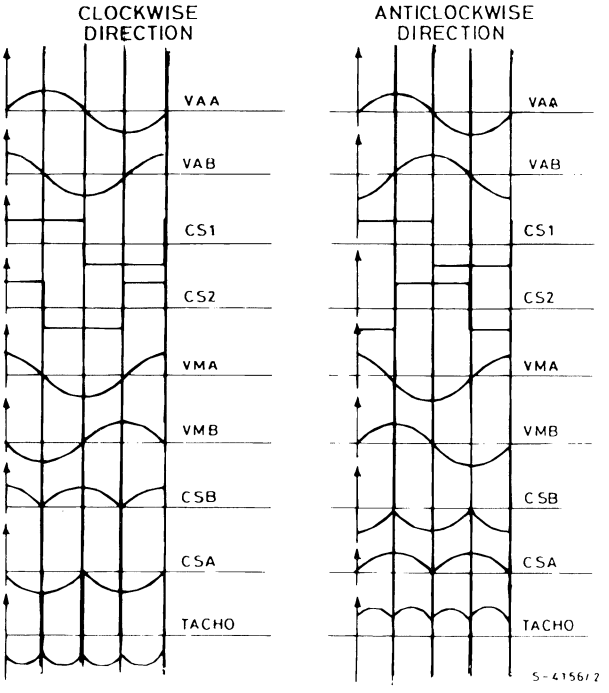
Note : Phase relationship between the signals :

* FTA : 0° FTB : 90°

** FTA : 0° FTB : − 90° V_{MA} = 90° V_{MB} = 0°

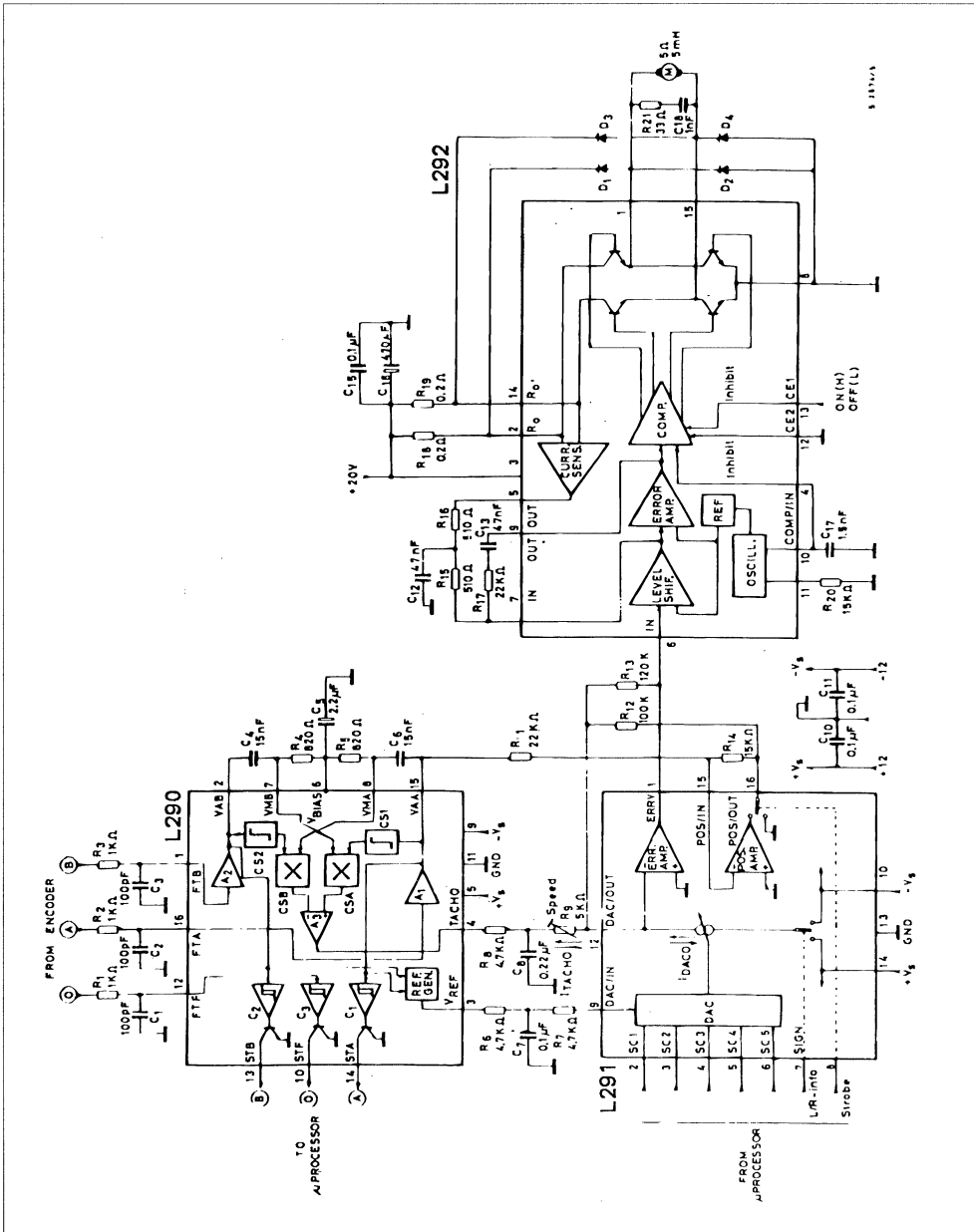
*** FTA : 0° FTB : 90° V_{MA} = 90° V_{MB} = 180°

WAVEFORMS (Neglecting threshold voltage level of the comparators).



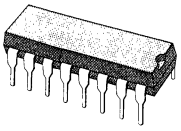
SYSTEM DESCRIPTION : refer to the L292 data sheet.

Figure 1 : Complete application circuit.



5 BIT – D/A CONVERTER AND POSITION AMPLIFIER

- 5 BIT D/A CONVERTER (1/2 LSB MAX LINEARITY ERROR) ;
- ERROR AMPLIFIER ;
- POSITION AMPLIFIER.



DIP-16
(Plastic 0.25)

ORDER CODE : L291B

DESCRIPTION

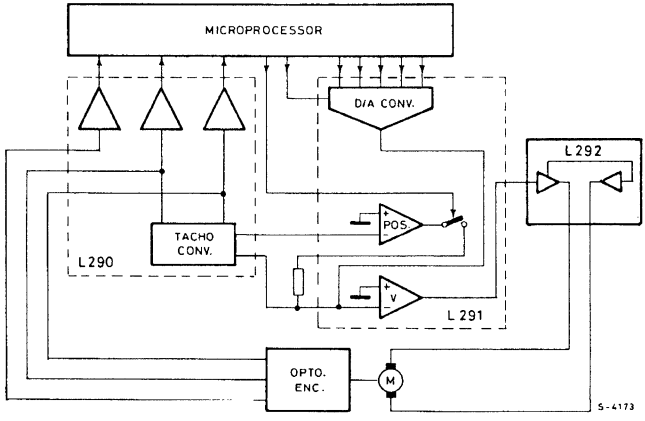
The L291, a monolithic LSI circuit in a 16-lead dual in-line plastic package, is intended for use with the L290 and L292 to form a complete 3 chip DC motor positioning system for applications such as carriage/daisy-wheel position control in typewriters.

The L290/291/292 system can be directly controlled by a microprocessor.

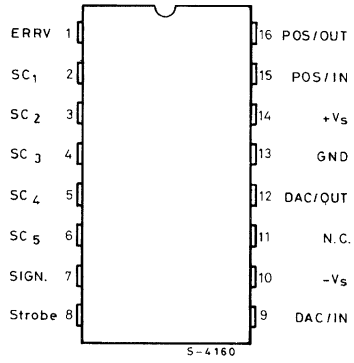
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 15	V
P_{tot}	Total Power Dissipation T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

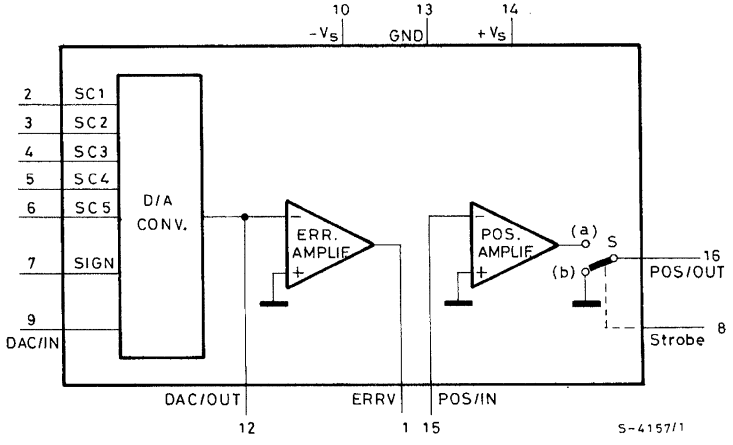
SYSTEM BLOCK DIAGRAM



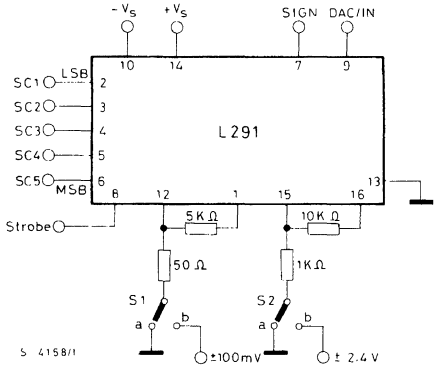
CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (refer to the circuit, S1 and S2 in (a), V_S = ± 12 V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		± 10		± 15	V
I_d	Quiescient Drain Current			6.5	10	mA

POSITION AMPLIFIER

V_{strobe}	Enable Voltage Level	V_L(S in (a)) *	0		0.8	V
		V_H(S in (b)) *	2.4		+ V_S	V
V_{os}	Output Offset Voltage (pin 16)	$V_{strobe} = V_L$; G_V = 20 dB			± 50	mV
I_b	Input Bias Current (pin 15)	$V_{strobe} = V_L$			0.3	µA
V_o	Output Voltage Swing (pin 16)	$V_{strobe} = V_L$; S2 in(b) ; V_S = ± 10.8 V	± 9			V
V_R	Residual Output Voltage (pin 16)	$V_{strobe} = V_H$			± 20	mV

* See block diagram and the note for Position Amplifier.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
D/A CONVERTER						
I_{ref}	Current Reference Input Range (pin 9)		0.3		1.2	mA
V_{os}	Current Reference Offset Voltage (pin 9)	I_{ref} = 0.3 to 1.2 mA All Inputs High			± 20	mV
I_o	Output Current Range (pin 12)				1.4	mA
I_o	Output Current (pin 12)	I_{ref} = 0.722 mA SC1 to SC5 = L SIGN = L(I_{o1})	− 1.358	− 1.4	− 1.442	mA
		SIGN = H(I_{o2})	+ 1.358	+ 1.4	+ 1.442	
ΔI_o		$I_{o1} + I_{o2}$	− 21		+ 21	µA
	Linearity Error	I_{ref} = 0.722 mA			1.61	%FS
I_{os}	Pin 12 Output Offset Current (including Error Amplifier bias current)	All Inputs High			± 0.4	µA
V_L	Low Voltage Level (digital inputs)	SC1 = LSB	0		0.8	V
V_H	High Voltage Level (digital inputs)	SC5 = MSB	2.4		+ V_S	V
I_L	Digital Inputs Current (low state)	V_L = 0.4V			− 50	µA
I_H	Digital Inputs Current (high state)	V_H = + V_S			1	µA
ERROR AMPLIFIER						
V_{os}	Output Offset Voltage (pin 1)	I_{ref} = 0.5 mA ; All Inputs High G_v = 40 dB			± 200	mV
I_o	Output Current (pin 1)				± 5	mA
V_o	Output Voltage Swing (pin 1)	All Inputs High S1 in (b) ; R_L = 10 KΩ	± 7.4		± 8.4	Vp

D/A CONVERTER

The L291 contains a 5-bit D/A converter accepting a binary code and generating a bipolar output current, the polarity of which depends on the SIGN input. The amplitude of the output current is a multiple of a reference current I_{ref}.

The maximum output current is

$$I_{FS} = \pm \frac{31}{16} I_{ref}$$

The following table shows the value of I_o for different input codes. Note that the input bits are active low.

DIGITAL INPUT WORD						Output Current I_o
SIGN	SC5 MSB	SC4	SC3	SC2	SC1 LSB	
L	L	L	L	L	L	$-\frac{31}{16} I_{ref}$
L	H	H	H	H	L	$-\frac{1}{16} I_{ref}$
X	H	H	H	H	H	O
H	H	H	H	H	L	$+\frac{1}{16} I_{ref}$
H	L	L	L	L	L	$+\frac{31}{16} I_{ref}$

X = indifferent
L = low
H = high

This D/A converter has a maximum linearity error equal to ± 1/2 LSB (or ± 1.61% Full Scale) ; that guarantees its monotonicity.

ERROR AMPLIFIER

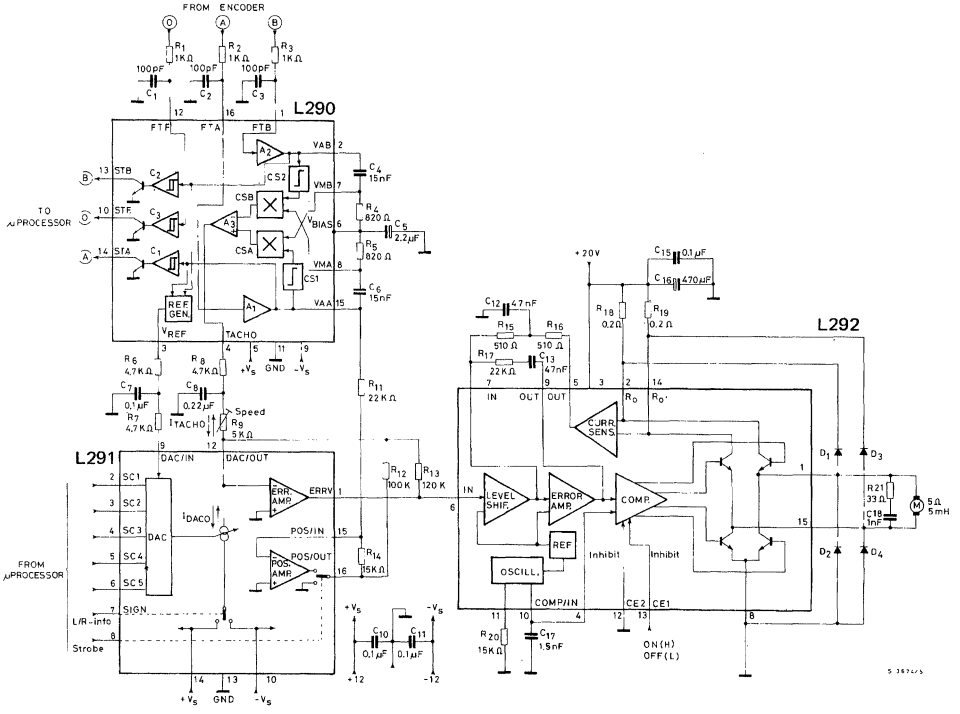
In order to have a good stability, the Error Amplifier must work with a closed loop gain greater or equal than 20 dB.

POSITION AMPLIFIER

It is inserted by means of the strobe signal, TTL and microprocessor compatible. Its output is connected to pin 16 when V_{strobe} = Low ; pin 16 is grounded for V_{strobe} = High.

SYSTEM DESCRIPTION : refer to the L292 data sheet.

Figure 1 : Complete Application Circuit.



D1 to D4 : { $V_F \leq 1.2V$ @ I = 2A
trr ≤ 200 ns

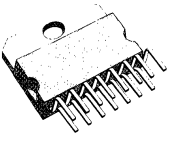
SWITCH–MODE DRIVER FOR DC MOTORS

- DRIVING CAPABILITY : 2 A, 36 V, 30 KHz
- 2 LOGIC CHIP ENABLE
- EXTERNAL LOOP GAIN ADJUSTEMENT
- SINGLE POWER SUPPLY (18 TO 36 V)
- INPUT SIGNAL SYMMETRIC TO GROUND
- THERMAL PROTECTION

DESCRIPTION

The L292 is a monolithic LSI circuit in 15-lead Multiwatt ® package. It is intended for use, together with L290 and L291, as a complete **3-chip motor positioning system** for applications such as carriage/daisy-wheel position control in typewrites.

The L290/1/2 system can be directly controlled by a microprocessor.



Multiwatt 15

ORDER CODE : L292

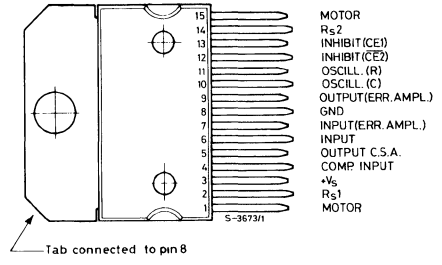
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Power Supply	36	V
V_i	Input Voltage	– 15 to + V_s	V
$V_{inhibit}$	Inhibit Voltage	0 to V_s	V
I_o	Output Current	2.5	A
P_{tot}	Total Power Dissipation (T_{case} = 75 °C)	25	W
T_{stg}	Storage and Junction Temperature	– 40 to + 150	°C

TRUTH TABLE

Vinhibit		Output Stage Condition
Pin 12	Pin 13	
L	L	Disabled
L	H	Normal Operation
H	L	Disabled
H	H	Disabled

CONNECTION DIAGRAM (top view)



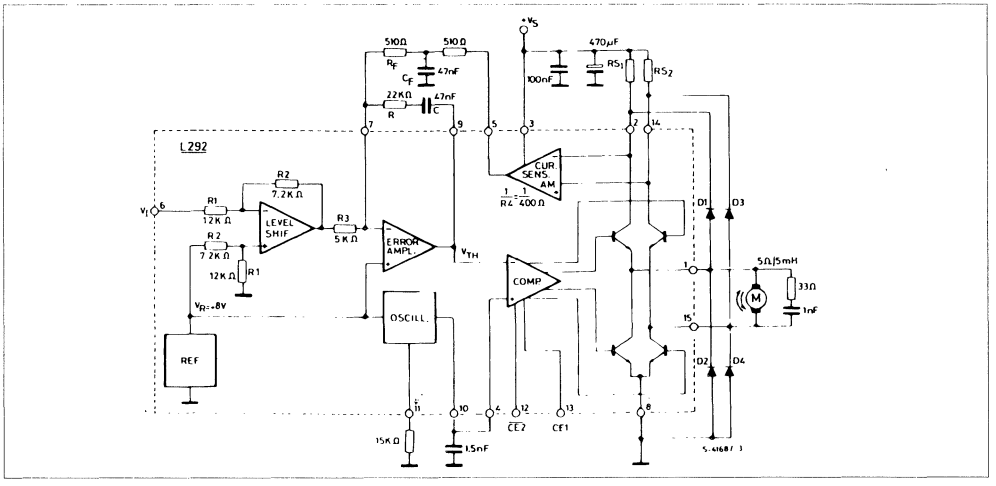
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 36 V, T_{amb} = 25 °C, f_{osc} = 20 KHz unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			18		36	V
I_d	Quiescent Drain Current	V_s = 20 V (offset null)			30	50	mA
V_{os}	Input Offset Voltage (pin 6)		I_o = 0			± 350	mV
$V_{inh.}$	Inhibit Low Level (pin 12,13)					2	V
	Inhibit High Level (pin 12,13)			3.2			V
$I_{inh.}$	Low Voltage Condition	$V_{inh.}$(L) = 0.4 V				− 100	µA
	High Voltage Conditions	$V_{inh.}$(H) = 3.2 V				10	µA
I_i	Input Current (pin (6)	V_I = − 8.8 V				− 1.8	mA
		V_I = + 8.8 V				0.5	mA
V_I	Input Voltage (pin 6)	$R_{S1} = R_{S2}$ = 0.2 Ω	I_o = 2 A		9.1		V
			I_o = −2 A		− 9.1		V
I_o	Output Current	V_I = ± 9.8 V $R_{S1} = R_{S2}$ = 0.2 Ω		± 2			A
V_D.	Total Drop Out Voltage	(inluding sensing resistors)	I_o = 2 A			5	V
			I_o = 1 A			3,5	V
V_{RS}	Sensing Resistor Voltage Drop	T_j = 150 °C	I_o = 2 A			0.44	V
$\frac{I_o}{V_I}$	Transconductance	$R_{S1} = R_{S2}$ = 0.2 Ω		205	220	235	mA / V
		$R_{S1} = R_{S2}$ = 0.4 Ω			120		mA / V
f_{osc}	Frequency Range (pin 10)			1		30	KHz

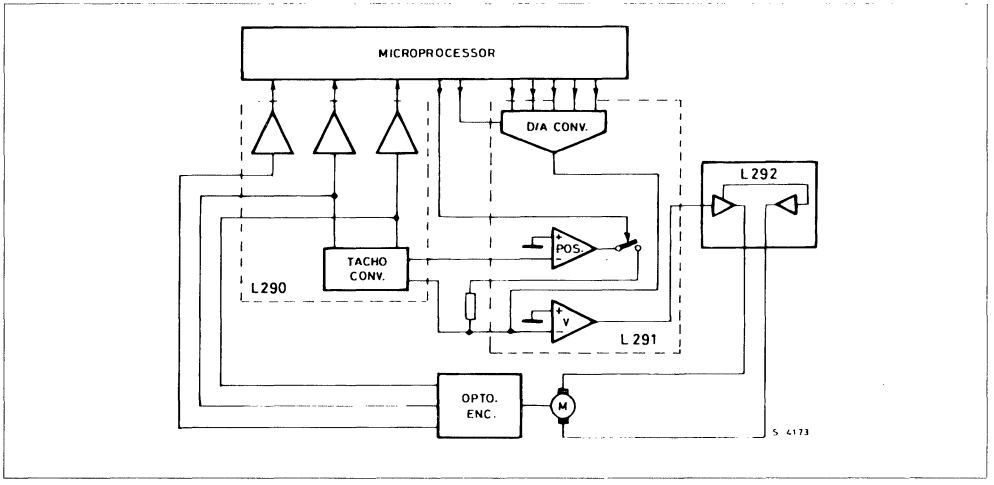
BLOCK DIAGRAM AND TEST CIRCUIT



SYSTEM DESCRIPTION

The L290, L291 and L292 are intended to be used as a 3-chip microprocessor controlled positioning system. The devices may be used separately - particularly the L292 motor driver - but since they will usually be used together, a description of a typical L290/1/2 system follows.

Figure 1 : System Block Diagram.



The system operates in two modes to achieve high speed, high-accuracy positioning.

Speed commands for the system originate in the microprocessor. It is continuously updated on the motor position by means of pulses from the L290 tachometer chip, which in turn gets its information from the optical encoder. From this basic input, the microprocessor computes a 5-bit control word that sets the system speed dependent on the distance to travel.

When the motor is stopped and the microprocessor orders it to a new position, the system operates initially in an open-loop configuration as there is no feedback from the tachometer generator. Therefore maximum current is fed to the motor. As maximum speed is reached, the tachometer chip output backs off the processor signal thus reducing accelerating torque. The motor continues to run at top speed but under closed-loop control

As the target position is approached, the microprocessor lowers the value of the speed-demand word ; this reduces the voltage at the main summing point, in effect braking the motor. The braking is applied progressively until the motor is running at minimum speed.

At that time, the microprocessor orders a switch to the position mode, (strobe signal at pin 8 of L291) and within 3 to 4 ms the L292 drives the motor to a null position, where it is held by electronic "detenting".

The mechanical/electrical interface consists of an optical encoder which generates two sinusoidal signals 90° out of phase (leading according to the motor direction) and proportional in frequency to the speed of rotation. The optical encoder also provides an output at one position on the disk which is used to set the initial position.

The opto encoder signals, FTA and FTB are filtered by the networks R_2 C_2 and R_3 C_3 (referring to Fig.4) and are supplied to the FTA/FTB inputs on the L290.

The main function of the L290 is to implement the following expression :

$$\text{Output signal (TACHO)} = \frac{dV_{AB}}{dt} \cdot \frac{FTA}{|FTA|} - \frac{dV_{AA}}{dt} \cdot \frac{FTB}{|FTB|}$$

Thus the mean value of TACHO is proportional to the rotation speed and its polarity indicates the direction of rotation.

The above function is performed by amplifying the input signals in A_1 and A_2 to obtain V_{AA} and V_{AB} (typ.7 V_p). From V_{AA} and V_{AB} the external differentiator RC networks R_5 C_6 and R_4C_4 give the signals V_{MA} and V_{MB} which are fed to the multipliers.

The second input to each multiplier consists of the sign of the first input of the other multiplier before differentiation, these are obtained using the comparators C_{S1} and C_{S2}. The multiplier outputs, C_{SA} and C_{SB}, are summed by A_3 to give the final output signal TACHO. The peak-to-peak ripple signal of the TACHO can be found from the following expression :

$$V_{ripple\ p\text{-}p} = \frac{\pi}{4}(\sqrt{2} - 1) \cdot V_{thaco\ DC}$$

The max value of TACHO is :

$$V_{tacho\ max} = \frac{\pi}{4}\sqrt{2} \cdot V_{thaco\ DC}$$

Using the comparators C_1 and C_2 another two signals from V_{AA} and V_{AB} are derived — the logic signals STA and STB.
These signals are used by the microprocessor to determine the position by counting the pulses.
The L290 internal reference voltage is also derived from V_{AA} and V_{AB} :

$$V_{ref} = |V_{AA}| + |V_{AB}|$$

This reference is used by the D/A converter in the L291 to compensate for variations in input levels, temperature changes and ageing.
The "one pulse per rotation" opto encoder output is connected to pin 12 of the L290 (FTF) where it is squared to give the STF logic output for the microprocessor.
The TACHO signal and V_{ref} are sent to the L291 via filter networks R_8 C_8 R_9 and R_6 C_7 R_7 respectively. Pin 12 of this chip is the main summing point of the system where TACHO and the D/A converter output are compared.
The input to the D/A converter consists of 5 bit word plus a sign bit supplied by the microprocessor. The sign bit represents the direction of motor rotation. The (analogue) output of the D/A converter – DAC/OUT – is compared with the TACHO signal and the resulting error signal is amplified by the error amplifier, and subsequently appears on pin 1.
The ERRV signal (from pin 1, L291) is fed to pin 6 of the final chip, the L292 H-bridge motor-driver.This input signal is bidirectional so it must be converted to a positive signal because the L292 uses a single supply voltage. This is accomplished by the first stage - the level shifter, which uses an internally generated 8 V reference.
This same reference voltage supplies the triangle wave oscillator whose frequency is fixed by the external RC network (R_{20}, C_{17} - pins 11 and 10) where :

$$1f_{osc} = \frac{1}{2RC} \qquad (\text{with } R \geq 8.2\ K\Omega)$$

The oscillator determines the switching frequency of the output stage and should be in the range 1 to 30 KHz.
Motor currrent is regulated by an internal loop in the L292 which is performed by the resistors R_{18}, R_{19} and the differential current sense amplifier, the output of which is filtered by an external RC network and fed back to the error amplifier.
The choice of the external components in these RC network (pins 5, 7, 9) is determined by the motor type and the bandwidth requirements.The values shown in the diagram are for a 5Ω, 5 mH motor. (See L292 Transfer Function Calculation in Application Information).
The error signal obtained by the addition of the input and the current feedback signals (pin 7) is used to pulse width modulate the oscillator signal by means of the comparator. The pulse width modulated signal controls the duty cycle of the H-bridge to give an output current corresponding to the L292 input signal.
The interval between one side of the bridge switching off and the other switching on, τ , is programmed by C_{17} in conjunction with an internal resistor $R\tau$.
This can be found from :

$$\tau = R\tau \cdot C_{pin\ 10.}\ (C_{17} \text{ in the diagram})$$

Since $R\tau$ is approximately 1.5 KΩ and the recommended τ to avoid simultaneous conduction is 2.5 μs $C_{pin\ 10}$ should be around 1.5 nF.
The current sense resistors R_{18} and R_{19} should be high precision types (maximum tolerance ± 2 %) and the recommended value is given by :

$$R_{max} \cdot I_{o\ max} \leq 0.44\ V$$

It is possible to synchronize two L292's, if desired, using the network shown in fig. 2.
Finally, two enable inputs are provided on the L292 (pins 12 and 13-active low and high respectively).
Thus the output stage may be inhibited by taking pin 12 high or by taking pin 13 low. The output will also be inhibited if the supply voltage falls below 18 V.

The enable inputs were implemented in this way because they are intended to be driven directly by a microprocessor. Currently available microprocessors may generates spikes as high as 1.5 V during power-up. These inputs may be used for a variety of applications such as motor inhibit during reset of the logical system and power-on reset (see fig. 3).

Figure 2.

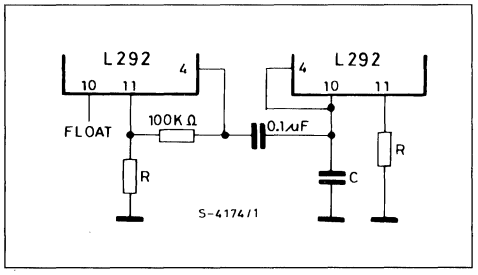


Figure 3.

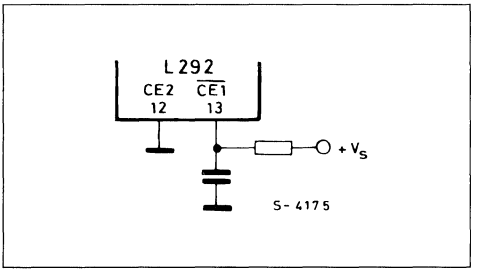
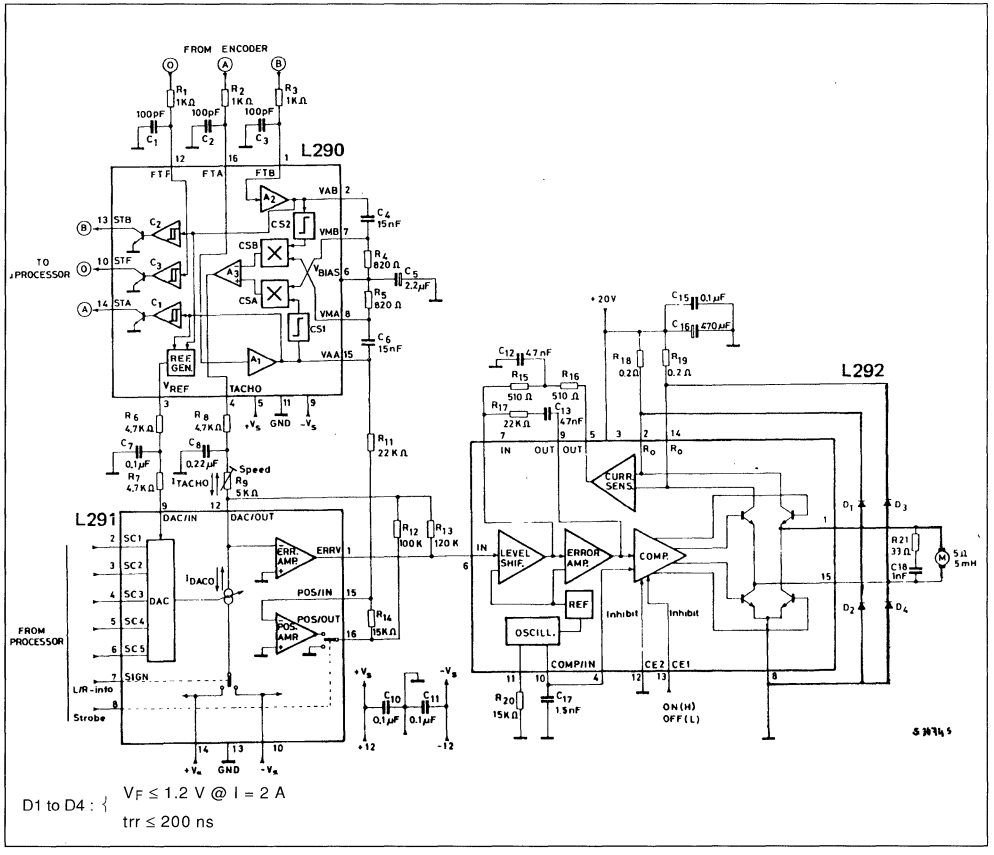


Figure 4 : Application Circuit.

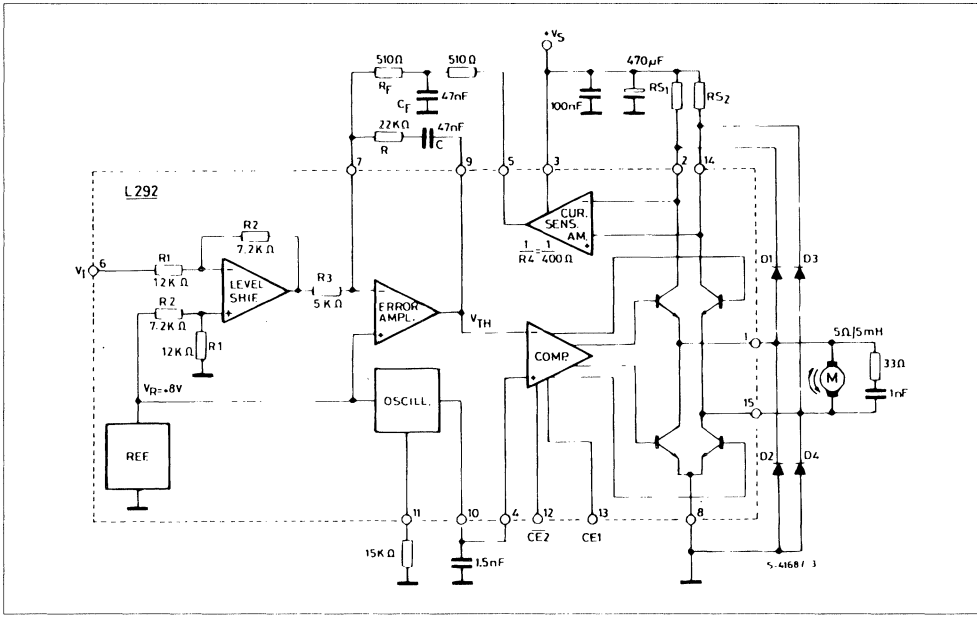


D1 to D4 : $V_F \leq 1.2$ V @ I = 2 A
trr ≤ 200 ns

APPLICATION INFORMATION

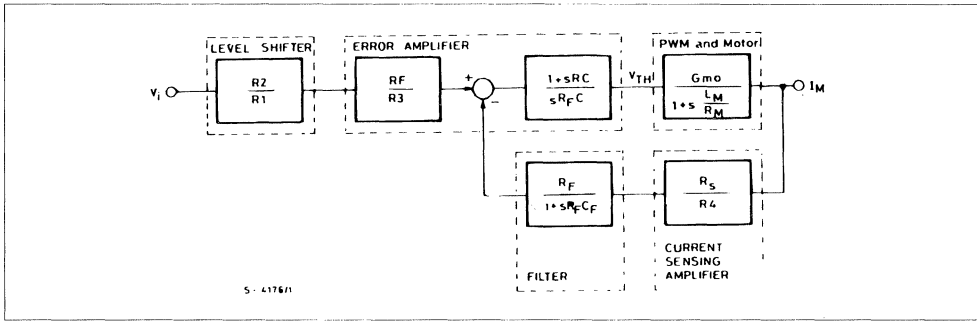
This section has been added in order to help the designer for the best choise of the values of external components.

Figure 5 : L292 Block Diagram.



The schematic diagram used for the Laplace analysis of the system is shown in fig. 6.

Figure 6.



$R_{S1} = R_{S2} = R_S$ (sensing resistors)

$\frac{1}{R_4} = 2.5 \cdot 10^{-3}\ \Omega$ (current sensing amplifier transconductance)

L_M = Motor inductance, R_M = Motor resistance, I_M = Motor current

$G_{mo} = \frac{I_M}{}\Big|_{s=0}$ (DC transfer function from the input of the comparator (V_{TH}) to the motor current(I_M)).

Neglecting the V_{CEsat} of the bridge transistors and the V_{BE} of the diodes :

$$G_{mo} = \frac{1}{R_M} \cdot \frac{2\,V_s}{V_R} \qquad (1)$$

where : V_s = supply voltage
V_R = 8 V (reference voltage)

DC TRANSFER FUNCTION

In order to be sure that the current loop is stable the following condition is imposed :

$$1 + sRC = 1 + s\,\frac{L_M}{R_M} \qquad \text{(pole cancellation)} \qquad (2)$$

$$\text{from which } RC = \frac{L_M}{R_M} \qquad \text{(Note that in practice R must greater than 5.6 K}\Omega\text{)}$$

The transfer function is then,

$$\frac{I_M}{V_I}(s) = \frac{R_2 R_4}{R_1 R_3} \cdot G_{mo} \cdot \frac{1 + s R_F C_F}{G_{mo} R_s + s R_4 C + s^2 R_F C_F R_4 C} \qquad (3)$$

In DC condition, this is reduced to

$$\frac{I_M}{V_I}(o) = \frac{R_2 R_4}{R_1 R_3} \cdot \frac{1}{R_s} = \frac{0.044}{R_s}\ \left[\frac{A}{V}\right] \qquad (4)$$

OPEN-LOOP GAIN AND STABILITY CRITERION

For $RC = L_M / R_M$, the open loop gain is:

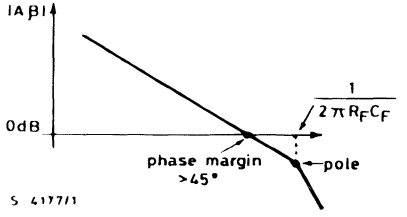
$$A\beta = \frac{1}{sR_F C} \cdot G_{mo} \cdot \frac{R_s}{R_4} \cdot \frac{R_F}{1 + s R_F C_F} = \frac{G_{mo} R_s}{R_4 C} \cdot \frac{1}{s(1 + s R_F C_F)} \qquad (5)$$

In order to achieve good stability, the phase margin must be greater than 45° when $|A\beta| = 1$.

That means that, at $f_F = \frac{1}{2\pi R_F C_F}$ must be $|A\beta| < 1$ (see fig .7), that is :

$$|A\beta|_f = \frac{1}{2\pi R_F C_F} = \frac{G_{mo} R_s}{R_4 C} \cdot \frac{R_F C_F}{\sqrt{2}} < 1 \qquad (6)$$

Figure 7 : Open Loop Frequency Response.



CLOSED-LOOP SYSTEM STEP RESPONSE

a) Small- signals analysis.

The transfer function (3) can be written as follows :

$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_s} \frac{1 + \frac{s}{2\xi\omega_o}}{1 + \frac{2\xi s}{\omega_o} + \frac{s^2}{\omega_o^2}} \qquad (7)$$

where $\omega_o = \sqrt{\frac{G_{mo} R_s}{R_4 C R_F C_F}}$ is the cutoff frequency

$$\xi = \sqrt{\frac{R_4 C}{4 R_F C_F G_{mo} R_s}}$$ is the dumping factor

By choosing the ξ value, it is possible to determine the system response to an input step signal.

Examples :

1) $\xi = 1$ from which

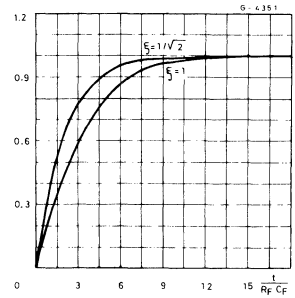
$$I_M(t) = \frac{0.044}{R_s} [\, 1 - e^{-\frac{t}{2R_F C_F}} (1 + \frac{t}{4R_F C_F}) \,] \,.\, V_i$$

(where V_i is the amplitude of the input step).

2) $\xi = \frac{1}{\sqrt{2}}$ from which

$$I_M(t) = \frac{0.044}{R_s} (1 - \cos\frac{t}{2R_F C_F} e^{-\frac{t}{2R_F C_F}}) V_i$$

Figure 8 : Small Signal Step Response (normalized amplitude vs. $t / R_F C_F$).



V_7 = 200 mV/div.
I_M = 100 mA/div.
t = 100 µs/div.
with V_I = 1.5 Vp.

It is possible to verify that the L292 works in "closed-loop" conditions during the entire motor current rise-time : the voltage at pin 7 (inverting input of the error amplifier) is locked to the reference voltage V_R, present at the non-inverting input of the same amplifier.
The previous linear analysis is correct for this example.
Decreasing the ξ value, the rise-time of the current decreases. But for a good stability, from relationship (6), the minimum value of ξ is :

$$\xi_{min} = \frac{1}{2\sqrt[4]{2}} \qquad \text{(phase margin} = 45^\circ\text{)}$$

b) Large signal reponse
The large step signal response is limited by slew-rate and inductive load.
In this case, during the rise-time of the motor current, the L292 works in open-loop condition.

CLOSED LOOP SYSTEM BANDWIDTH.
A good choice for ξ is the value $1/\sqrt{2}$. In this case :

$$\frac{I_M}{V_I}(s) = \frac{0.044}{R_S} \cdot \frac{1 + s R_F C_F}{1 + 2s R_F C_F + 2s^2 R_F^2 C_F^2} \qquad (8)$$

The module of the transfer function is :

$$\left|\frac{I_M}{V_I}\right| = \frac{0.044}{R_S} \cdot \frac{2\sqrt{1 + \omega^2 R_F^2 C_F^2}}{\sqrt{[(1 + 2\omega R_F C_F)^2 + 1] \cdot [(1 - 2\omega R_F C_F)^2 + 1]}} \qquad (9)$$

The cutoff frequency is derived by the expression (9) by putting $\left|\frac{I_M}{V_I}\right| = 0.707 \cdot \frac{0.044}{R_S}$ (–3 dB), from which :

$$\omega_T = \frac{0.9}{R_F C_F} \qquad f_T = \frac{0.9}{2\pi R_F C_F}$$

Example :

a) Data

- Motors charasteristics: $L_M = 5$ mH, $R_M = 5\ \Omega$, $L_M / R_M = 1$msec
- Voltage and current charasteristics: $V_s = 20$ V, $I_M = 2$ A, $V_I = 9.1$ V
- Closed loop bandwidth : 3 kHz.

b) Calculation

- From relationship (4) :

$$R_s = \frac{0.044}{I_M} V_I = 0.2\ \Omega$$

and from (1) :

$$G_{mo} = \frac{2V_S}{R_M V_R} = 1\ \Omega^{-1}$$

- RC = 1 msec [from expression (2)].
- Assuming $\xi = 1/\sqrt{2}$; from (7) follows :

$$\xi^2 = \frac{1}{2} = \frac{400\ C}{4R_F C_F . 0.2}$$

- The cutoff frequency is :

$$f_T = \frac{143 .10^{-3}}{R_F C_F} = 3\ \text{kHz}$$

c) Summarising

- $RC = 1.10^{-3}$ sec
- $\frac{1000\ C}{R_F C_F} = 1$
- $R_F C_F \cong 47\ \mu s$

} $C = 47$ nF, $R = 22\ K\Omega$

For $R_F = 510\ \Omega \rightarrow C_F = 92$ nF

SGS-THOMSON MICROELECTRONICS

L293B
L293E

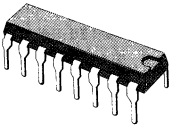
PUSH-PULL FOUR CHANNEL DRIVERS

- OUTPUT CURRENT 1A PER CHANNEL
- PEAK OUTPUT CURRENT 2A PER CHANNEL (NON REPETITIVE)
- INHIBIT FACILITY
- HIGH NOISE IMMUNITY
- SEPARATE LOGIC SUPPLY
- OVERTEMPERATURE PROTECTION

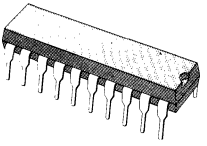
The L293B and L293E are quad push-pull drivers capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally, the L293E has external connection of sensing resistors, for switchmode control.

The L293B and L293E are packaged in 16 and 20-pin plastic DIPs respectively; both use the four center pins to conduct heat to the printed circuit board.



DIP-16 Plastic
(0.4)



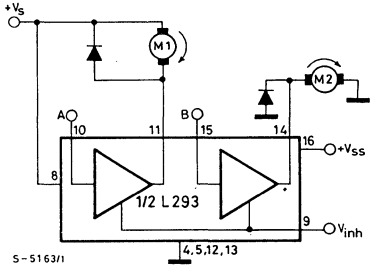
Powerdip
16+2+2

ORDERING NUMBERS: L293B (16 leads)
L293E (20 leads)

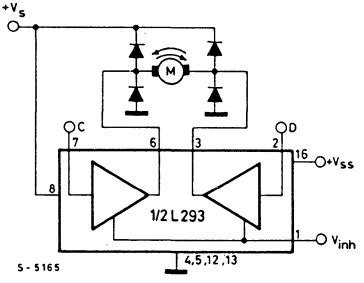
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	36	V
V_{ss}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{inh}	Inhibit voltage	7	V
I_{out}	Peak output current (non-repetitive t = 5ms)	2	A
P_{tot}	Total power dissipation at $T_{ground-pins}$ = 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

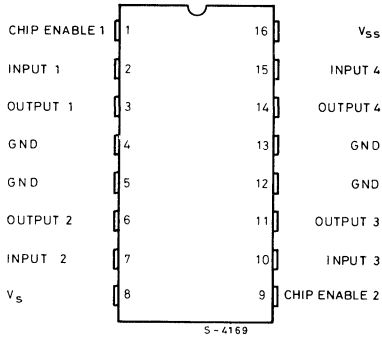
DC motor control

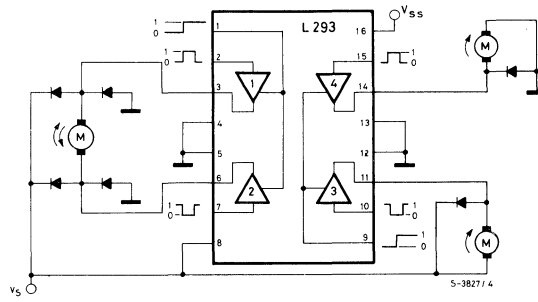


Bidirectional DC motor control

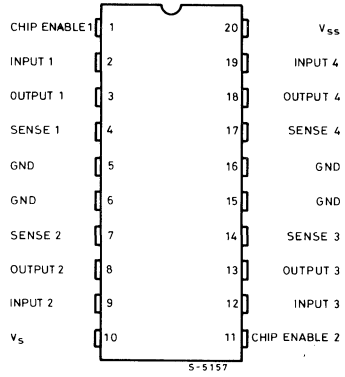


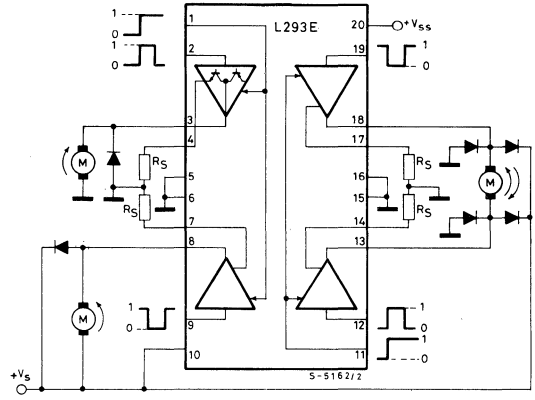
CONNECTION AND BLOCK DIAGRAM (L293)
(top view)



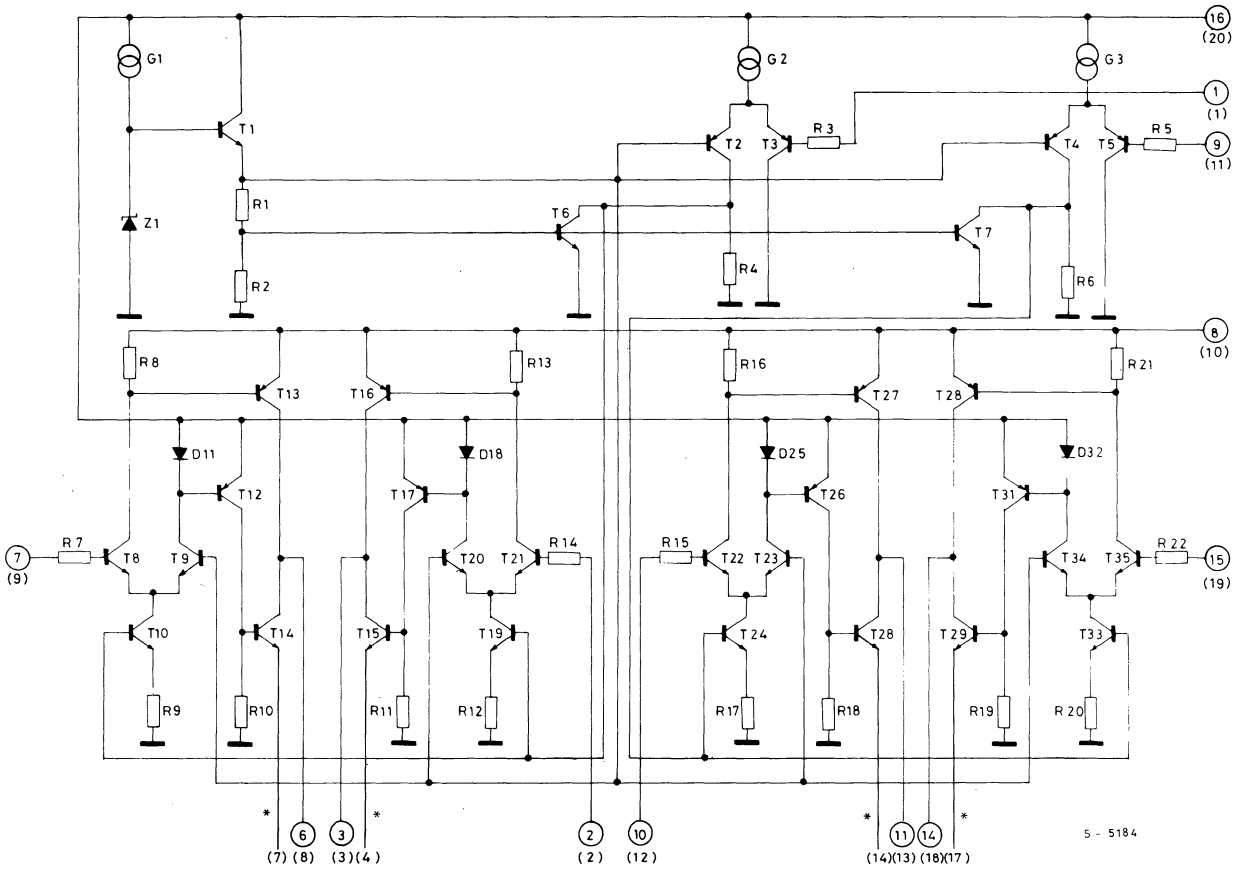


CONNECTION AND BLOCK DIAGRAM (L293E)
(top view)





SCHEMATIC DIAGRAM



(*) In the L293 these points are not externally available. They are internally connected to the ground (substrate).

○ Pins of L293 ( ) Pins of L293E

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_S= 24V, V_{SS}= 5V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		V_{ss}		36	V
V_{ss}	Logic supply voltage		4.5		36	V
I_s	Total quiescent supply current	V_i = L I_o = 0 V_{inh}= H		2	6	mA
		V_i = H I_o = 0 V_{inh}= H		16	24	
		V_{inh}= L			4	
I_{ss}	Total quiescent logic supply current	V_i = L I_o = 0 V_{inh}= H		44	60	mA
		V_i = H I_o = 0 V_{inh}= H		16	22	
		V_{inh}= L		16	24	
V_{iL}	Input low voltage		-0.3		1.5	V
V_{iH}	Input high voltage	$V_{ss} \leqslant 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{iL}	Low voltage input current	V_{IL} = 1.5V			-10	μA
I_{iH}	High voltage input current	$2.3V \leqslant V_{iH} \leqslant V_{ss} - 0.6V$		30	100	μA
V_{inhL}	Inhibit low voltage		-0.3		1.5	V
V_{inhH}	Inhibit high voltage	$V_{ss} \leqslant 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{inhL}	Low voltage inhibit current	V_{inhL} = 1.5V		-30	-100	μA
I_{inhH}	High voltage inhibit current	$2.3V \leqslant V_{inhH} \leqslant V_{ss} - 0.6V$			± 10	μA
V_{CEsatH}	Source output saturation voltage	I_o = -1A		1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage	I_o = 1A		1.2	1.8	V
V_{SENS}	Sensing Voltage (pins 4, 7, 14, 17) (**)				2	V
t_r	Rise time	0.1 to 0.9 V_o (*)		250		ns
t_f	Fall time	0.9 to 0.1 V_o (*)		250		ns
t_{on}	Turn-on delay	0.5 V_i to 0.5 V_o (*)		750		ns
t_{off}	Turn-off delay	0.5 V_i to 0.5 V_o (*)		200		ns

(*) See fig. 1.

(**) Referred to L293E.

TRUTH TABLE

V_i (each channel)	V_o	$V_{inh.}$ (°°)
H	H	H
L	L	H
H	X (°)	L
L	X (°)	L

(°) High output impedance.
(°°) Relative to the considerate channel.

Fig. 1 - Switching times

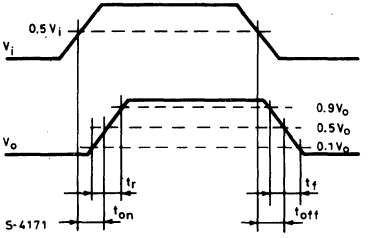


Fig. 2 - Saturation voltage vs. output current

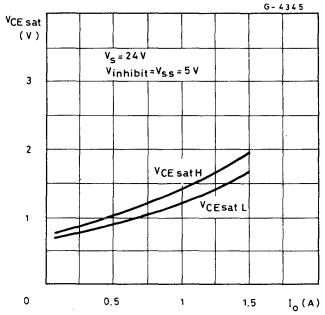


Fig. 3 - Source saturation voltage vs. ambient temperature

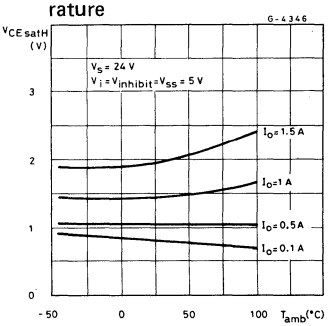


Fig. 4 - Sink saturation voltage vs. ambient temperature

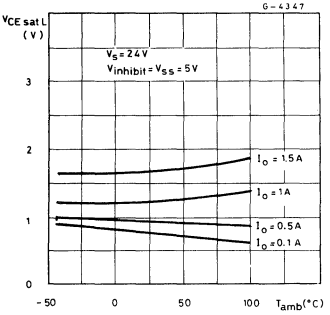


Fig. 5 - Quiescent logic supply current vs. logic supply voltage

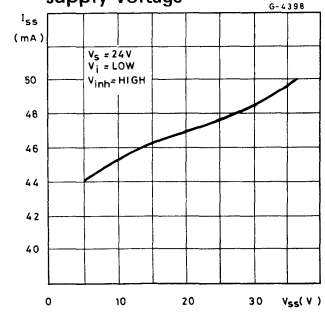


Fig. 6 - Output voltage vs. input voltage

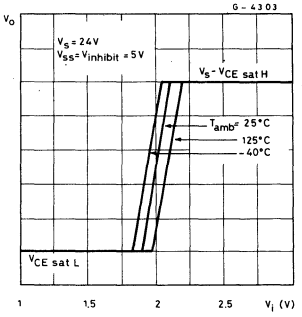
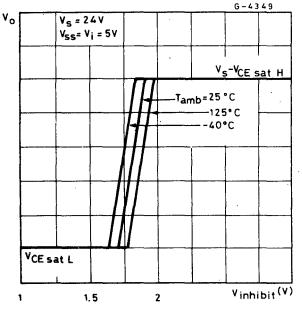
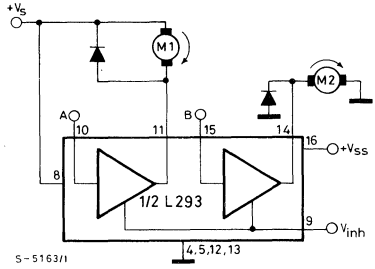


Fig. 7 - Output voltage vs. inhibit voltage



APPLICATION INFORMATION

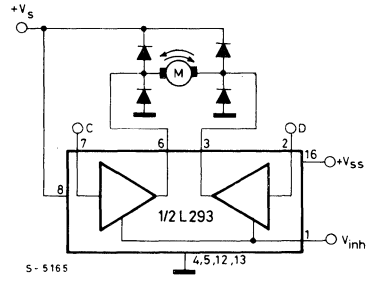
Fig. 8 - DC motor controls (with connection to ground and to the supply voltage)



V_{inh}	A	M1	B	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free running motor stop	X	Free running motor stop

L = Low H = High X = Don't care

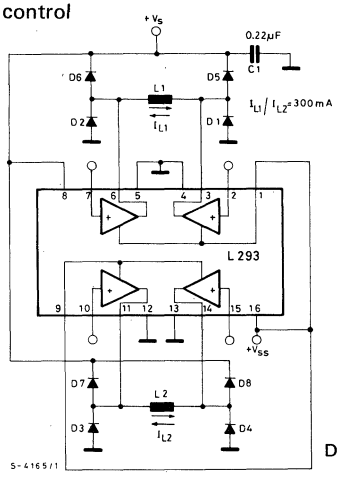
Fig. 9 - Bidirectional DC motor control



INPUTS		FUNCTION
V_{inh}= H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{inh}= L	C = X; D = X	Free running motor stop

L = Low H = High X = Don't care

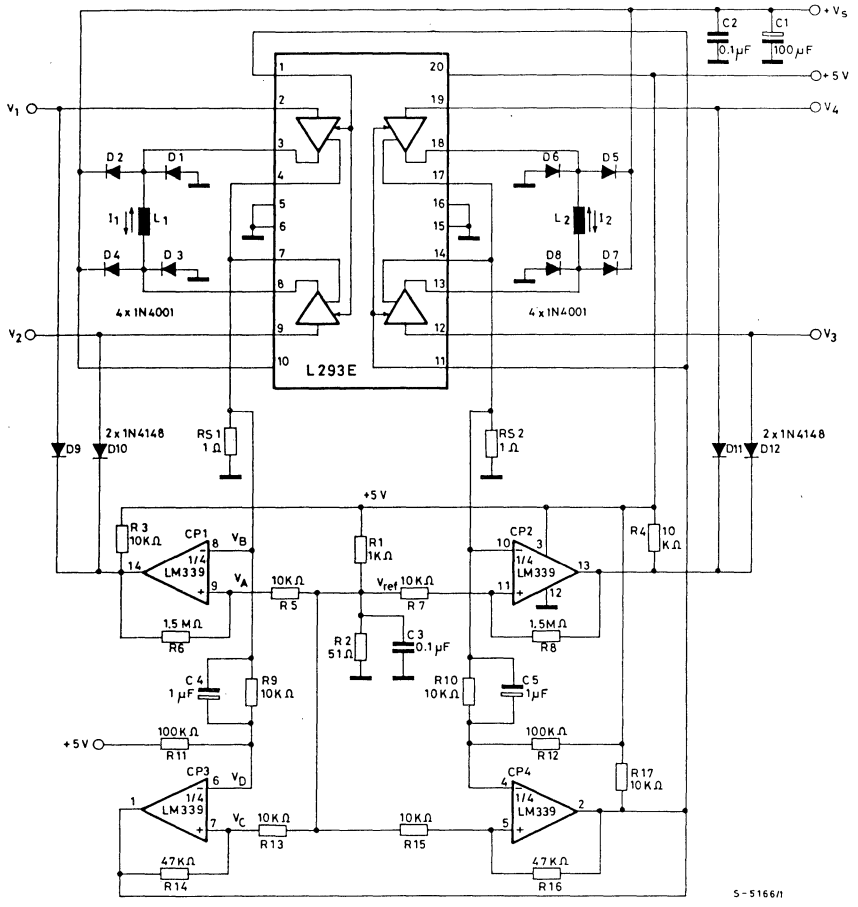
Fig. 10 - Bipolar stepping motor control



D1 - D8 = { $V_F \leqslant 1.2V$ @ I = 300 mA; trr $\leqslant$ 500 ns

APPLICATION INFORMATION (continued)

Fig. 11 - Stepping motor driver with phase current control and short circuit protection



D1 to D8 : $\begin{cases} V_F \leqslant 1.2V \text{ @ } I = 300 \text{ mA} \\ trr \leqslant 200 \text{ ns} \end{cases}$

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the L293 and the L293E can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 12 or to an external heatsink (figure 13).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 12 - Example of P.C. board copper area which is used as heatsink

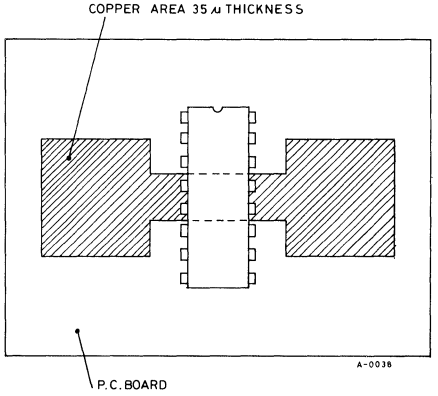
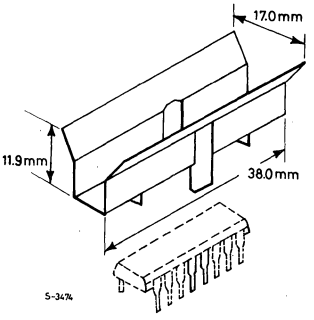


Fig. 13 - External heatsink mounting example (R_{th} = 30 °C/W)



PUSH-PULL FOUR CHANNEL/DUAL H-BRIDGE DRIVER

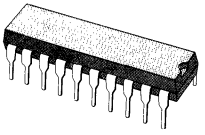
PRELIMINARY DATA

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON REPETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- SEPARATE HIGH VOLTAGE POWER SUPPLY (UP TO 44V)

The L293C is a monolithic high voltage, high current integrated circuit four channel driver in a 20 pin DIP. It is designed to accept standard TTL or DTL input logic levels and drive inductive loads (such as relays, solenoids, DC and stepping motors) and switching power transistors.

The device may easily be used as a dual H-bridge driver: separate chip enable and high voltage power supply pins are provided for each H-bridge. In addition, a separate power supply is provided for the logic section of the device.

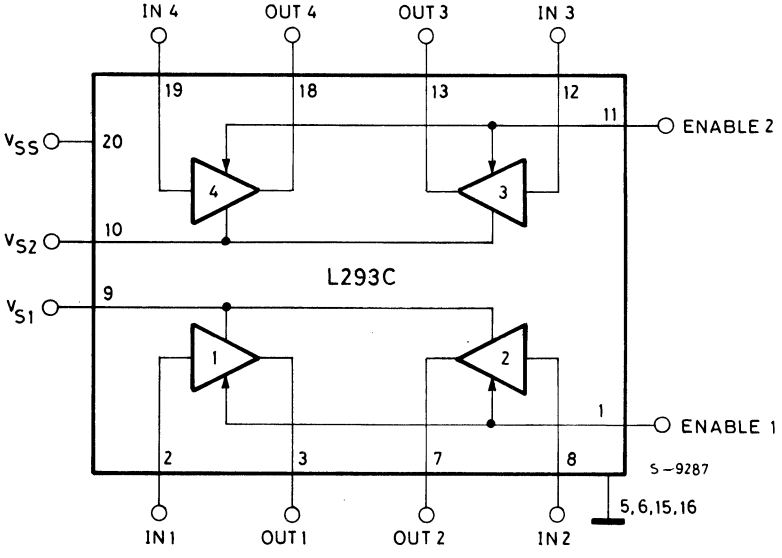
The L293C is assembled in a 20 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip
(16+2+2)

ORDER CODE: L293C

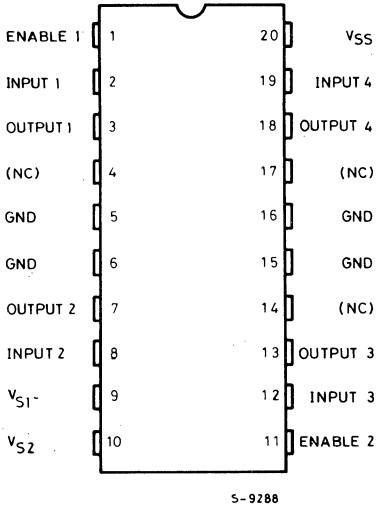
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	50	V
V_{ss}	Logic supply voltage	7	V
V_i	Input voltage	7	V
V_{EN}	Enable voltage	7	V
I_{out}	Peak output current (non-repetitive t = 5ms)	1.2	A
P_{tot}	Total power dissipation at $T_{ground\text{-}pins} = 80°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40, to 150	°C

CONNECTION DIAGRAM
(Top view)

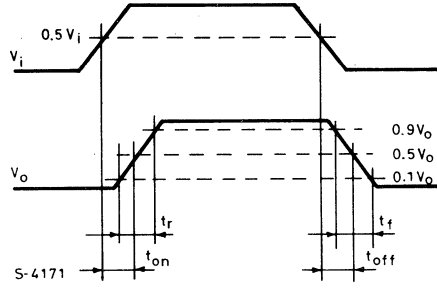


TRUTH TABLE

INPUT	ENABLE	OUTPUT
H	H	H
L	H	L
X	L	Z

Z = High output impedance
X = Don't care

SWITCHING TIMES



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_S = 24V, V_{SS} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply voltage (pin 9, 10)		V_{SS}		44	V
V_{SS}	Logic supply voltage (pin 20)		4.5		7	V
I_S	Total quiescent supply current (pin 9, 10)	V_i = L; I_o = 0; V_{EN} = H		2	6	mA
		V_i = H; I_o = 0; V_{EN} = H		16	24	
		V_{EN} = L			4	
I_{SS}	Total quiescent logic supply current (pin 20)	V_i = L; I_o = 0; V_{EN} = H		44	60	mA
		V_i = H; I_o = 0; V_{EN} = H		16	22	
		V_{EN} = L		16	24	
V_{IL}	Input low voltage (pin 2, 8, 12, 19)		-0.3		1.5	V
V_{IH}	Input high voltage (pin 2, 8, 12, 19)		2.3		V_{SS}	V
I_{IL}	Low voltage input current (pin 2, 8, 12, 19)	V_i = 1.5V			-10	μA
I_{IH}	High voltage input current (pin 2, 8, 12, 19)	2.3V ≤ V_i ≤ V_{SS} -0.6V		30	100	μA
V_{ENL}	Enable low voltage (pin 1, 11)		-0.3		1.5	V
V_{ENH}	Enable high voltage (pin 1, 11)		2.3		V_{SS}	V
I_{ENL}	Low voltage enable current (pin 1, 11)	V_{ENL} = 1.5V		-30	-100	μA
I_{ENH}	High voltage enable current (pin 1, 11)	2.3V ≤ VENH ≤ V_{ss} -0.6			± 10	μA
$V_{CE(sat)H}$	Source output saturation voltage (pins 3, 7, 13, 18)	I_o = -0.6A		1.4	1.8	V
$V_{CE(sat)L}$	Sink output saturation voltage (pins 3, 7, 13, 18)	I_o = +0.6A		1.2	1.8	V
t_r	Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f	Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on}	Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off}	Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

(*) See switching times diagram

PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

PRELIMINARY DATA

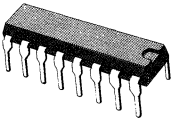
- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON REPETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VILTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

The L293D is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power transistors.

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

This device is suitable for use in switching applications at frequencies up to 5 kHz.

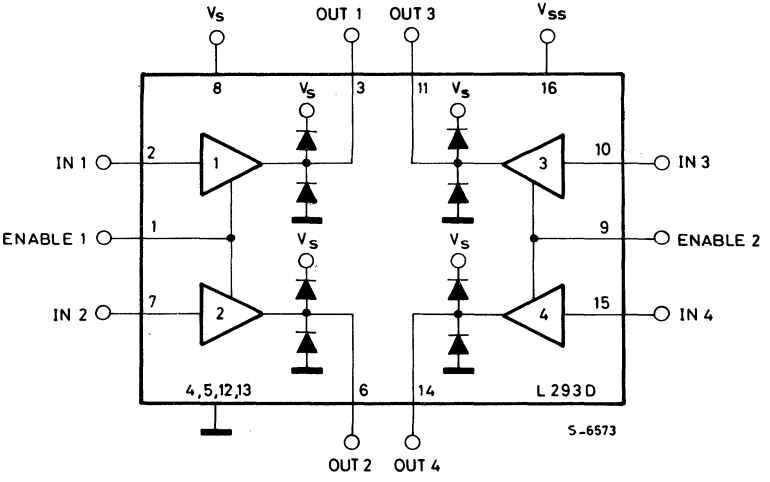
The L293D is assembled in a 16 lead plastic package which has 4 center pins connected together and used for heatsinking.



Powerdip 12+2+2

ORDERING NUMBER: L293D

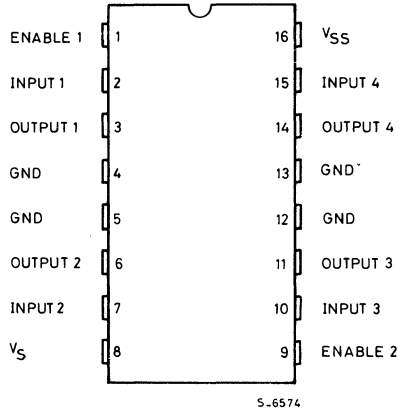
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	36	V
V_{SS}	Logic supply voltage	36	V
V_i	Input voltage	7	V
V_{en}	Enable voltage	7	V
I_o	Peak output current (100μs non repetitive)	1.2	A
P_{tot}	Total power dissipation at $T_{ground-pins}$= 80°C	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j-case}$	Thermal resistance junction-case	max	14	°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (For each channel, V_s = 24V, V_{ss} = 5V, T_{amb} = 25°C, unless otherwise specified)

Parameter		Test condition	Min.	Typ.	Max.	Unit
V_s	Supply voltage (pin 8)		V_{ss}		36	V
V_{ss}	Logic supply voltage (pin 16)		4.5		36	V
I_s	Total quiescent supply current (pin 8)	V_i = L I_o = 0 V_{en} = H		2	6	mA
		V_i = H I_o = 0 V_{en} = H		16	24	
		V_{en} = L			4	
I_{ss}	Total quiescent logic supply current (pin 16)	V_i = L I_o = 0 V_{en} = H		44	60	mA
		V_i = H I_o = 0 V_{en} = H		16	22	
		V_{en} = L		16	24	
V_{IL}	Input low voltage (pin 2, 7, 10, 15)		-0.3		1.5	V
V_{IH}	Input high voltage (pin 2, 7, 10, 15)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{IL}	Low voltage input current (pin 2, 7, 10, 15)	V_{IL} = 1.5V			-10	μA
I_{IH}	High voltage input current (pin 2, 7, 10, 15)	$2.3V \leq V_{IH} \leq V_{ss} - 0.6V$		30	100	μA
V_{enL}	Enable low voltage (pin 1, 9)		-0.3		1.5	V
V_{enH}	Enable high voltage (pin 1, 9)	$V_{ss} \leq 7V$	2.3		V_{ss}	V
		$V_{ss} > 7V$	2.3		7	
I_{enL}	Low voltage enable current current (pin 1, 9)	V_{enL} = 1.5V		-30	-100	μA
i_{enH}	High voltage enable current (pin 1, 9)	$2.3V \leq V_{enH} \leq V_{ss} - 0.6V$			± 10	μA
V_{CEsatH}	Source output saturation voltage (pins 3, 6, 11, 14)	I_o = - 0.6A		1.4	1.8	V
V_{CEsatL}	Sink output saturation voltage (pins 3, 6, 11, 14)	I_o = + 0.6A		1.2	1.8	V
V_F	Clamp diode forward voltage	I_o = 600 mA		1.3		V
t_r	Rise time (*)	0.1 to 0.9 V_o		250		ns
t_f	Fall time (*)	0.9 to 0.1 V_o		250		ns
t_{on}	Turn-on delay (*)	0.5 V_i to 0.5 V_o		750		ns
t_{off}	Turn-off delay (*)	0.5 V_i to 0.5 V_o		200		ns

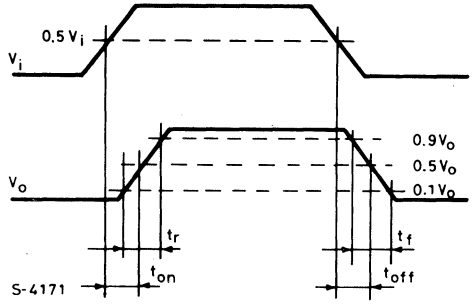
(*) See fig. 1

TRUTH TABLE (One channel)

INPUT	ENABLE (*)	OUTPUT
H	H	H
L	H	L
H	L	Z
L	L	Z

Z = High output impedance
(*) Relative to the considered channel

Fig. 1 - Switching Times



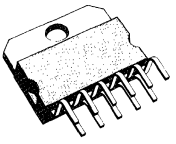
SWITCH-MODE SOLENOID DRIVER

- HIGH VOLTAGE OPERATION (UP TO 50V)
- HIGH OUPTPUT CURRRENT CAPABILITY (UP TO 4A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

DESCRIPTION

The L294 is a monolithic switchmode solenoid driver designed for fast, high-current applications such as hammer and needle driving in printers and electronic typewriters. Power dissipation is reduced by efficient switchmode operation. An extra feature of the L294 is a latched diagnostic output which indicates when the output is short circuited.

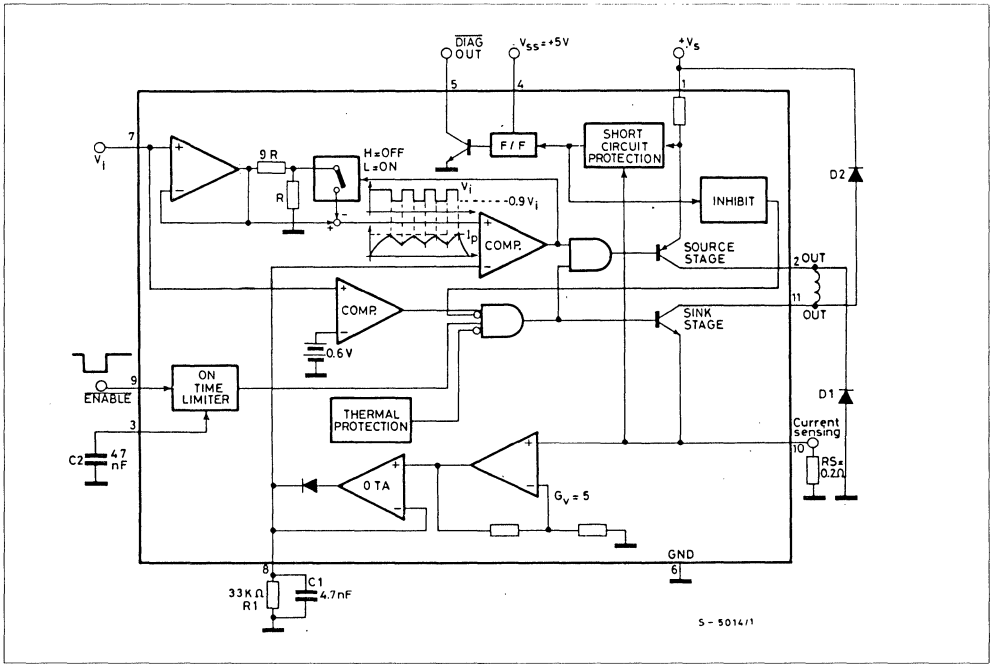
The L294 is supplied in a 11-lead Multiwatt ® plastic power package.



Multiwatt 11

ORDER CODE : L294

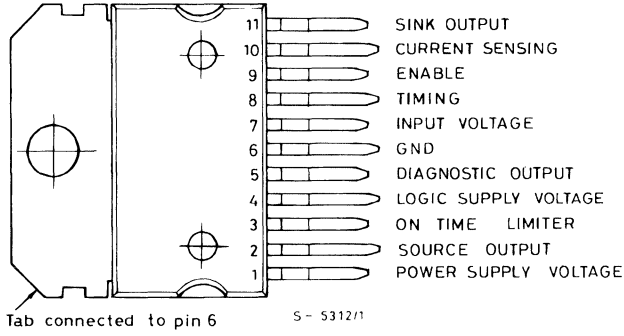
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_s	Power Supply Voltage	50	V
V_{ss}	Logic Supply Voltage	7	V
V_{EN}	Enable Voltage	7	V
V_i	Input Voltage	7	V
I_p	Peak Output Current (repetitive)	4.5	A
P_{tot}	Total Power Dissipation (at T_{case} = 75°C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_S = 40V , V_{SS} = 5V , T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Power Supply Voltage (pin 1)	Operative Condition	12		46	V
I_d	Quiescent Drain Current (pin 1)	V_{ENABLE} = H		20	30	mA
		$V_i \geq 0.6V$; V_{ENABLE} = L		70		
V_{SS}	Logic Supply Voltage (pin 4)		4.5		7	V
I_{SS}	Quiescent Logic Supply Current	V_{DIAG} = L		5	8	mA
		DIAG Output at High Impedance		10	100	µA
V_i	Input Voltage (pin 7)	Operating Output	0.6			V
		Non-operative Output			0.45	
I_i	Input Current (pin 7)	$V_i \geq 0.6V$		– 1		µA
		$V_i \leq 0.45V$		– 3		
V_{ENABLE}	Enable Input Voltage (pin 9)	Low Level	– 0.3		0.8	V
		High Level	2.4			
I_{ENABLE}	Enable Input Current (pin 9)	V_{ENABLE} = L			– 100	µA
		V_{ENABLE} = H			100	
I_{load}/V_i	Transconductance	R_s = 0.2Ω V_i = 1V	0.95	1	1.05	A/V
		V_i = 4V	0.97	1	1.03	
$V_{sat\ H}$	Source Output Saturation Voltage	I_p = 4A		1.7		V
$V_{sat\ L}$	Sink Output Saturation Voltage	I_p = 4A		2		V
$V_{sat\ H}$+ $V_{sat\ L}$	Total Saturation Voltage	I_p = 4A			4.5	V
$I_{leakage}$	Output Leakage Current	R_s = 0.2Ω ; $V_i \leq 0.45V$		1		mA
K	On Time Limiter Constant (°)	V_{ENABLE} = L		120		
V_{DIAG}	Diagnostic Output Voltage (pin 5)	I_{DIAG} = 10 mA			0.4	V
I_{DIAG}	Diagnostic Leakage Current (pin 5)	V_{DIAG} = 40V			10	µA
$\frac{V_{pin\ 8}}{V_{pin\ 10}}$	OP AMP and OTA DC Voltage Gain (°°)	$V_{pin\ 10}$ = 100 to 800 mV		5		
V_{SENS}	Sensing Voltage (pin 10) (°°°)				0.9	V

(°) After a time interval $t_{max} = KC_2$, the output stages are disabled.
(°°) See the block diagram.
(°°°) Allowed range of V_{SENS} without the intervention of the short circuit protection.

CIRCUIT OPERATION

The L294 works as a transconductance amplifier : it can supply an output current directly proportional to an input voltage level (V_i). Furthermore, it allows complete switching control of the output current waveform (see fig.1).

The following explanation refers to the Block Diagram, to fig.1 and to the typical application circuit of fig.2.

The t_{on} time is fixed by the width of the Enable input signal (TTL compatible) : it is active low and enables the output stages "source" and "sink". At the end of t_{on}, the load current I_{load} recirculates through D1 and D2, allowing fast current turn-off.

The rise time t_r depends on the load characteristics, on V_i and on the supply voltage value (V_s, pin 1). During the t_{on} time, I_{load} is converter into a voltage signal by means of the external sensing resistance R_s connected to pin 10. This signal, amplified by the op amp and converted by the transconductance amplifier OTA, charges the external RC network at pin 8 (R1, C1). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage V_i (pin 7).

After t_r, the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of V_i (1/10), allowing hysteresis operation. The current in the load now flows through D1.

Two cases are possible : the time constant of the recirculation phase is higher than R1.C1 ; the time constant is lower than R1.C1. In the first case, the voltage sensed on the non-inverting input of the comparator is just the value proportional to I_{load}. In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the R1 C1 network.

In the first case t_1 depends on the load characteristics, while in the second case it depends only on the value of R1.C1.

In other words, R1.C1 fixes the minimum value of t_1 ($t_1 \geq 1/10$ R1.C1. Note that C1 should be chosen in the range 2.7 to 10 nF for stability reasons of the OTA).

After t_1, the comparator switches again : the output is confirmed by the voltage on the non-inverting input, which reaches V_i again (hysteresis).

Now the cycle starts again : t_2, t_4 and t_6 have the same characteristics as t_r, while t_3 and t_5 are similar to t_1. The peak current I_p depends on V_i as shown in the typical transfer function of fig.3.

It can be seen that for V_i lower than 450 mV the device is not operating.

For V_i greater than 600 mV, the L294 has a transconductance of 1A/V with $R_s = 0.2\Omega$. For V_i included between 450 and 600 mV, the operation is not guaranteed.

The order parts of the device have protection and diagnostic functions. At pin 3 is connected an external capacitor C2, charged at constant current when the Enable is low.

After a time interval equal to K · C2 (K is defined in the table of Electrical Characteristics and has the dimensions of ohms) the output stages are switched off independently by the Input signal.

This avoids the load being driven in conduction for an excessive period of time (overdriving protection). The action of this protection is shown in fig.1b. Note that the voltage ramp at pin 3 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 3 and to restore the normal conditions, pin 9 must return high.

This protection can be disabled by grounding pin 3.

The thermal protection included in the L294 has a hysteresis.

It switches off the output stages whenever the junction temperature increases too much. After a fall of about 20°C, the circuit starts again.

Finally, the device is protected against any type of short circuit at the outputs : to ground, to supply and across the load.

When the source stage current is higher than 5A and/or when the pin 10 voltage is higher then 1V (i.e. for a sink current greater than $1V/R_s$) the output stages are switched off and the device is inhibited.

This condition is indicated at the open-collector output DIAG (pin 5) ; the internal flip-flop F/F changes and forces the output transistor into saturation. The F/F must be supplied independently through V_{ss} (pin 4). The DIAG signal is reset and the output stages are still operative by switching off the supply voltage at pin 1 and then by switching the device on again. After that, two cases are possible : the reason for the "bad operation" is still present and the protection acts again ; the reason has been removed and the device starts to work properly.

Figure 1 : Output Current Waveforms.

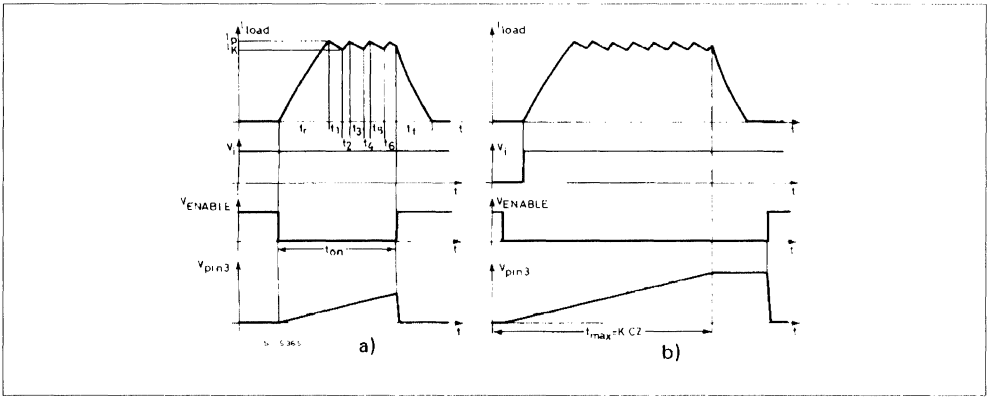


Figure 2 : Test and Typical Application Circuit.

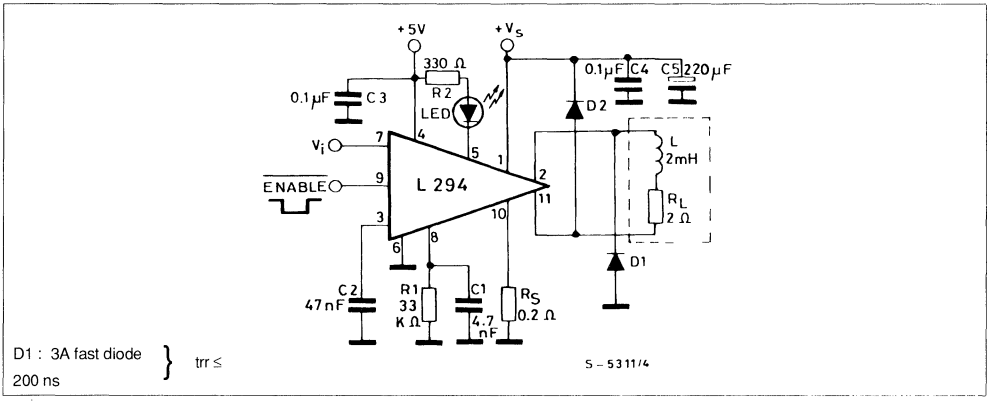


Figure 3 : Peak Output Current vs. Input Voltage.

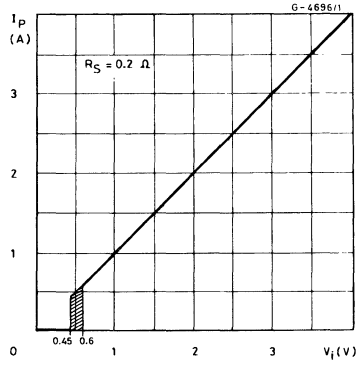


Figure 4 : Output Saturation Voltages vs. Peak Output Current.

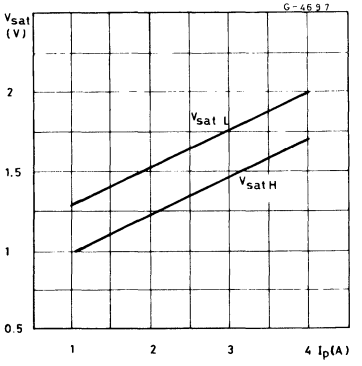


Figure 5 : Safe Operating Areas.

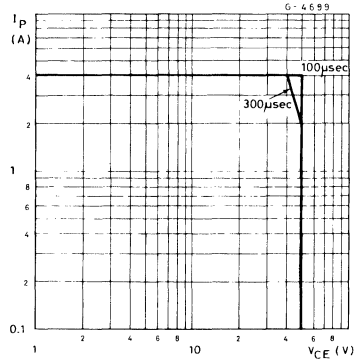
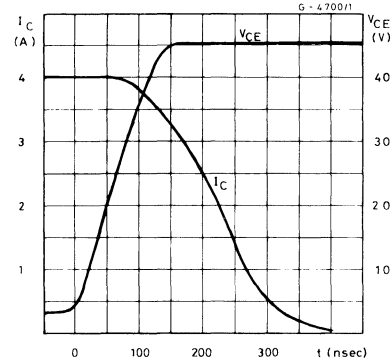


Figure 6 : Turn-off Phase.



CALCULATION OF THE SWITCHING TIMES

Referring to the block diagram and to the waveforms of fig.1, it is possible to calculate the switching times by means of the following relationships.

$$t_r = -\frac{L}{R_L} \ln\left(1 - \frac{R_L}{V1} \cdot I_p\right)$$

where : $V1 = V_s - V_{sat\,L} - V_{sat\,H} - V_{R\,sens}$

$$t_f = -\frac{L}{R_L} \ln\frac{V2}{V2 + R_L \cdot I_o}$$

Where : $V2 = V_s + V_{D1} + V_{D2}$

$I_K \leq I_o \leq I_p$

I_o is the value of the load current at the end of t_{on}.

$$t_1 = t_3 = t_5 = \ldots = \begin{cases} a) -\frac{L}{R_L} \ln\frac{0.9\, I_p \cdot R_L + V3}{I_p R_L + V3} & \text{where } V3 = V_{sat\,L} + V_{R\,sens} + V_{D1} \\ b) -R1\,C1 \ln 0.9 \cong \frac{1}{10} R1\,C1 \end{cases}$$

$$t_2 = t_4 = t_6 = \ldots = -\frac{L}{R_L} \ln\left(\frac{V1 - I_p R_L}{V1 - I_K R_L}\right)$$

Note that the time interval $t_1 = t_3 = t_5 = \ldots$ takes the longer value between case a) and case b). The switching frequency is always :

$$f_{switching} = \frac{1}{t_1 + t_2}$$

In the case a) the main regulation loop is always closed and it forces :

$$I_K = (0.9 \pm S)\, I_p$$

where : S = 3 % @ V_i = 1 V
S= 1.5 % @ V_i = 4 V

In the case b), the same loop is open in the recirculation phase and I_K, which is always lower than 0.9 I_p, is obtained by means of the following relationship.

$$I_K = I_p\, e^{-\frac{t_1 R_L}{L}} - \frac{V3}{R_L}\left(1 - e^{-\frac{t_1 R_L}{L}}\right)$$

With the typical application circuit, in the conditions V_s = 40V, I_p = 4A, the following switching times result :

t_r = 255 µs $\quad$ t_f = 174 µs @ $I_o = I_p$

t_1 = a) 70 µs, b) 16 µs $\quad$ t_2 = 29 µs $\quad$ f=10.2 KHz

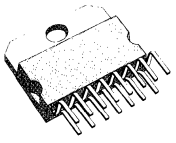
DUAL SWITCH-MODE SOLENOID DRIVER

PRELIMINARY DATA

- HIGH CURRENT CAPABILITY (up to 2.5A per channel)
- HIGH VOLTAGE OPERATION (up to 46V for power stage)
- HIGH EFFICIENCY SWITCHMODE OPERATION
- REGULATED OUTPUT CURRENT (adjustable)
- FEW EXTERNAL COMPONENTS
- SEPARATE LOGIC SUPPLY
- THERMAL PROTECTION

The L295 is a monolithic integrated circuit in a 15 - lead Multiwatt ® package ; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels at the inputs and can drive 2 solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and dual supplies (for interfacing with peripherals running at a higher voltage than the logic).

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.



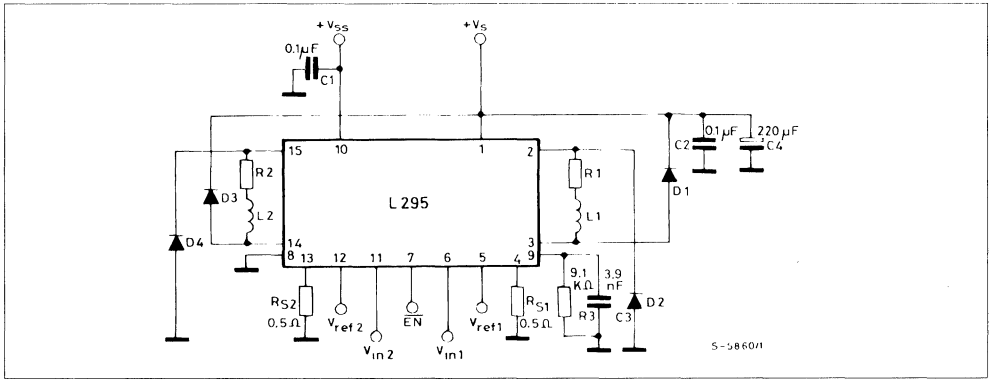
Multiwatt 15

ORDER CODE : L295

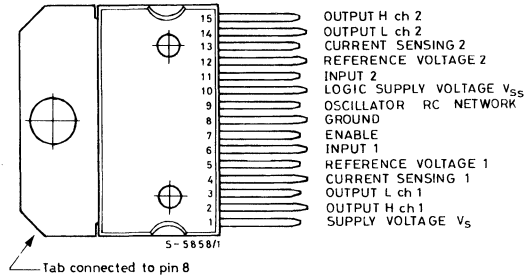
ABSOLUTE MAXIMUM RATINGS

V_S	Supply voltage	50	V
V_{SS}	Logic supply voltage	12	V
V_{EN}, V_i	Enable and input voltage	7	V
V_{ref}	Reference voltage	7	V
I_o	Peak output current (each channel)		
	– non repetitive (t = 100 µsec)	3	A
	– repetitive (80 % on – 20 % off ; T_{on} = 10 ms)	2.5	A
	– DC operation	2	A
P_{tot}	Total power dissipation (at T_{case} = 75 °C)	25	W
T_{stg}, T_j	Storage and junction temperature	– 40 to 150	°C

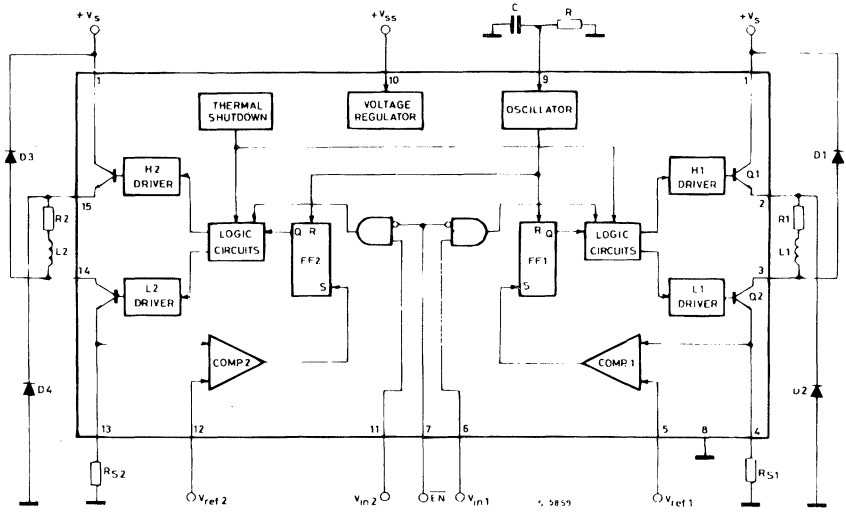
APPLICATION CIRCUIT



CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



THERMAL DATA

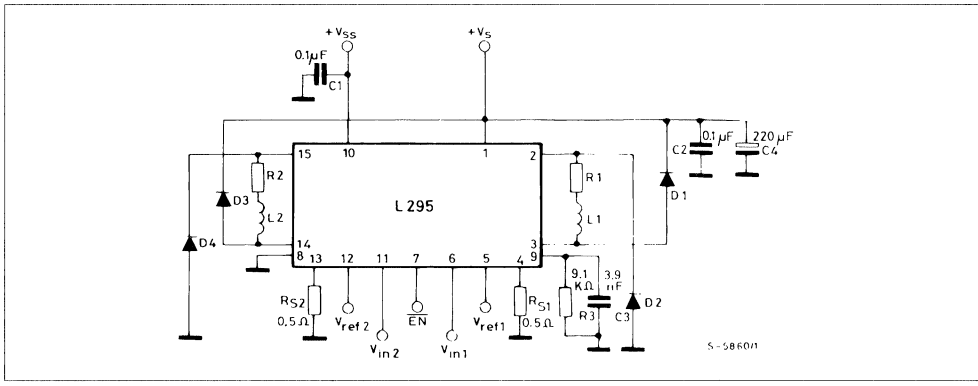
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the application circuit, V_{ss} = 5V, V_s = 36V; T_j = 25°C; L = low; H = high; unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			12		46	V
V_{ss}	Logic Supply Voltage			4.75		10	V
I_d	Quiescent drain current (from VSS)	V_S = 46 V; V_{i1} = V_{i2} = V_{EN} = L				4	mA
I_{ss}	Quiescent drain current (from VS)	V_{SS} = 10 V				46	mA
V_{i1}, V_{i2}	Input Voltage		Low	− 0.3		0.8	V
			High	2.2		7	
V_{EN}	Enable Input Voltage		Low	− 0.3		0.8	V
			High	2.2		7	
I_{i1}, I_{i2}	Input Current		V_{i1} = V_{i2} = L			− 100	µA
			V_{i1} = V_{i2} = H			10	
I_{EN}	Enable Input Current		V_{EN} = L			− 100	µA
			V_{EN} = H			10	
V_{ref1}, V_{ref2}	Input Reference Voltage			0.2		2	V
I_{ref1}, I_{ref2}m	Input Reference Voltage					− 5	µA
F_{osc}	Oscillation Frenquency	C = 3.9 nF ;	R = 9.1 KΩ		25		KHz
$\frac{I_p}{V_{ref}}$	Transconductance (each ch.)	V_{ref} = 1 V	R_S = 0.5Ω	1.9	2	2.1	A/V
V_{drop}	Total output voltage drop (each channel) (*)	I_o = 2 A			2.8	3.6	V
V_{sens1} V_{sens2}	External sensing resistors voltage drop					2	V

(*) V_{drop} = $V_{CEsat\ Q1}$ + $V_{CEsat\ Q2}$.

APPLICATION CIRCUIT



D2, D4 = 2A High speed diodes
D1, D3 = 1A High speed diodes) trr ≤ 200 ns

R1 = R2 = 2Ω
L1 = L2 = 5 mH

FUNCTIONAL DESCRIPTION

The L295 incorporates two independent driver channels with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three microprocessor compatible digital inputs and two analog inputs. These inputs are :

$\overline{EN}$ chip enable (digital input,active low) , enables both channels when in the low state.

V_{in1}, V_{in2} channel inputs (digital inputs,active high), enable each channel independently. A channel is actived when both $\overline{EN}$ and the appropriate channel input are active.

V_{ref1}, V_{ref2} reference voltages (analog inputs), used to program the peak load currents. Peak load current is proportional to V_{ref}.

Since the two channels are identical, only channel one will be described.

The following description applies also the channel two, replacing FF2 for FF1, V_{ref2} for V_{ref1} etc.

When the channel is activated by a low level on the EN input and a high level on the channel input, V_{in2}, the output transistors Q1 and Q2 switch on and current flows in the load according to the exponential law :

$$I = \frac{V}{R1} \left(1 - e^{\frac{-R1\,t}{L1}}\right)$$

where : R1 and L1 are the resistance and inductance of the load and V is the voltage available on the load ($V_s - V_{drop} - V_{sense}$).

The current increases until the voltage on the external sensing resistor, R_{S1}, reaches the reference voltage, V_{ref1}. This peak current, I_{p1}, is given by :

$$I_{p1} = \frac{V_{ref1}}{R_{S1}}$$

At this point the comparator output, Comp1, sets the RS flip–flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1}, decreases according to the law :

$$I = \left(\frac{V_A}{R1} + I_{p1}\right) e^{\frac{-R1\,t}{L1}} - \frac{V_A}{R1}$$

where $V_A = V_{CEsat\,Q2} + V_{sense\,1} + V_{D2}$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in fig. 1.

At the time t_2 the channel 1 is disabled, by taking the inputs V_{in1} low and/or $\overline{EN}$ high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law :

$$I = \left(\frac{V_B}{R1} + I_{T2} \right) e^{\frac{-R1\,t}{L1}} - \frac{V_B}{R1}$$

where $V_B = V_S + V_{D1} + V_{D2}$

I_{T2} = current value at the time t_2.

Fig. 2 in shows the current waveform obtained with an RC network connected between pin 9 and ground. From to t_1 the current increases as in fig. 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the outout transistor, Q1. The current increases until the drop on the sensing resistor R_{S1} is equal to V_{ref1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in fig. 4 and must be chosen in the range 10 to 30 KHz.

It is possible with external hardware to change the reference voltage V_{ref} in order to obtain a high peak current I_p and a lower holding current I_h (see fig.3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150 °C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20 °C.

The analog input pins (V_{ref1}, V_{ref2}) can be left open or connected to V_{ss} ; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_S :

$$I_p = \frac{2.5}{R_S}$$

SIGNAL WAVEFORMS

Figure 1 : Load current waveform with pin 9 connected to GND.

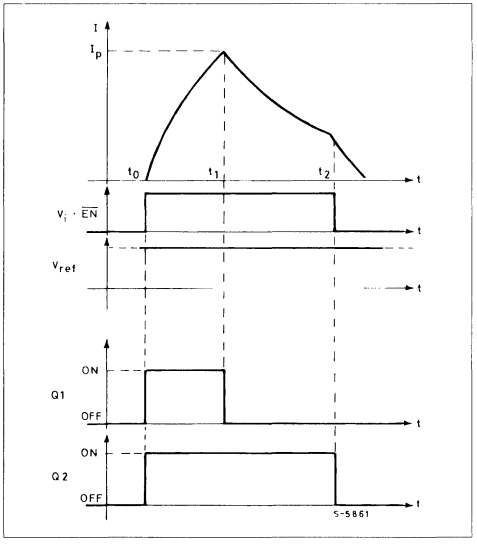
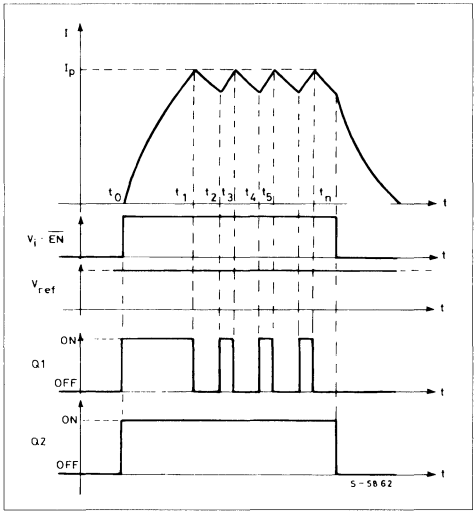


Figure 2 : Load current waveform with external R–C network connected between pin 9 and ground.



SIGNAL WAVEFORMS (continued)

Figure 3 : With V_{ref} changed by hardware.

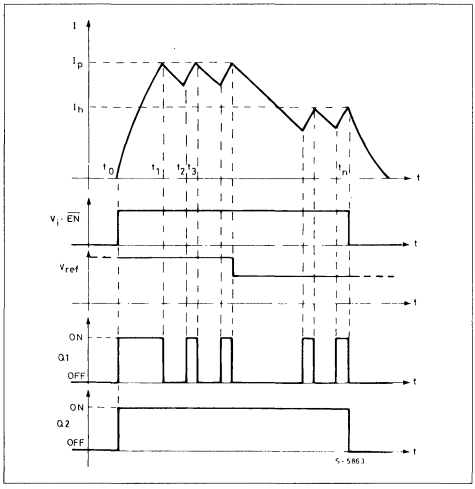
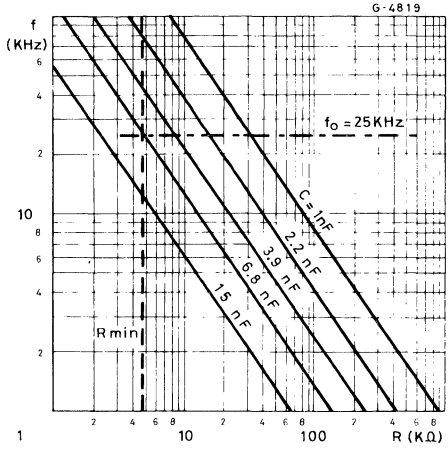


Figure 4 : Switching frequency vs. values of R and C.



HIGH CURRENT SWITCHING REGULATORS

- 4 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (±2 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

The L296 and L296P are stepdown power switching regulators delivering 4 A at a voltage variable from 5.1 V to 40 V.

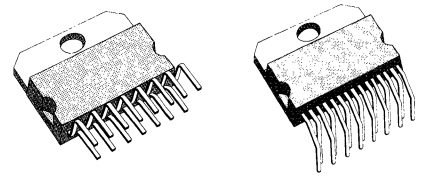
Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P incudes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200 KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

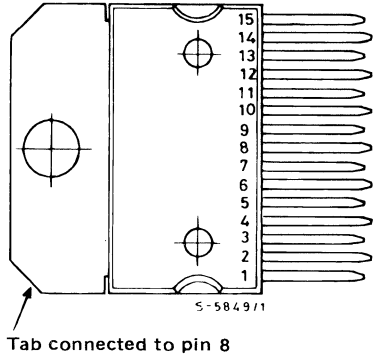
Multiwatt®
(15-lead)



ORDER CODES :

L296	L296HT
L296P	L296PHT

PIN CONNECTION (top view)



CROWBAR DRIVE
RESET OUTPUT
RESET DELAY
RESET INPUT
OSCILLATOR
FEEDBACK INPUT
FREQUENCY COMPENSATION
GROUND
SYNC. INPUT
INHIBIT INPUT
SOFT-START
CURRENT LIMIT
SUPPLY VOLTAGE
OUTPUT
CROWBAR INPUT

Tab connected to pin 8

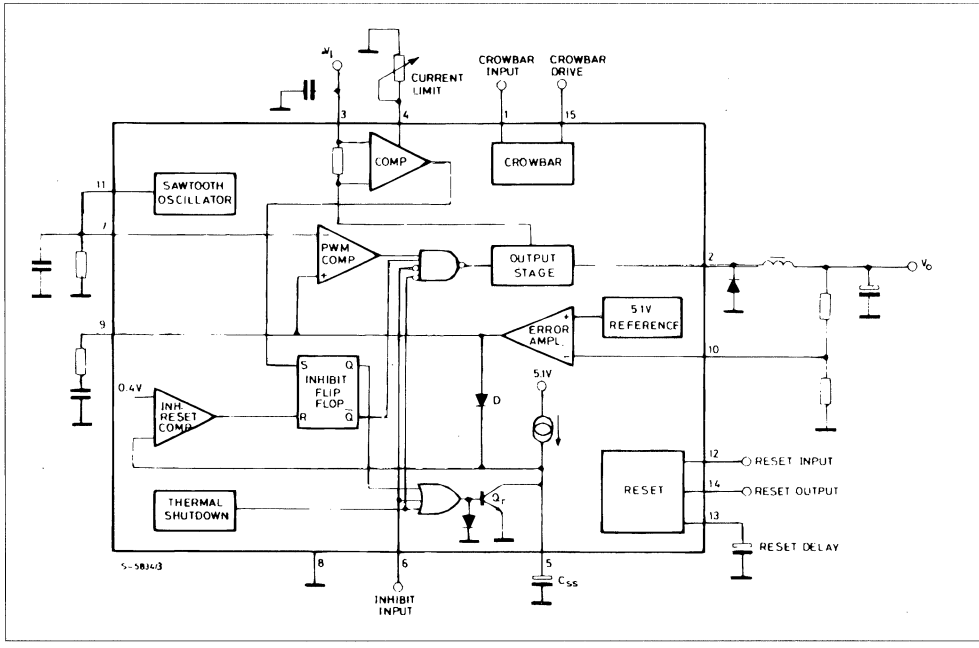
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_i	Input Voltage (pin 3)	50	V
$V_i - V_2$	Input to Output Voltage Difference	50	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 200KHz	− 1 − 7	V V
V_1, V_{12}	Voltage at Pins 1, 12	10	V
V_{15}	Voltage at Pin 15	15	V
V_4, V_5, V_7, V_9, V_{13}	Voltage at Pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at Pins 10 and 6	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	− 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

BLOCK DIAGRAM



PIN FUNCTIONS

N°	Name	Function
1	CROWBAR INPUT	Voltage Sense Input for Crowbar Overvoltage Protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20 %. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator Output.
3	SUPPLY VOLTAGE	Unrergulated Voltage Input. An internal Regulator Powers the L296s Internal Logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – Level Remote Inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal on the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC networki connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1 V to 40 V and delivering 4 A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1 V on-chip reference (zener zap trimmed to ± 2 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1 V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor Css and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4 V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

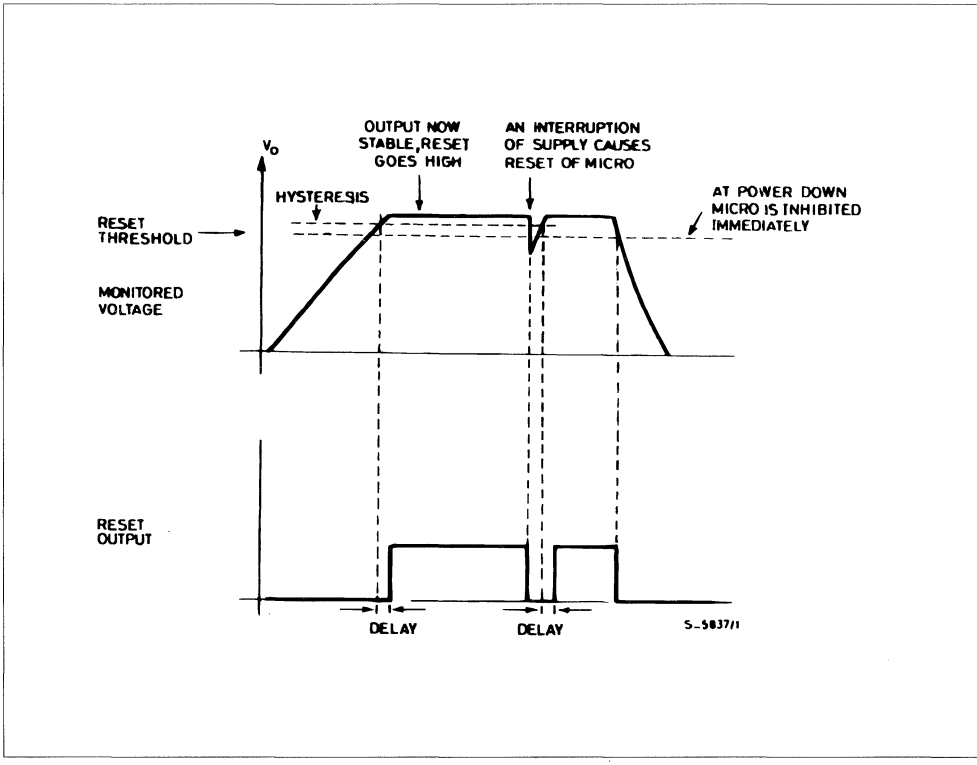
The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The scrowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20 %. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 °C and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms.



CIRCUIT OPERATION (continued)

Figure 2 : Soft Start Waveforms.

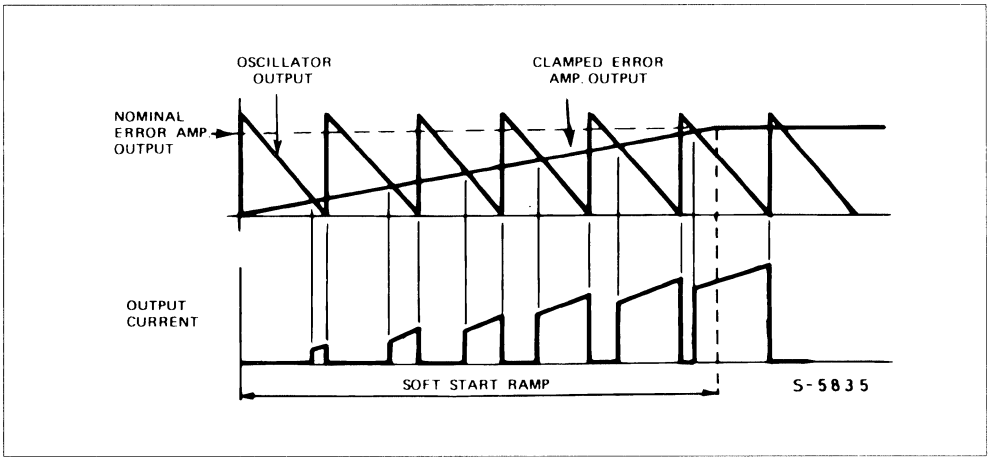
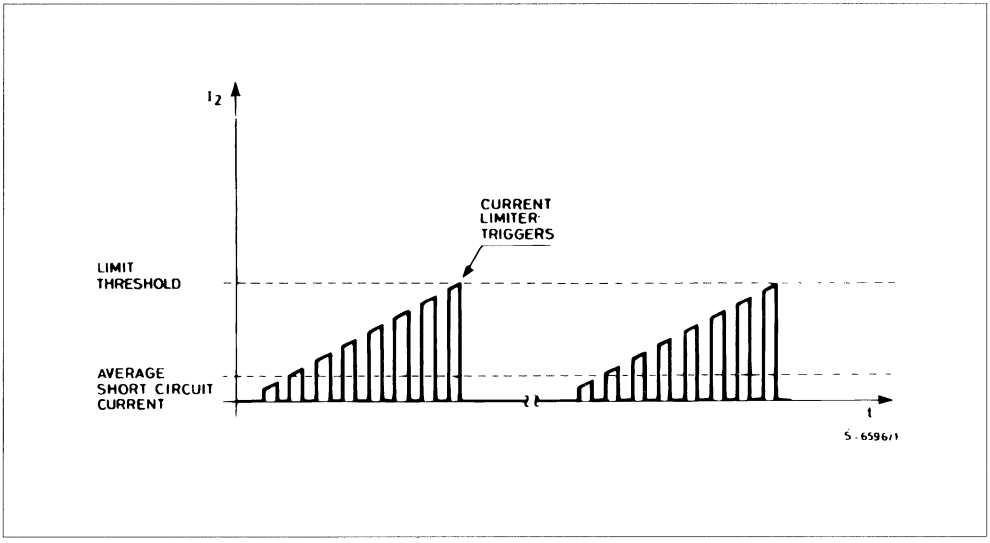


Figure 3 : Current Limiter Waveforms.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, V_i = 35 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)

V_o	Output Voltage Range	V_i = 46 V I_o = 1 A	V_{ref}		40	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 36 V $I_o \leq$ 3 A	9		46	V	4
V_i	Input Voltage Range	Note (1) $V_o = V_{REF}$ to 36 V I_o = 4 A			46	V	4
ΔV_o	Line Regulation	V_i =10 V to 40 V, $V_o = V_{ref}$, I_o = 2 A		15	50	mV	4
ΔV_o	Load Regulation	I_o = 2 A to 4 A		10	30	mV	4
		$V_o = V_{ref}$ I_o = 0.5 A to 4 A		15	45	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9 V to 46 V I_o = 2 A	5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0 °C to 125 °C I_o = 2 A		0.4		mV/°C	
V_d	Dropout Voltage Between Pin 2 and Pin 3	I_o = 4 A		2	3.2	V	4
		I_o = 2 A		1.3	2.1	V	4
I_{2L}	Current Limiting Threshold (pin 2)	L296 Pin 4 Open V_i = 9 V to 40 V $V_o = V_{ref}$ to 36 V	4.5		7.5	A	4
		L296P Pin 4 Open V_i = 9 V to 40 V $V_o = V_{ref}$	5		7	A	4
		R_{lim} = 22 KΩ	2.5		4.5	A	4
I_{SH}	Input Average Current	V_i = 46 V; Output Short-circuited		60	100	mA	4
η	Efficiency	I_o = 3 A $V_o = V_{ref}$		75		%	4
		V_o = 12 V		85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_i = 2 V_{rms} f_{ripple} = 100 Hz $V_o = V_{ref}$ I_o = 2 A	50	56		dB	4
f	Switching Frequency		85	100	115	KHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9 V to 46 V		0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0 °C to 125 °C		1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$; I_o = 1 A	200			KHz	–
T_{sd}	Thermal Shutdown Junction Temperature	Note (2)	135	145		°C	–

DC CHARACTERISTICS

I_{3Q}	Quiescent Drain Current	V_i = 46 V V_7 = 0 V V_6 = 0 V		66	85	mA	6a
		S1 : B S2 : B V_6 = 3V		30	40	mA	6a
$-I_{2L}$	Output Leakage Current	V_i = 46 V, V_6 = 3 V, S1 : B, S2 : A, V_7 = 0 V			2	mA	6a

Note (1) : Using min. 7 A schottky diode.
(2) : Guaranteed by design, not 100 % tested in production.

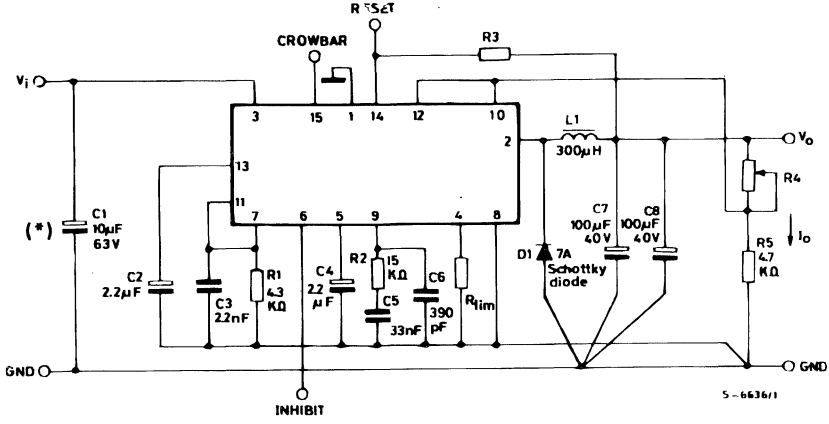
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
SOFT START								
$I_{5\,so}$	Source Current	$V_6 = 0$ V, $V_5 = 3$ V		80	130	150	µA	6b
$I_{5\,si}$	Sink Current	$V_6 = 3$ V, $V_5 = 3$ V		50	70	120	µA	6b
INHIBIT								
V_{6L}	Low Input Voltage	$V_i = 9$ V to 46 V	S1 : B S2 : B	− 0.3		0.8	V	6a
V_{6H}	High Input Voltage	$V_7 = 0$ V		2		5.5	V	6a
$-I_{6L}$	Input Current with Low Input Voltage	$V_i = 9$ V to 46 V	$V_6 = 0.8$ V			10	µA	6a
$-I_{6H}$	Input Current with High Input Voltage	$V_7 = 0$ V S1 : B S2 : B	$V_6 = 2$ V			3	µA	6a
ERROR AMPLIFIER								
V_{9H}	High Level Output Voltage	$V_{10} = 4.7$ V, $I_9 = 100$ µA, S1 : A, S2 : A		3.5			V	6c
V_{9L}	Low Level Output Voltage	$V_{10} = 5.3$ V, $I_9 = 100$ µA, S1 : A, S2 : E				0.5	V	6c
$I_{9\,si}$	Sink Output Current	$V_{10} = 5.3$ V,	S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	$V_{10} = 4.7$ V,	S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	$V_{10} = 5.2$ V,	S1 : B		2	10	µA	6c
		$V_{10} = 6.4$ V,	S1 : B, L296P		2	10	µA	6c
G_v	DC Open Loop Gain	$V_9 = 1$ V to 3 V,	S1 : A, S2 : C	46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR								
$-I_7$	Input Bias Current of PWM Comparator	$V_7 = 0.5$ V to 3.5 V				5	µA	6a
$-I_{11}$	Oscillator Source Current	$V_{11} = 2$ V,	S1 : A S2 : B	5				mA
RESET								
$V_{12\,R}$	Rising Threshold Voltage	$V_i = 9$ V to 46 V,	S1 : B, S2 : B	V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
$V_{12\,F}$	Falling Threshold Voltage			4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
$V_{13\,D}$	Delay Thershold Voltage	$V_{12} = 5.3$ V,	S1 : A, S2 : B	4.3	4.5	4.7	V	6d
$V_{13\,H}$	Delay Threshold Voltage Hysteresis				100		mV	6d
$V_{14\,S}$	Output Saturation Voltage	$I_{14} = 16$ mA; $V_{12} = 4.7$ V; S1, S2 : B				0.4	V	6d
I_{12}	Input Bias Current	$V_{12} = 0$ V to V_{ref},	S1 : B, S2 : B		1	3	µA	6d
$-I_{13\,so}$	Delay Source Current	$V_{13} = 3$ V S1 : A S2 : B	$V_{12} = 5.3$ V	70	110	140	µA	6d
$I_{13\,si}$	Delay Sink Current		$V_{12} = 4.7$ V	10			mA	6d
I_{14}	Output Leakage Current	$V_i = 46$ V, $V_{12} = 5.3$ V,	S1 : B, S2 : A			100	µA	6d

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
CROWBAR								
V_1	Input Threshold Voltage	S1 : B		5.5	6	6.4	V	6b
V_{15}	Output Saturation Voltage	V_i = 9 V to 46 V, I_{15} = 5 mA	V_i = 5.4 V S1 : A		0.2	0.4	V	6b
I_1	Input Bias Current	V_1 = 6 V,	S1 : B			10	µA	6b
$-I_{15}$	Output Source Current	V_i = 9 V to 46 V, V_{15} = 2 V	V_1 = 6.5 V S1 : B	70	100		mA	6b

Figure 4 : Dynamic Test Circuit.



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A Core type : MAGNETICS 58930 - A2 MPP
N° turns : 43 Wire Gauge : 1 mm (18 AWG) COGEMA 946044
(*) Minimum suggested value (10 µF) to avoid oscillations. Ripple consideration leads to typical value of 1000 µF or higher.

Figure 5 : PC. Board and Component Layout of the Circuit of Figure 4 (1:1 scale).

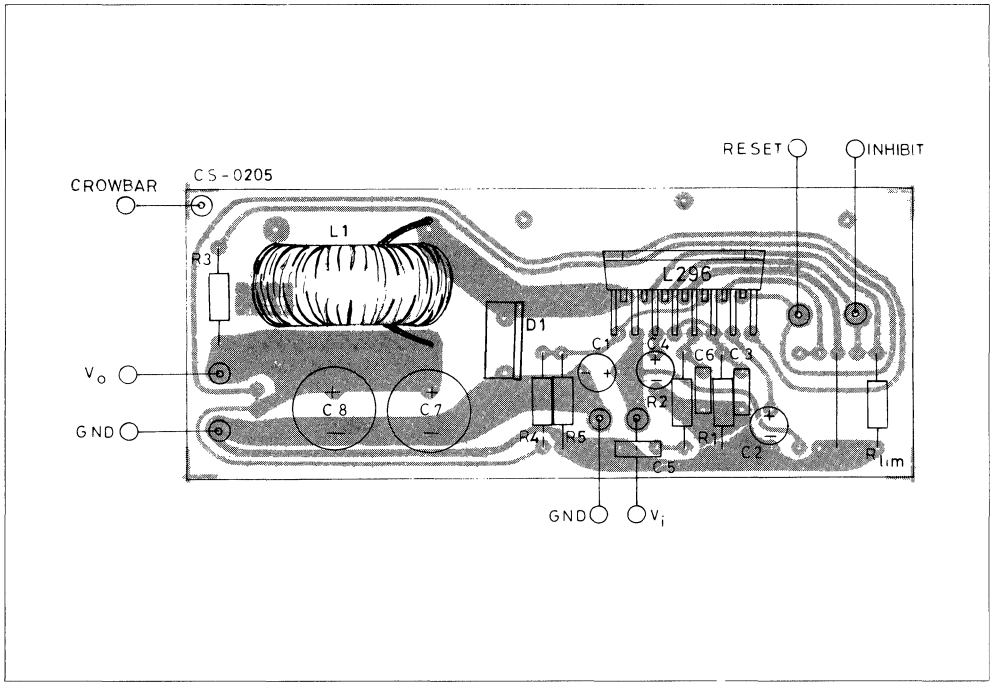


Figure 6 : DC Test Circuits.

Figure 6a.

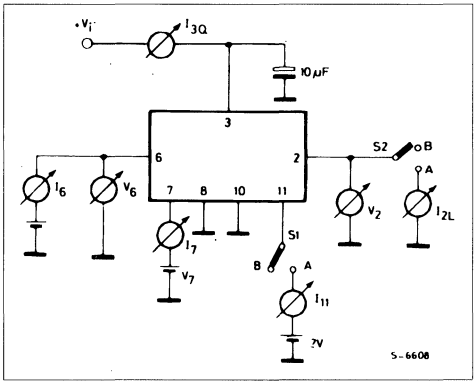


Figure 6b.

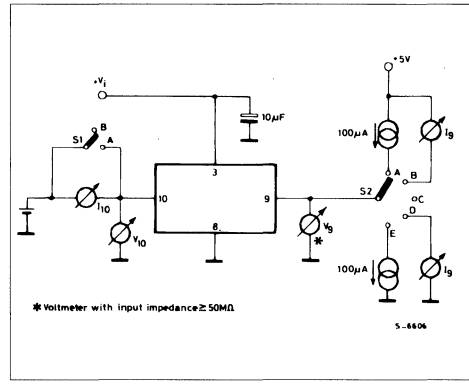


Figure 6c.

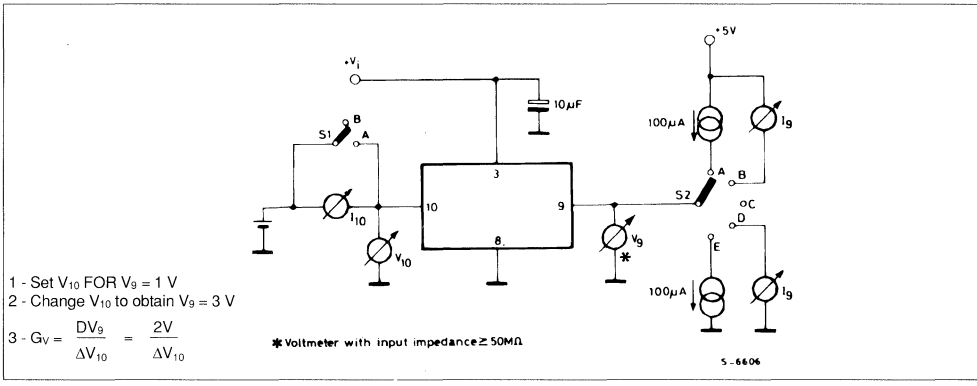


Figure 6d.

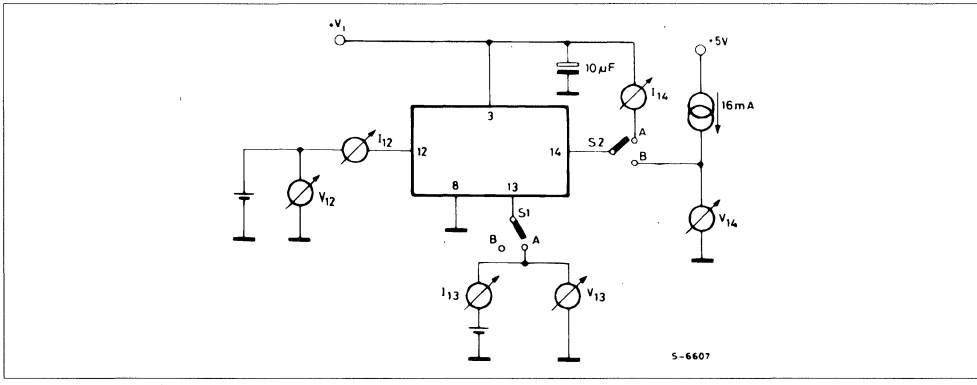


Figure 7 : Quienscent Drain Current vs. Supply Voltage (0 % Duty Cycle - see fig. 6a).

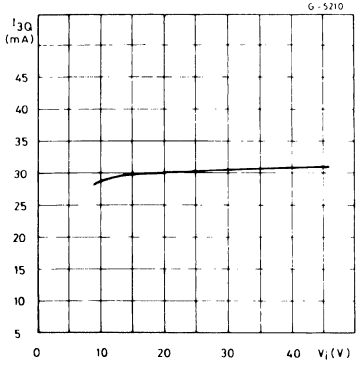


Figure 8 : Quienscent Drain Current vs. Supply Voltage (100 % Duty Cycle see fig. 6a).

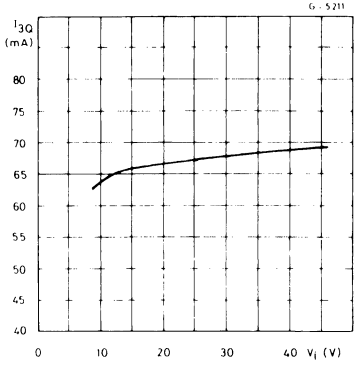


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % Duty Cycle - see fig. 6a).

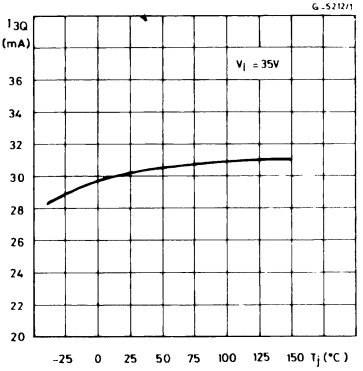


Figure 10 : Quiescent Drain Current vs. Junction Temperature (100 % Duty Cycle - see fig. 6a).

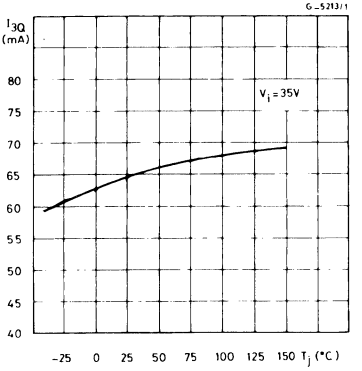


Figure 11 : Reference Voltage (pin 10) vs. V_I (see fig. 4).

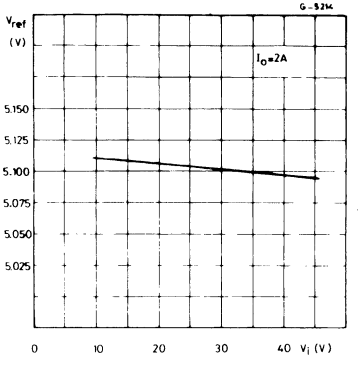


Figure 12 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

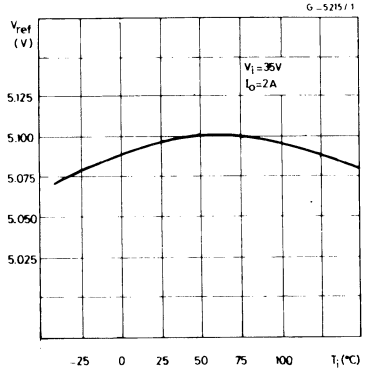


Figure 13 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

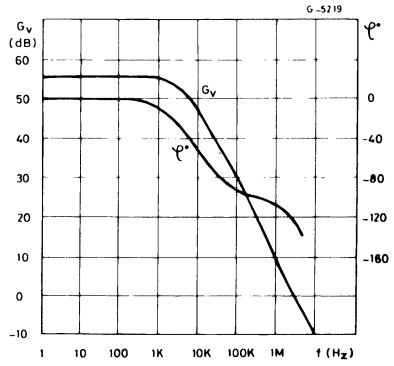


Figure 14 : Switching Frequency vs. Input Voltage (see fig. 4).

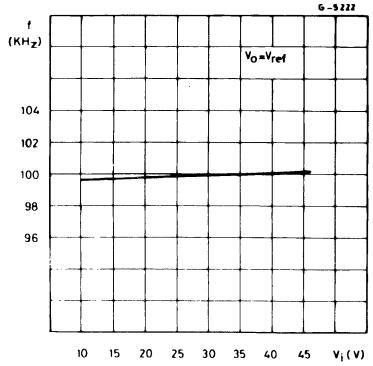


Figure 15 : Switching Frequency vs. Junction Temperature (see fig. 4).

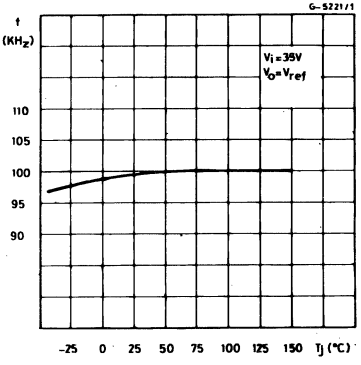


Figure 16 : Switching Frequency vs. R1 (see fig. 4).

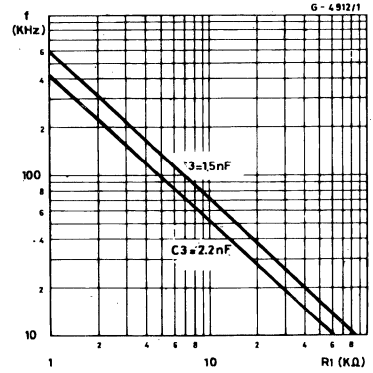


Figure 17 : Line Transient Response (see fig. 4).

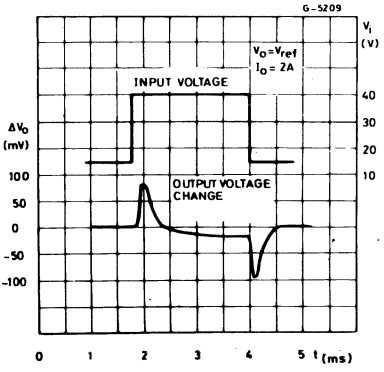


Figure 18 : Load Transient Response (see fig. 4).

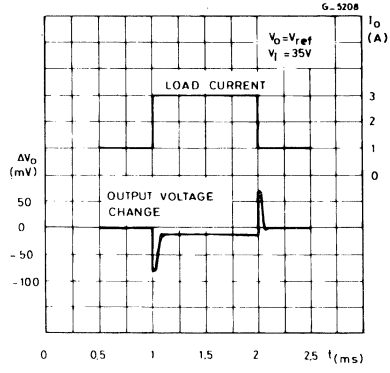


Figure 19 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 4).

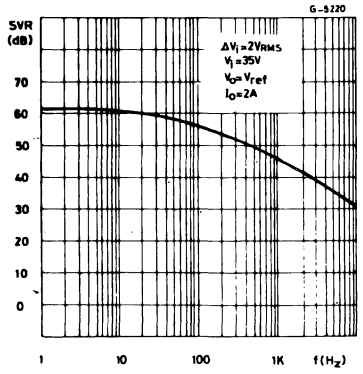


Figure 20 : Dropout Voltage Between Pin 3 and Pin 2 vs. Current at Pin 2.

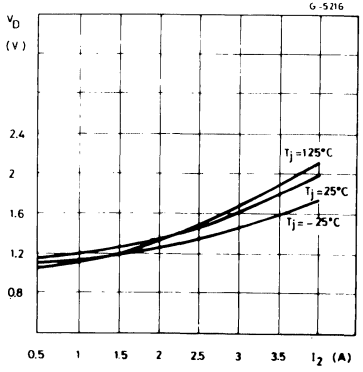


Figure 21 : Dropout Voltage Between Pin 3 and Pin 2 vs. Junction Temperature.

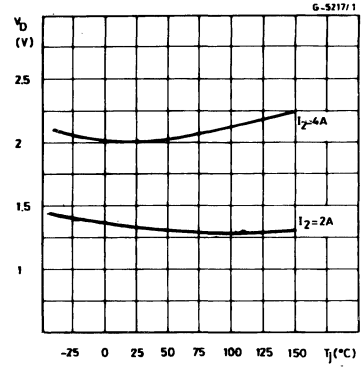


Figure 22 : Power Dissipation Derating Curve.

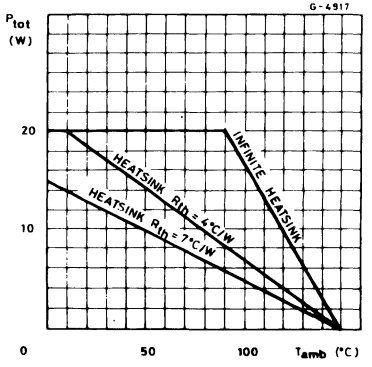


Figure 23 : Power Dissipation (device only) vs. Input Voltage.

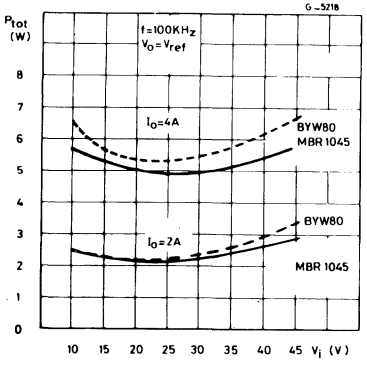


Figure 24 : Power Dissipation (device only) vs. Input voltage.

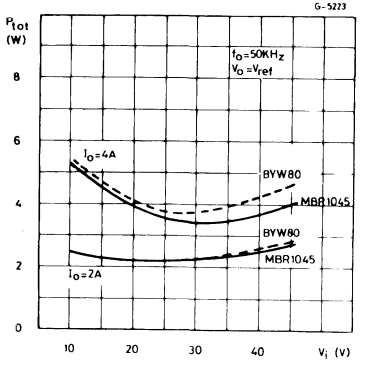


Figure 25 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

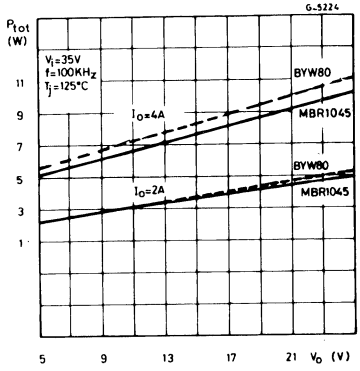


Figure 26 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

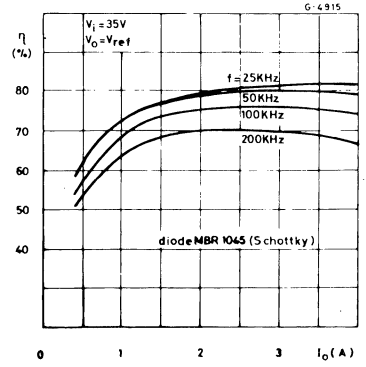


Figure 27 : Voltage and Current Waveforms at Pin 2 (see fig. 4).

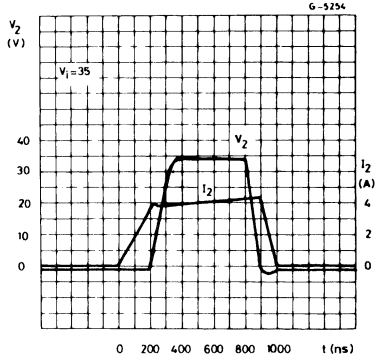


Figure 28 : Efficiency vs. Output Current.

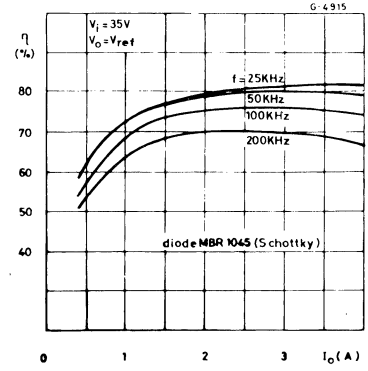


Figure 29 : Efficiency vs. Output Voltage.

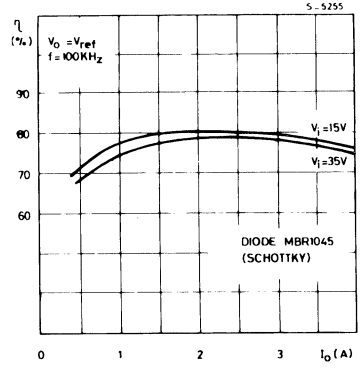


Figure 30 : Efficiency vs. Output Voltage.

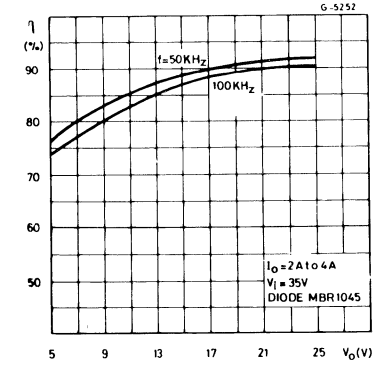


Figure 31 : Current Limiting Threshold vs. $R_{pin\ 4}$ (L296P only).

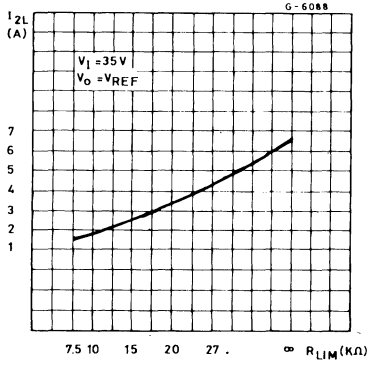


Figure 32 : Current Limiting Threshold vs. Junction Temperature.

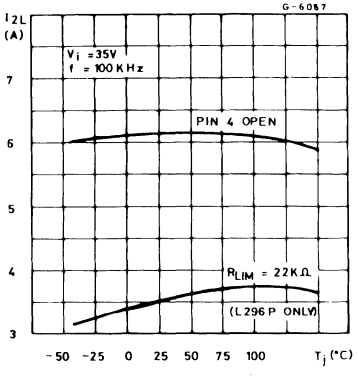
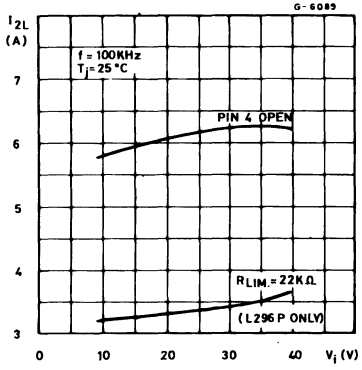
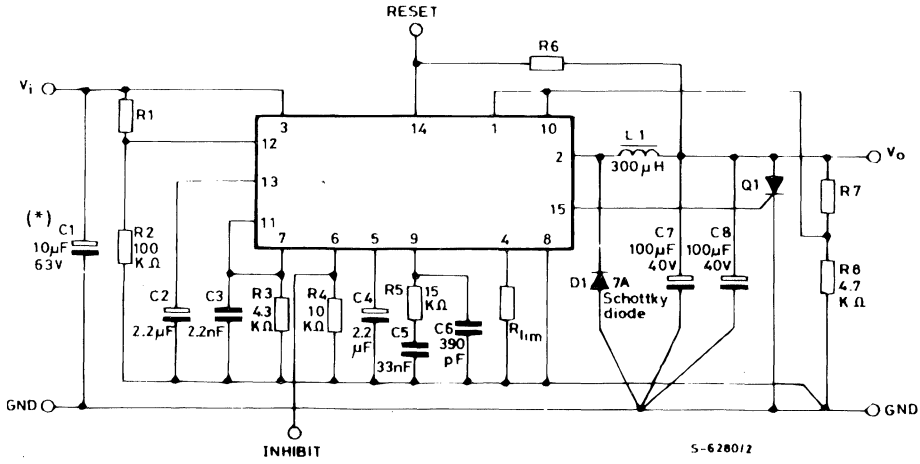


Figure 33 : Current Limiting Threshold vs. Supply Voltage.



APPLICATION INFORMATION

Figure 34 : Typical Application Circuit.



(*) Minimum value (10 µF) to avoid oscillations ; ripple consideration leads to typical value of 1000 µF or higher L1 : 58930 - MPP COGEMA 946044 ; GUP 20 COGEMA 946045

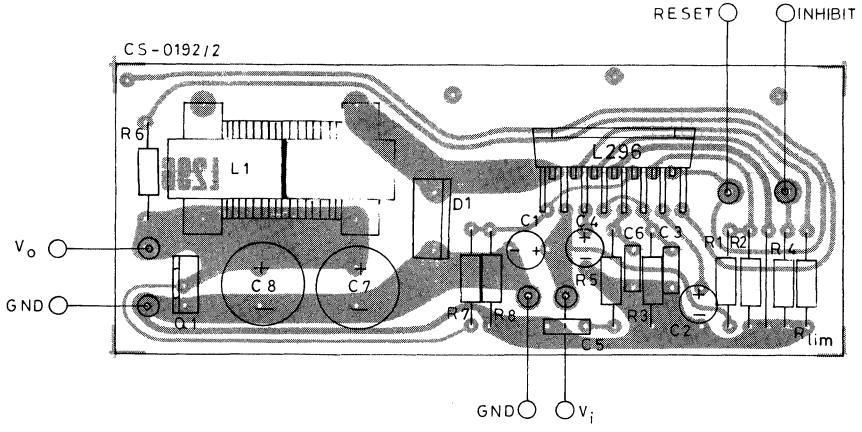
SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	65	0.8 mm	1 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages

V_O	R8	R7
12 V	4.7 KΩ	6.2 KΩ
15 V	4.7 KΩ	9.1 KΩ
18 V	4.7 KΩ	12 KΩ
24 V	4.7 KΩ	18 KΩ

Figure 35 : P.C. Board and Component Layout of the Circuit of fig. 34 (1:1 scale).



SELECTION OF COMPONENT VALUES (see fig. 34)

Component	Recommended Value	Purpose	Allowed Rage Min.	Allowed Rage Max.	Notes
R1 R2	– 100 kΩ	Set Input Voltage Threshold for Reset.	–	 220 kΩ	$R1/R2 = \frac{V_{i\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets Switching Frequency	1 kΩ	100 kΩ	
R4	10 kΩ	Pull-down Resistor		22 kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency Compensation	10 kΩ		
R6		Collector Load For Reset Output	$\frac{V_o}{0.05\ A}$		Omitted if reset function not used.
R7 R8	– 4.7 kΩ	Divider to Set Output Voltage	– –	– 10 kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}} -$
R_{lim}	–	Sets Current Limit Level	7.5 kΩ		If R_{lim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 µF	Stability	2.2 µF		
C2	2.2 µF	Sets Reset Delay	–	–	Omitted if reset function not used.
C3	2.2 nF	Sets Switching Frequency	1 nF	3.3 nF	
C4	2.2 µF	Soft Start	1 µF	–	Also determines average short circuit current.
C5	33 nF	Frequency Compensation			
C6	390 pF	High Frequency Compensation	–	–	Not required for 5 V operation.
C7, C8 L1	100 µF 300 µH	Output Filter	– 100 µH	–	
Q1		Crowbar Protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation Diode			7A Schottky or 35 ns t_{rr} Diode.

Figure 36 : A Minimal 5.1 V Fixed Regulator. Very Few Components are Required.

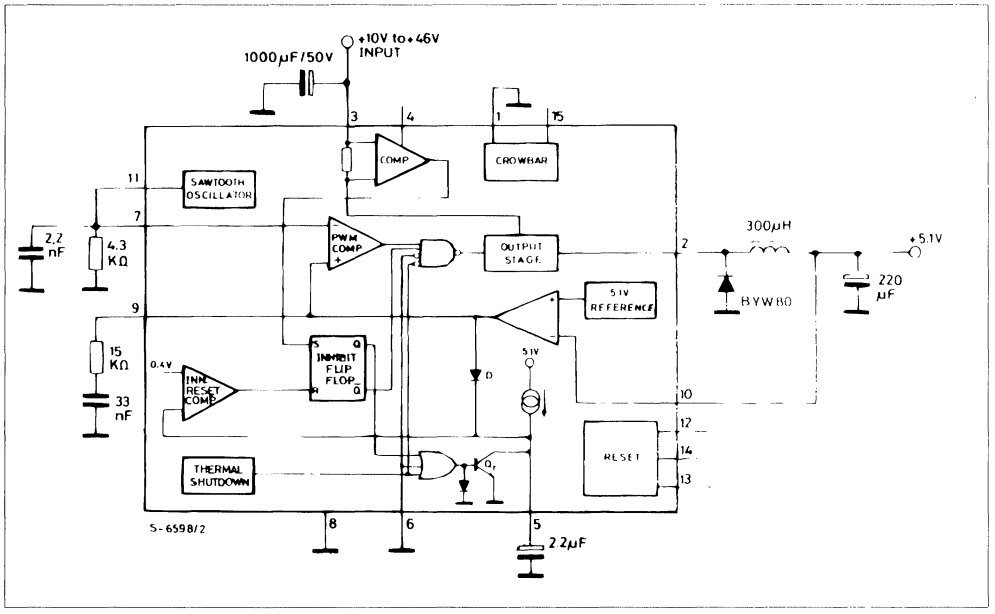


Figure 37 : 12 V/10 A Power Supply.

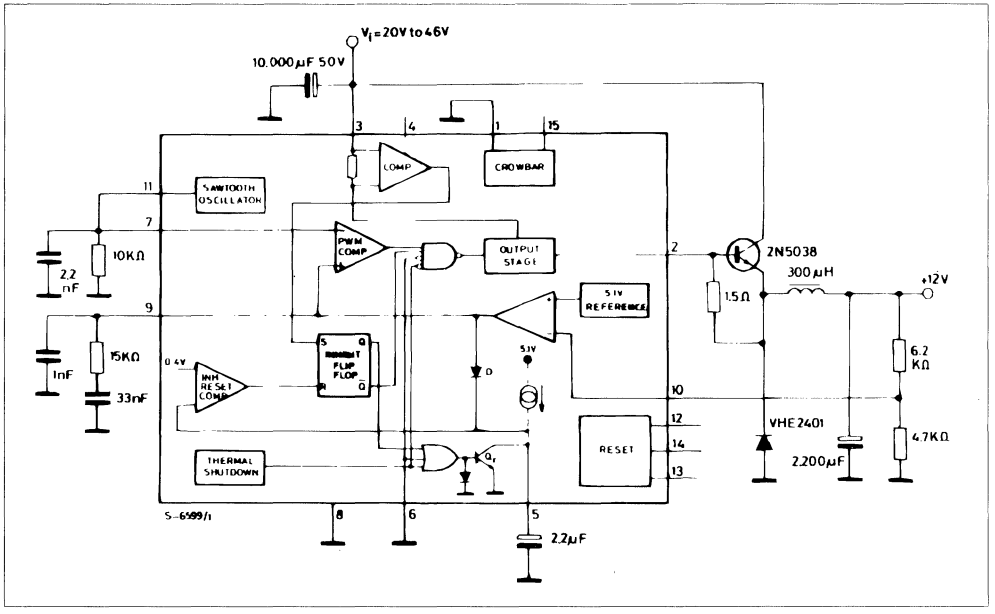
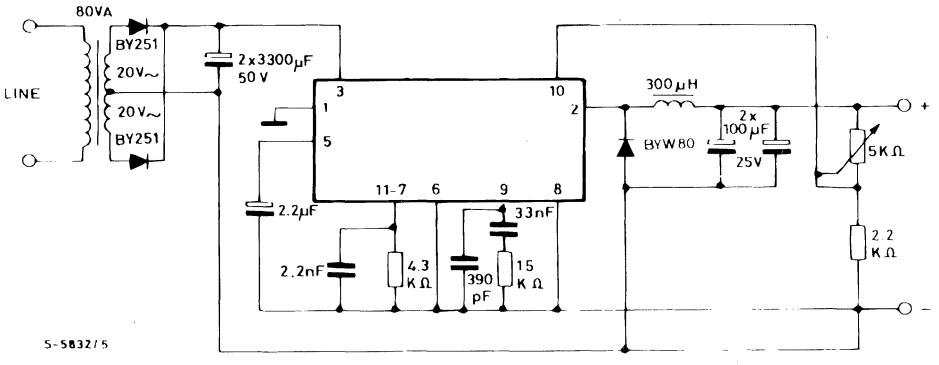
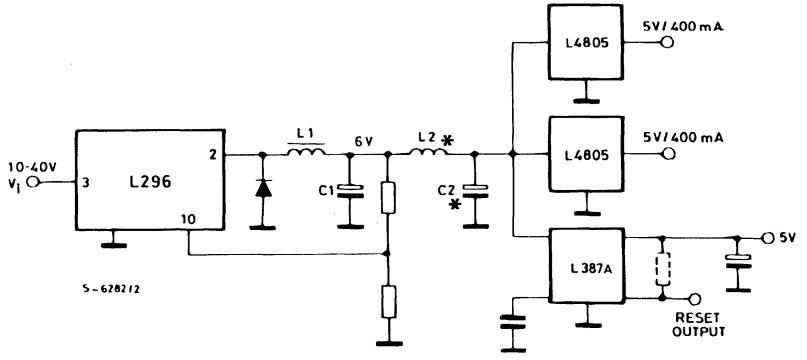


Figure 38 : Programmable Power Supply.



V_o = 5.1 to 15 V
I_o = 4 A max. (min. load current = 100 mA)
ripple ≤ 20 mV
load regulation (1 A to 4 A) = 10 mV (V_o = 5.1 V)
line regulation (220 V ± 15 % and to I_o = 3 A) = 15 mV (V_o = 5.1 V)

Figure 39 : Preregulator for Distributed Supplies.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Figure 40 : In Multiple Supplies Several L296s can be Synchronized As Shown.

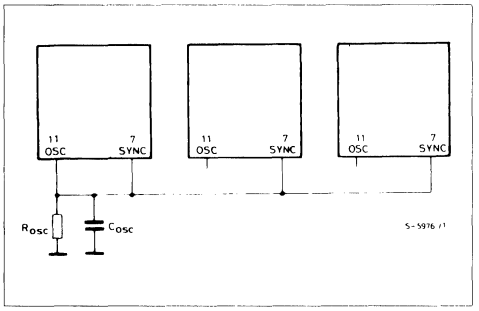


Figure 41 : Voltage Sensing for Remote Load.

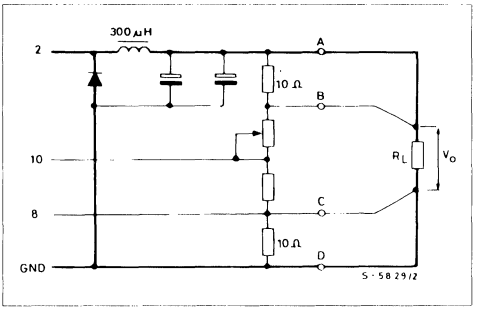


Figure 42 : A 5.1 V/15 V/24 V Multiple Supply. Note the Synchronization of the Three L296s.

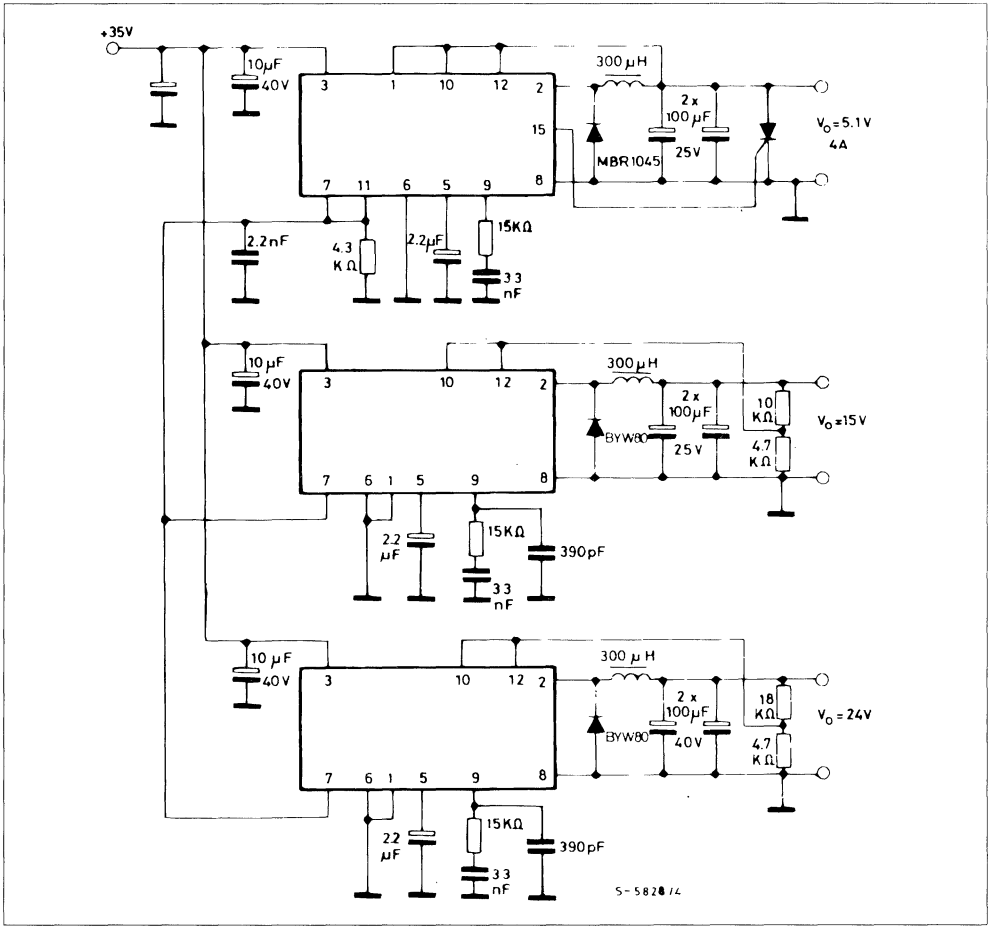
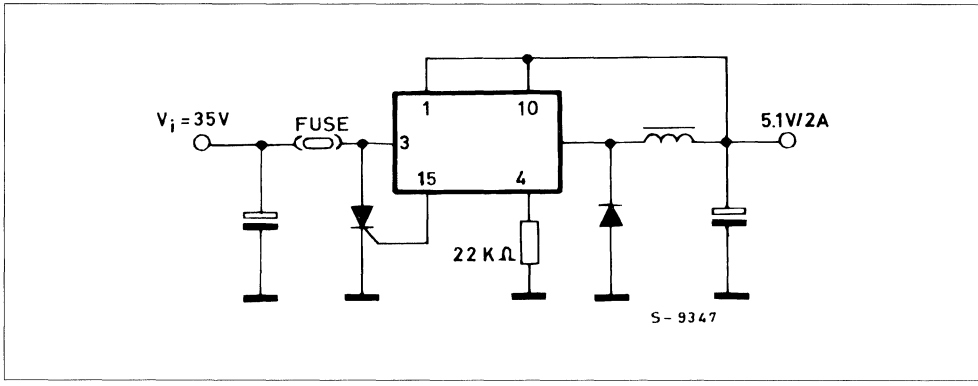


Figure 43 : 5.1 V/2 A Power Supply using External Limiting Current Resistor and Crowbar Protection on the Supply Voltage (L296P only).



SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{SS}, must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Fig. 44.

In this circuit the divider R1, R2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{SS}.

The approximate discharge times obtained with this circuit are :

C_{SS}	t_{DIS}
2.2 µF	200 µs
4.7 µF	300 µs
10 µF	600 µs

If these times are still too long, an external PNP transistor may be added, as shown in Fig. 45 ; with this circuit discharge times of a few microseconds may be obtained.

Figure 44.

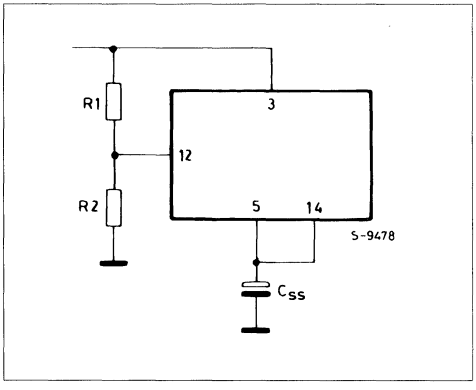
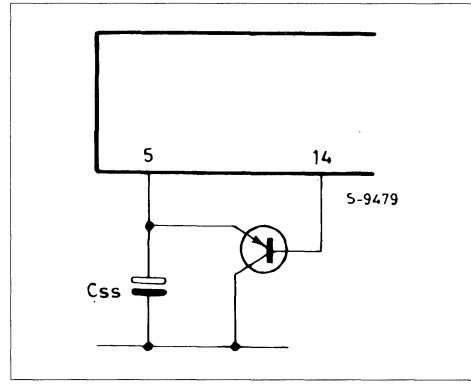


Figure 45.



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

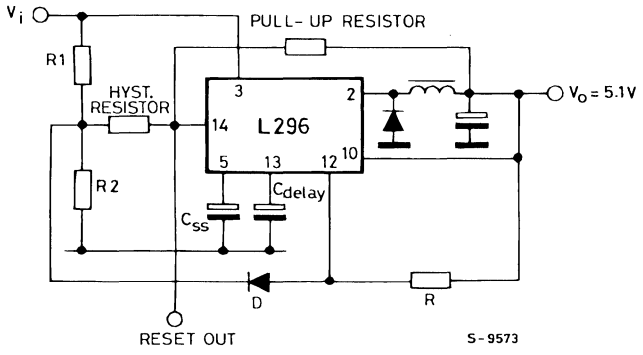
In this case the reset delay time (pin 13) can only start when the output voltage is $V_o \geq V_{REF}$ - 100 mV and the voltage across R2 is higher than 4.5 V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100 Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft start. Soft start and delayed reset are thus two sequential functions.

The hysteresis resistor should be in the range of about 100 KΩ and the pull-up resistor of 1 to 2.2 KΩ.

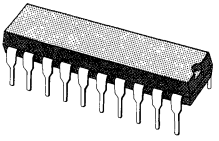
Figure 46.



STEPPER MOTOR CONTROLLERS

- NORMAL/WAWE DRIVE
- HALF/FULL STEP MODES
- CLOCKWISE/ANTICLOCKWISE DIRECTION
- SWITCHMODE LOAD CURRENT REGULATION
- PROGRAMMABLE LOAD CURRENT
- FEW EXTERNAL COMPONENTS
- RESET INPUT & HOME OUTPUT
- ENABLE INPUT
- STEP MULSE SOUBLER (l297a only)

The L297 Stepper Motor Controller IC generates four phase drive signals for two phase bipolar and four phase unipolar step motors in microcomputer-controlled applications. The motor can be driven in half step, normal and wawe drive modes and on-chip PWM chopper circuits permit switch-mode control of the current in the windings. A feature of this device is that it requires only clock, direction and mode input signals. Since the phase are generated internally the burden on the microprocessor, and the programmer, is greatly reduced. Mounted in a 20-pin plastic package, the L297 can be used with monolithic bridge drives such as the L298N or L293E, or with discrete transistors and darlingtons. The L297A also includes a clock pulse doubler.



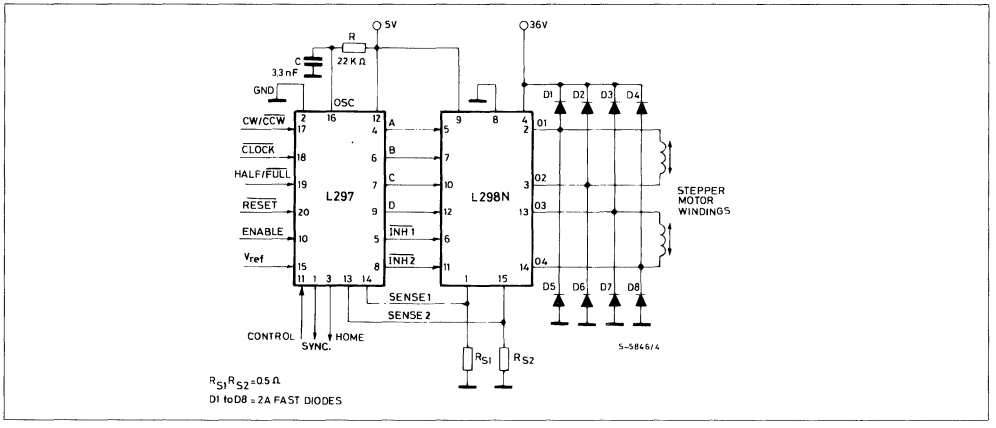
DIP-20 Plastic
(0.25)

ORDER CODES : L297 – L297A

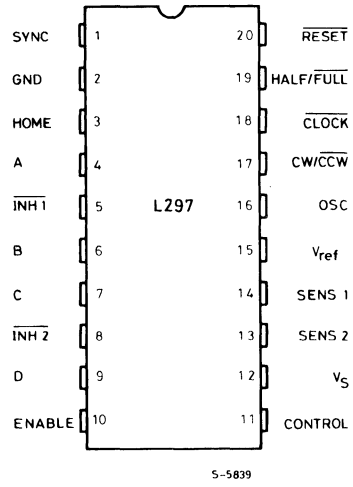
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	10	V
V_i	Input signals	7	V
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	– 40 to + 150	°C

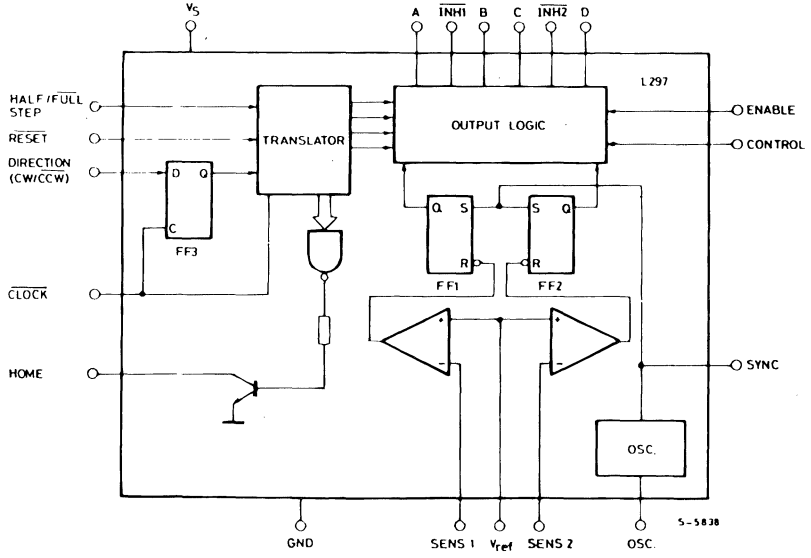
TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT



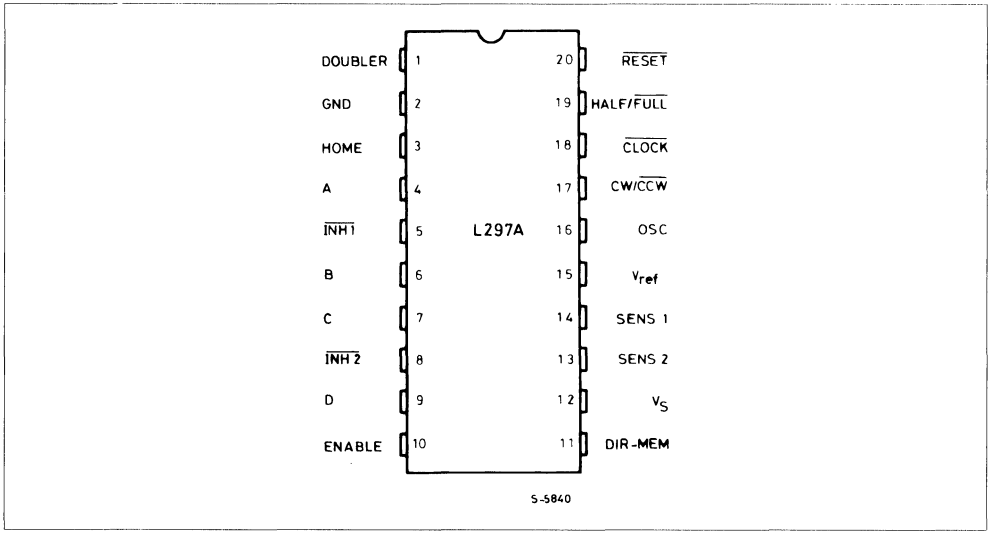
PIN CONNECTION (L297)



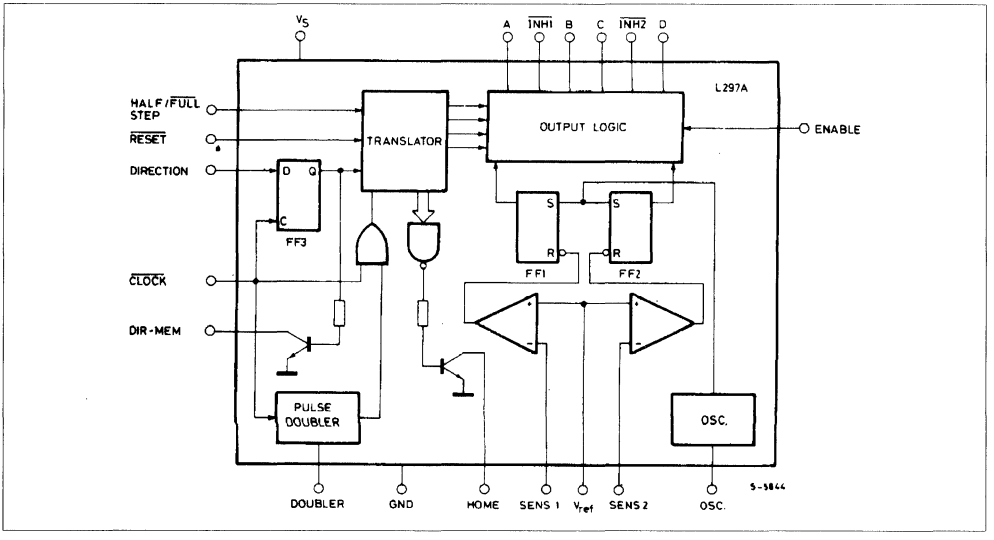
BLOCK DIAGRAM (L297)



PIN CONNECTION (L297A)



BLOCK DIAGRAM (L297A)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

PIN FUNCTIONS – L297

N°	NAME	FUNCTION
1	SYNC	Output of the on-chip chopper oscillator. The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground connection
3	HOME	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	A	Motor phase A drive signal for power stage.
5	$\overline{INH1}$	Active low inhibit control for driver stages of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate load current if CONTROL input is low.
6	B	Motor phase B drive signal for power stage.
7	C	Motor phase C drive signal for power stage.
8	$\overline{INH2}$	Active low inhibit control for drive stages of C and D phases. Same functions as $\overline{INH1}$.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) $\overline{INH1}$, $\overline{INH2}$, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on $\overline{INH1}$ and $\overline{INH2}$; when high chopper acts on phase lines ABCD.
12	V_S	5V supply input.
13	$SENS_2$	Input for load current sense voltage from power stages of phases C and D.
14	$SENS_1$	Input for load current sense voltage from power stages of phases A and B.
15	V_{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V_{CC}, C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69\ RC$, $R > 10k\Omega$.
17	CW/$\overline{CCW}$	Clockwise/counterclockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	$\overline{CLOCK}$	Step clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.

PIN FUNCTIONS – L297 (continued)

N°	NAME	FUNCTION
19	HALF/$\overline{\text{FULL}}$	Half/full step select input. When high selects half step operation, when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (The home position is designate state 1).
20	$\overline{\text{RESET}}$	Reset input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

PIN FUNCTIONS – L297A

Pin function of the L297A are identical to those of the L297 except for pins 1 and 11.

N°	NAME	FUNCTIONS
1	DOUBLER	An RC network connected to this pin determines the delay between an input clock pulse and the corresponding ghost pulse.
11	DIR-MEM	Direction Memory. Inverted output of the direction flip flop. Open collector output.

CIRCUIT OPERATION

The L297(A) is intended for use with a dual bridge driver, quad darlington array or discrete power devices in step motor driving applications. It receives step clock, direction and mode signals from the systems controller (usually a microcomputer chip) and generates control signals for the power stage.

The principal functions are a translator, which generates the motor phase sequences, and a dual PW/M chopper circuit which regulates the current in the motor windings. The translator generates three different sequences, selected by the HALF/$\overline{\text{FULL}}$ input. These are normal (two phases energised), wave drive (one phase energised) and half-step (alternately one phase energised/two phases energised). Two inhibit signals are also generated by the L297 in half step and wave drive modes. These signals, which connect directly to the L298's enable inputs, are intended to speed current decay when a winding is de-energised. When the L297 is used to drive a unipolar motor the chopper acts on these lines.

An input called CONTROL determines whether the chopper will act on the phase lines ABCD or the inhibit lines $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$. When the phase lines are chopped the non-active phase line of each pair (AB or CD) is activated (rather than interrupting the line then active). In L297 + L298 configurations this technique reduces dissipation in the load current sense resistors.

A common on-chip oscillator drives the dual chopper. It supplies pulses at the chopper rate which set the two flip-flops FF1 and FF2. When the current in a winding reaches the programmed peak value the voltage across the sense resistor (connected to one of the sense inputs $SENS_1$ or $SENS_2$) equals V_{ref} and the corresponding comparator resets its flip flop, interrupting the drive current until the next oscillator pulse arrives. The peak current for both windings is programmed by a voltage divider on the V_{ref} input.

Ground noise problems in multiple configurations can be avoided by synchronising the chopper oscillators. This is done by connecting all the SYNC pins together, mounting the oscillator RC network on one device only and grounding the OSC pin on all other devices.

The L297A includes a pulse doubler on the step clock line which is intended to simplify the implementation of multiple stepping. A ghost pulse is generated automatically after each input pulse, delayed by the time $0.75\ R_d\ C_d$.

The RC network should be dimensioned to place the ghost pulse roughly halfway between clock pulses. If pin 1 (DOUBLER) is grounded the doubler function is disabled.

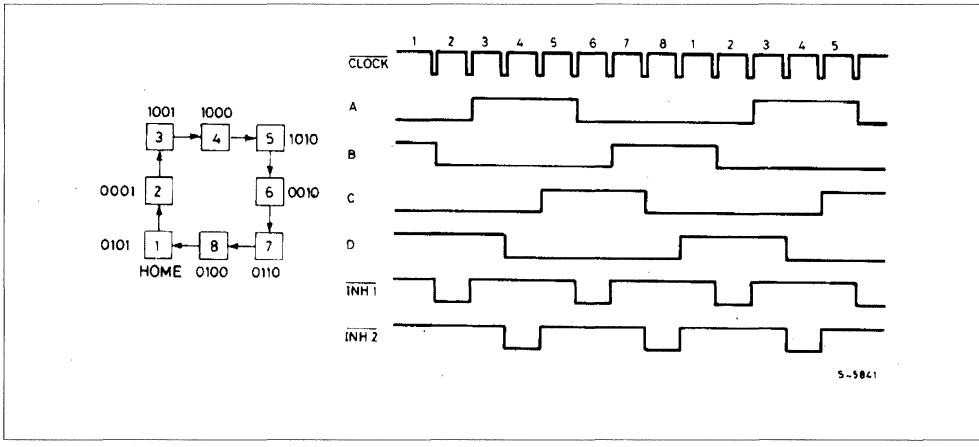
MOTOR DRIVING PHASE SEQUENCES

The L297's translator generates phase sequences for normal drive, wave drive and half step modes. The state sequences and output waveforms for these three modes are shown below. In all cases the translator advances on the low to high transistion of CLOCK.

Clockwise rotation is indicated ; for anticlockwise rotation the sequences are simply reversed RESET restores the translator to state 1, where ABCD = 0101.

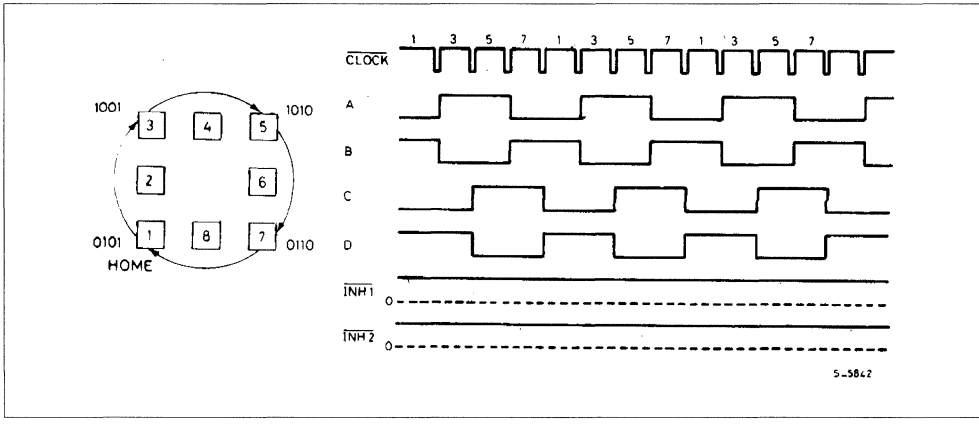
HALF STEP MODE

Half step mode is selected by a high level on the HALF/FULL input.



NORMAL DRIVE MODE

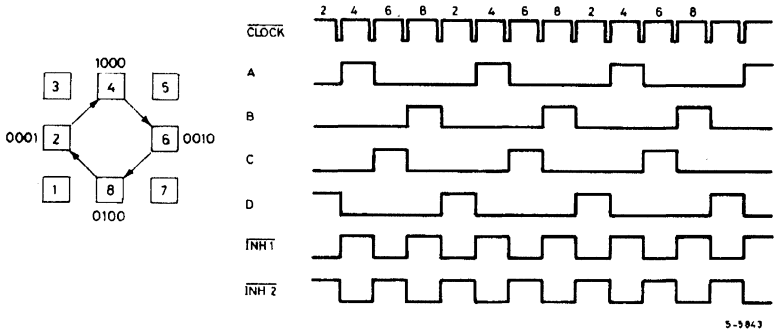
Normal drive mode (also called "two-phase-on" drive) is selected by a low level on the HALF/FULL input when the translator is at an odd numbered state (1, 3, 5 or 7). In this mode the INH1 and INH2 outputs remain high throughout.



MOTOR DRIVING PHASE SEQUENCES (continued)

WAVE DRIVE MODE

Wave drive mode (also called "one-phase-on" drive) is selected by a low level on the HALF/$\overline{\text{FULL}}$ input when the translator is at an even numbered state (2, 4, 6 or 8).



ELECTRICAL CHARACTERISTICS (Refer to the block diagram T_{amb} = 25°C, V_S = 5V unless otherwise specified)

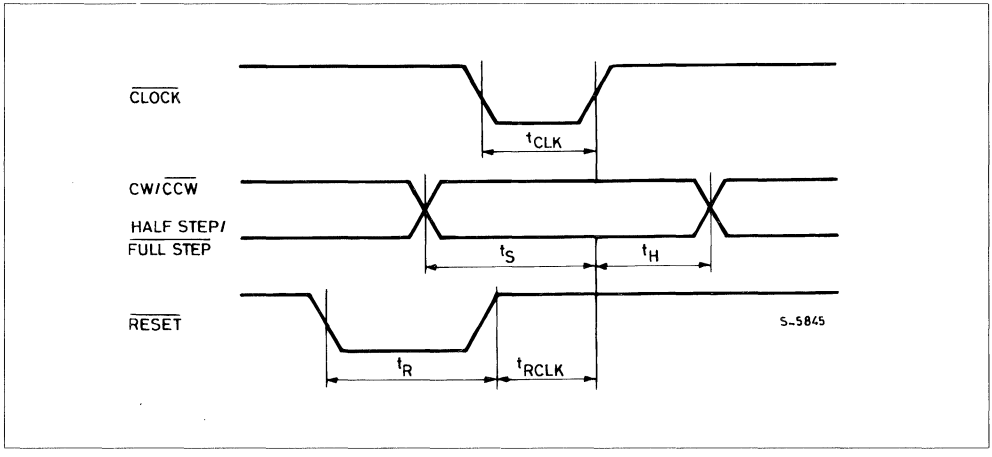
Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_S	Supply voltage (pin 12)			4.75		7	V
I_S	Quiescient supply current (pin 12)	Outputs floating			50	80	mA
V_i	Input voltage (pin 11, 17, 18, 19, 20)		Low			0.8	V
			High	2		V_S	V
I_i	Input current (pin 11, 17, 18, 19, 20)		V_i = L			– 100	µA
			V_i = H			10	µA
V_{en}	Enable input voltage (pin 10)		Low			1.5	V
			High	2		V_S.	V
I_{en}	Enable input current (pin 10)		V_{en} = L			– 100	µA
			V_{en} = H			10	µA
V_o	Phase output voltage (pins 4, 6, 7, 9)	I_o = 10mA	V_{OL}			0.4	V
		I_o = 5mA	V_{OH}	3.9			V
V_{inh}	Inhibit output voltage (pins 5, 8)	I_o = 10mA	$V_{inh\,L}$			0.4	V
		I_o = 5mA	$V_{inh\,H}$	3.9			V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_{leak}	Leakage current (pin 3, 11*)	V_{CE} = 7 V			1	µA
V_{sat}	Saturation voltage (pins 3, 11*)	I = 5 mA			0.4	V
V_{off}	Comparators offset voltage (pins 13, 14, 15)	V_{ref} = 1 V			5	mV
I_b	Comparator bias current (pins 13, 14, 15)		– 100		10	µA
V_{ref}	Input reference voltage (pin 15)		0		3	V
t_{CLK}	Clock time		0.5			µs
t_S	Set up time		1			µs
t_H	Hold time		4			µs
t_R	Reset time		1			µs
t_{RCLK}	Reset to clock delay		1			µs

* L297A only

Figure 1.



APPLICATION INFORMATION

TWO PHASE BIPOLAR STEPPER MOTOR CONTROL CIRCUIT

This circuit drives bipolar stepper motors with winding currents up to 2A. The diodes are fast 2A types.

Figure 2.

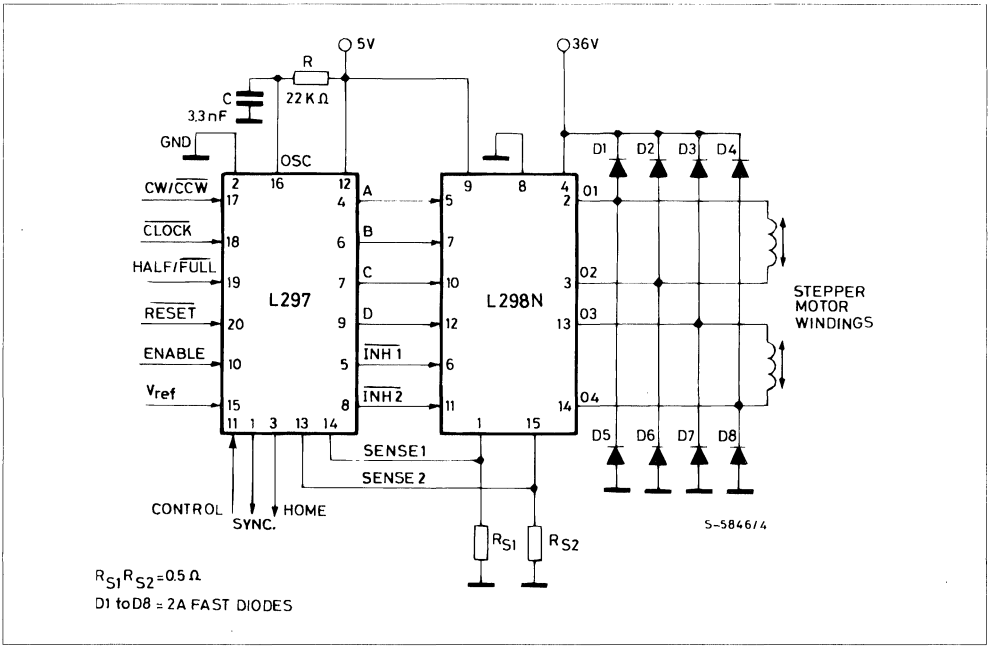


Figure 3 : Synchronising L297s

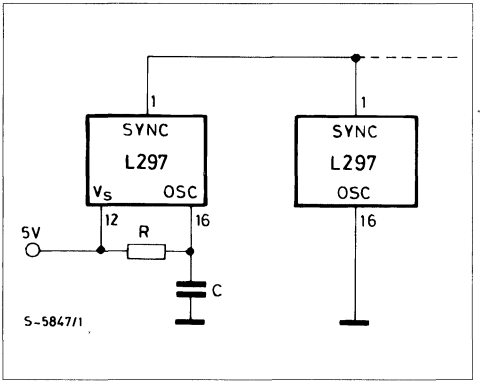
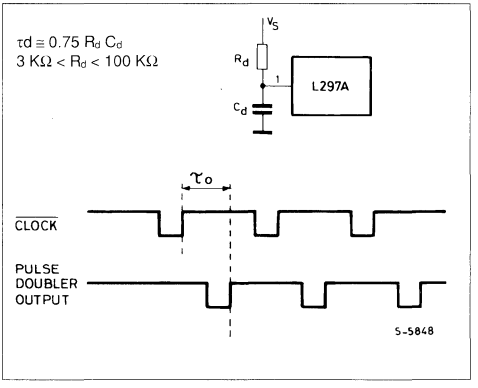


Figure 4 : Pulse doubler (L297A)



DUAL FULL-BRIDGE DRIVER

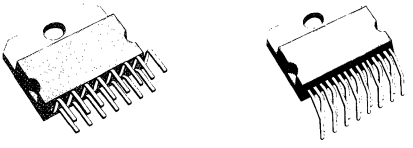
PRELIMINARY DATA

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)

DESCRIPTION

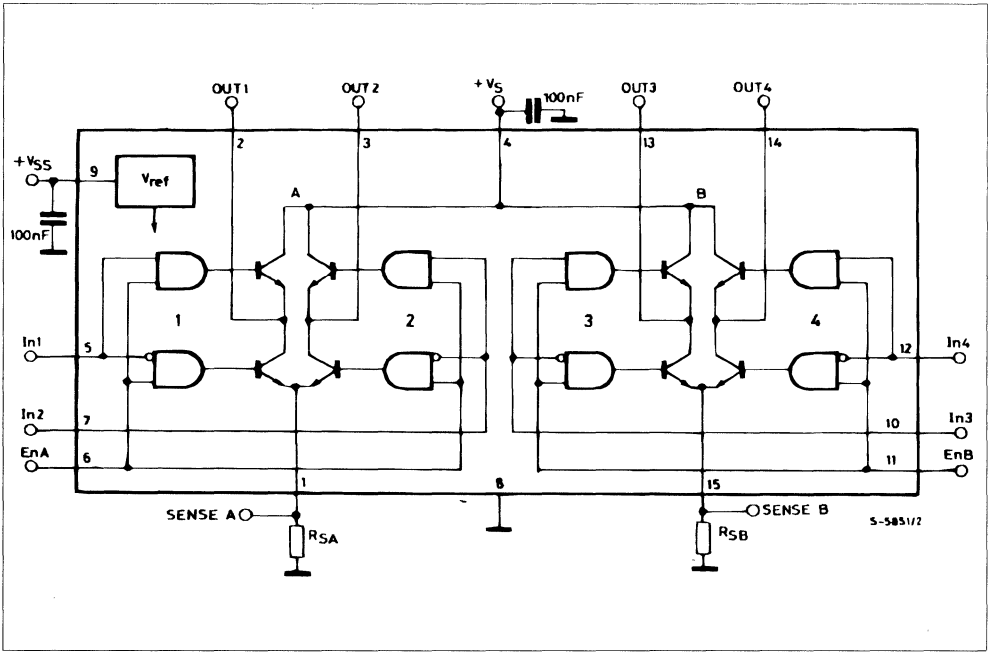
The L298N is an integrated monolithic circuit in a 15-lead Multiwatt® package. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

Multiwatt
(15-lead)



ORDER CODES : L298N
L298HN

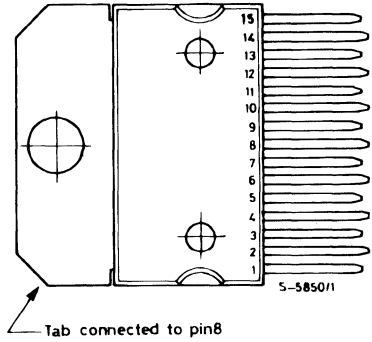
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_I, V_{en}	Input and Enable Voltage	– 0.3 to 7	V
I_O	Peak Output Current (each channel) - Non Repetitive (t = 100 µs) - Repetitive (80 % on – 20 % off ; t_{on} = 10 ms) - DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	– 1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75 °C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	° C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	° C/W

PIN FUNCTIONS (refer to the block diagram)

N°	Name	Function
1 ; 15	Sense A ; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2 ; 3	Out 1 ; Out 2	Outputs of the Bridge A ; the current that flows through the load connected between these two pins is monitored at pin 1.
4	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100 nF capacitor must be connected between this pin and ground.
5 ; 7	Input 1 ; Input 2	TTL Compatible Inputs of the Bridge A.
6 ; 11	Enable A ; Enable B	TTL Compatible Enable Input : the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	GND	Ground.
9	V_{SS}	Supply Voltage for the Logic Bloks. A 100 nF capacitor must be connected between this pin and ground.
10 ; 12	Input 3 ; Input 4	TTL Compatible Inputs of the Bridge B.
13 ; 14	Out 3 ; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.

ELECTRICAL CHARACTERISTICS (V_S = 42 V ; V_{SS} = 5 V, T_j = 25 °C ; unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition		V_{IH} + 2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)			4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H I_L = 0	V_i = L		13	22	mA
			V_i = H		50	70	
		V_{en} = L	V_i = x			4	
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H I_L = 0	V_i = L		24	36	mA
			V_i = H		7	12	
		V_{en} = L	V_i = x			6	
V_{iL}	Input Low Voltage (pins 5,7,10,12)			− 0.3		1.5	V
V_{iH}	Input High Voltage (pins 5,7,10,12)			2.3		V_{SS}	
I_{iL}	Low Voltage Input Current (pins 5,7,10,12)	V_i = L				− 10	µA
I_{iH}	High Voltage Input Current (pins 5,7,10,12)	V_i = H ≤ V_{SS} − 0.6 V			30	100	
V_{en} = L	Enable Low Voltage (pins 6,11)			− 0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6,11)			2.3		V_{SS}	
I_{en} = L	Low Voltage Enable Current (pins 6,11)	V_{en} = L				− 10	µA
I_{en} = H	High Voltage Enable Current (pins 6,11)	V_{en} = H ≤ V_{SS} − 0.6 V			30	100	
$V_{CE\ sat\ (H)}$	Source Saturation Voltage	I_L = 1 A			1.35	1.7	V
		I_L = 2 A			2	2.7	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CE\ sat\ (L)}$	Sink Saturation Voltage	I_L = 1 A (5)		1.2	1.6	V
		I_L = 2 A (5)		1.7	2.3	
$V_{CE\ sat}$	Total Drop	I_L = 1 A (5)			3.2	V
		I_L = 2 A (5)			4.9	
V_{sens}	Sensing Voltage (pins 1, 15)		− 1 (1)		2	V
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2) ; (4)		1.5		µs
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2) ; (4)		0.2		µs
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2) ; (4)		2		µs
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2) ; (4)		0.7		µs
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3) ; (4)		0.7		µs
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3) ; (4)		0.25		µs
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3) ; (4)		1.6		µs
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3) ; (4)		0.2		µs
f_c (V_i)	Commutation Frequency	I_L = 2 A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2) ; (4)		3		µs
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2) ; (4)		1		µs
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2) ; (4)		0.3		µs
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2) ; (4)		0.4		µs
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3) ; (4)		2.2		µs
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3) ; (4)		0.35		µs
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (3) ; (4)		0.25		µs
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3) ; (4)		0.1		µs
f_c (V_{en})	Commutation Frequency	I_L = 2 A		1		KHz

1) Sensing voltage can be −1 V for t ≤ 50 µsec; in steady state V_{sens} min ≥ − 0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.
5) PIN 1 and PIN 15 connected to GND.

Figure 1 : Typical Saturation Voltage vs. Output Current.

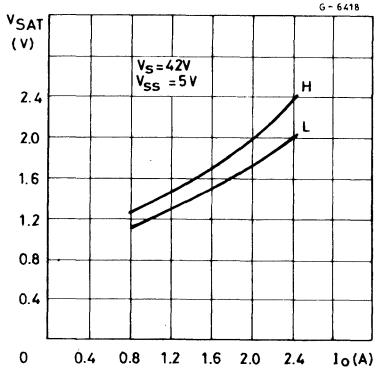
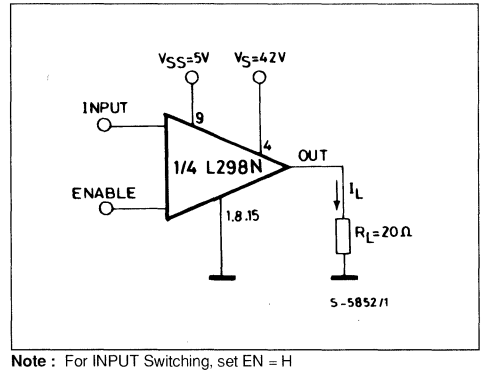


Figure 2 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = H

Figure 3 : Source Current Delay Times vs. Input or Enable Switching.

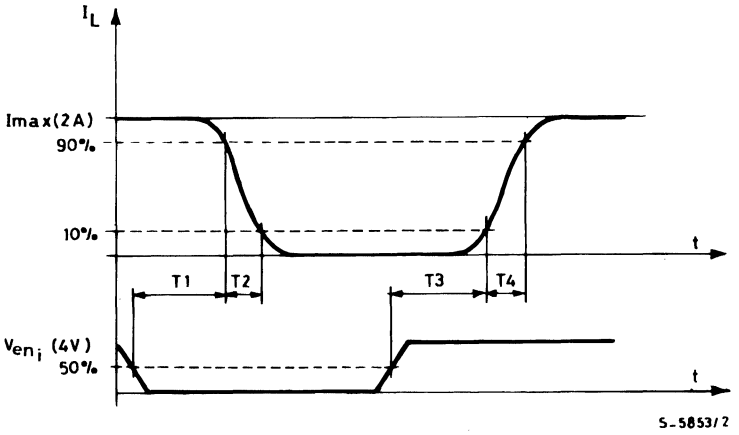
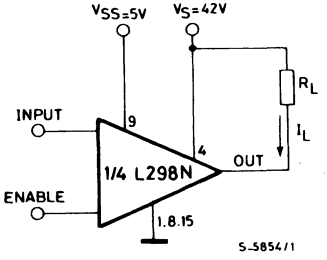


Figure 4 : Switching Times Test Circuits.



Note : For INPUT Switching, set EN = H
For ENABLE Switching, set IN = L

Figure 5 : Sink Current Delay Times vs. Input 0 V Enable Switching.

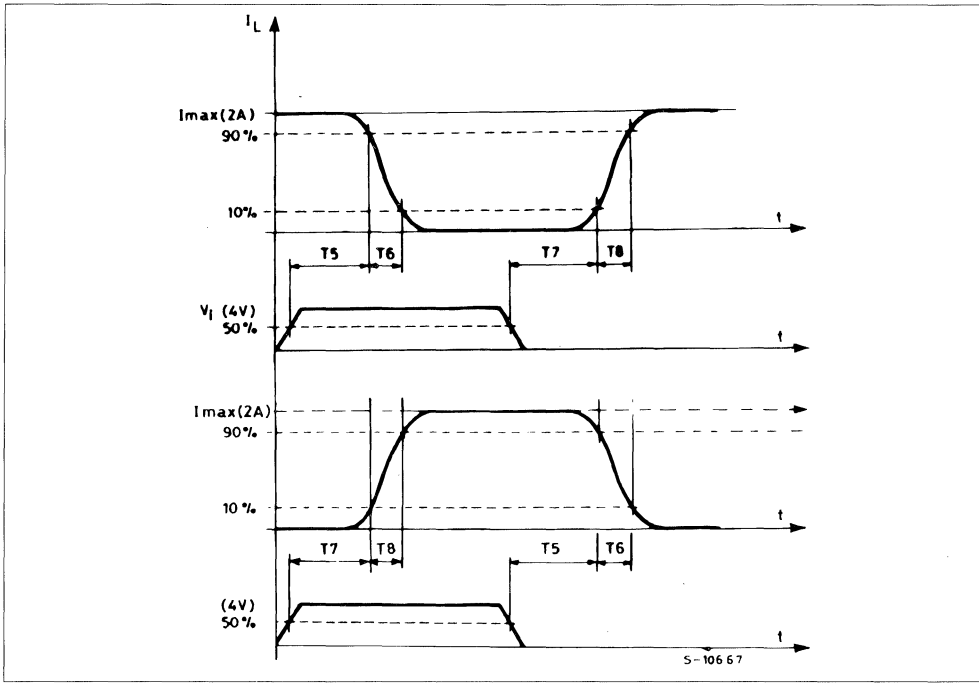
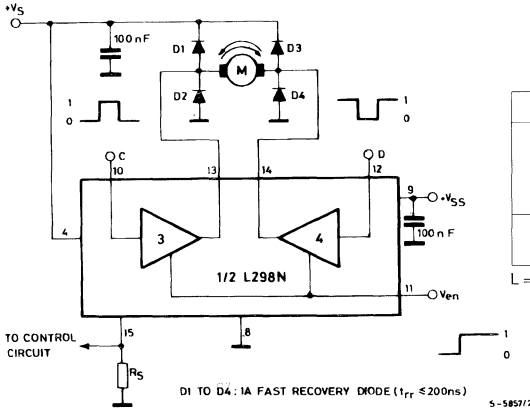


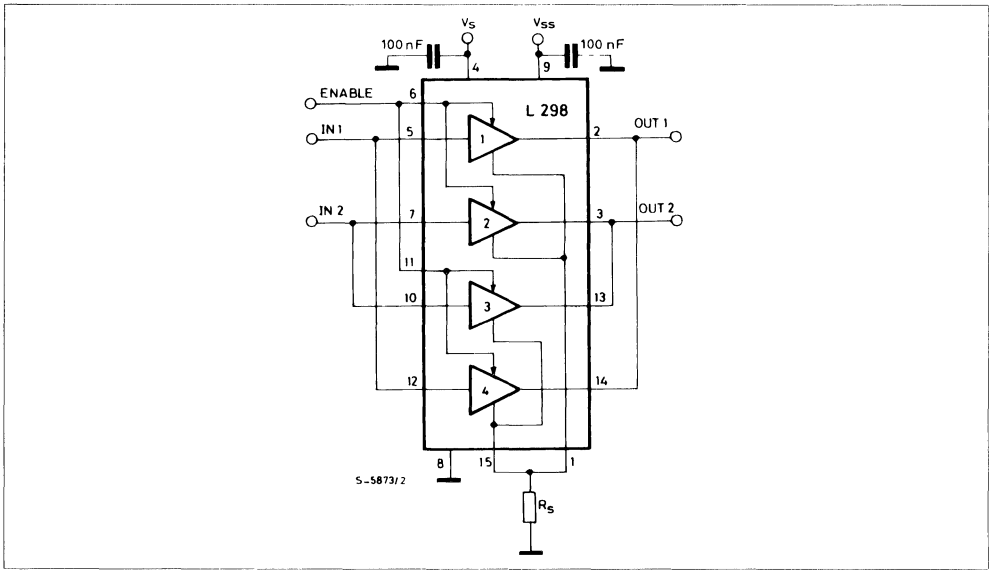
Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Turn Right
	C = L ; D = H	Turn Left
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = C	Free Running Motor Stop

L = Low H = High X = Don't care

Figure 7 : For higher currents, outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



APPLICATION INFORMATION (Refer to the block diagram)

1.1. POWER OUTPUT STAGE

The L298N integrates two power output stages (A ; B). The power output stage is a bridge configuration and its outputs can drive an inductive load in common or differenzial mode, depending on the state of the inputs. The current that flows through the load comes out from the bridge at the sense output : an external resistor (R_{SA} ; R_{SB}.) allows to detect the intensity of this current.

1.2. INPUT STAGE

Each bridge is driven by means of four gates the input of which are In1 ; In2 ; EnA and In3 ; In4 ; EnB. The In inputs set the bridge state when The En input is high ; a low state of the En input inhibits the bridge. All the inputs are TTL compatible.

2. SUGGESTIONS

A non inductive capacitor, usually of 100 nF, must be foreseen between both Vs and Vss, to ground, as near as possible to pin 8 (GND). When the large capacitor of the power supply is too far from the IC, a second smaller one must be foreseen near the L298N.

The sense resistor, not of a wire wound type, must be grounded near the negative pole of Vs that must be near the GND pin of the I.C.

Each input must be connected to the source of the driving signals by means of a very short path.

Turn-On and Turn-Off : Before to Turn-ON the Supply Voltage and before to Turn it OFF, the Enable input must be driven to the Low state.

3. APPLICATIONS

Fig 6 shows a bidirectional DC motor control Schematic Diagram for which only one bridge is needed. The external bridge of diodes D1 to D4 is made by four fast recovery elements (trr $\leq$ 200 nsec) that must be chosen of a VF as low as possible at the worst case of the load current.

The sense output voltage can be used to control the current amplitude by chopping the inputs, or to provide overcurrent protection by switching low the enable input.

The brake function (Fast motor stop) requires that the Absolute Maximum Rating of 2 Amps must never be overcome.

When the repetitive peak current needed from the load is higher than 2 Amps, a paralleled configuration can be chosen (See Fig.7).

An external bridge of diodes are required when inductive loads are driven and when the inputs of the

IC are chopped ; Shottky diodes would be preferred.

This solution can drive until 3 Amps In DC operation and until 3.5 Amps of a repetitive peak current.

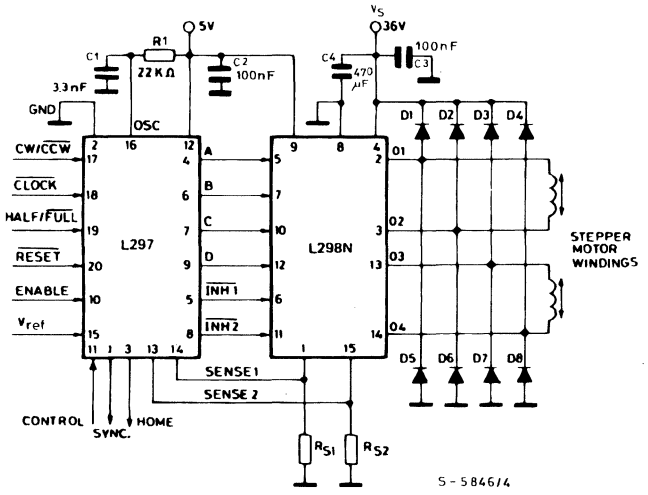
On Fig 8 it is shown the driving of a two phase bipolar stepper motor ; the needed signals to drive the inputs of the L298N are generated, in this example, from the IC L297.

Fig 9 shows an example of P.C.B. designed for the application of Fig 8.

Fig 10 shows a second two phase bipolar stepper motor control circuit where the current is controlled by the I.C. L6506.

Figure 8 : Two Phase Bipolar Stepper Motor Circuit.

This circuit drives bipolar stepper motors with winding currents up to 2 A. The diodes are fast 2 A types.



$R_{S1} = R_{S2} = 0.5\ \Omega$

D1 to D8 = 2 A Fast diodes { $V_F \leq 1.2$ V @ I = 2 A ; trr ≤ 200 ns

Figure 9: Suggested Printer Circuit Board Layout for the Circuit of fig. 8 (1 : 1 scale)

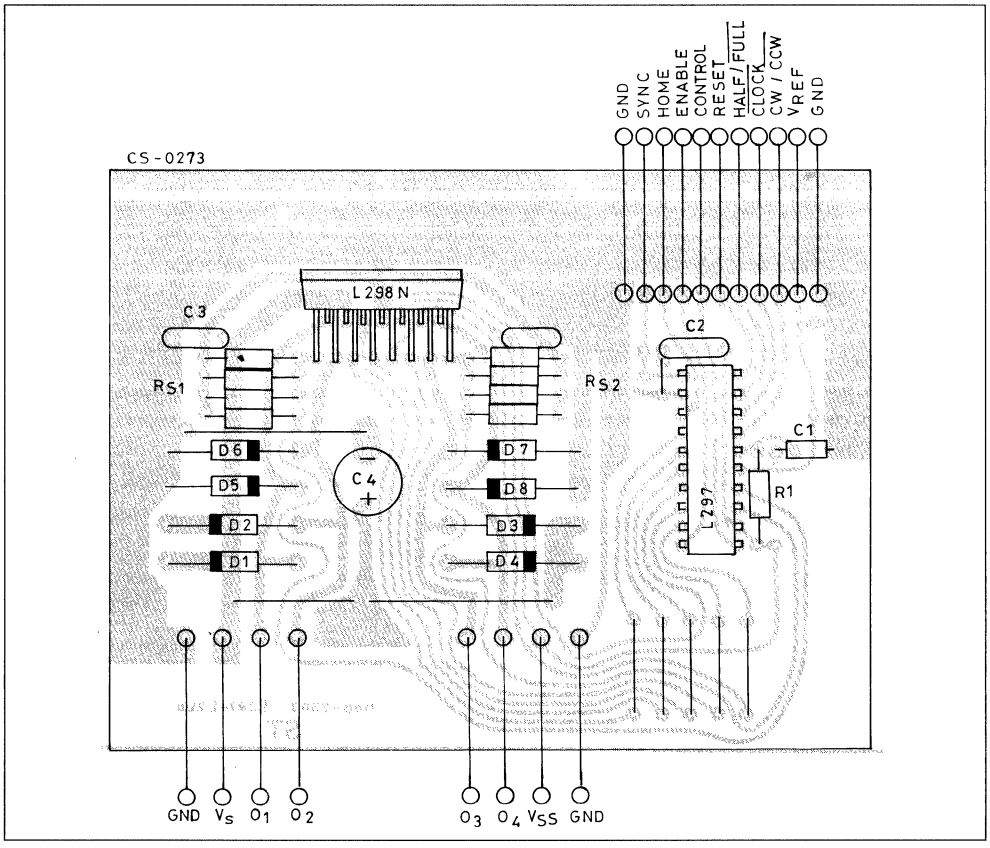
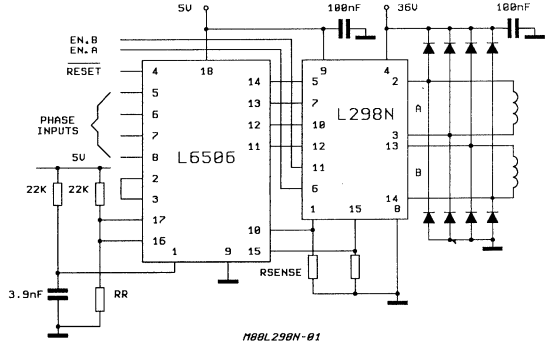


Figure 10: Two Phase Bipolar Stepper Motor Control Circuit by Using the Current Controller L6506.

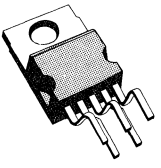


R_R and R_{sense} depend from the load current

VERY LOW DROP 5V REGULATOR

- PRECISE OUTPUT VOLTAGE (5 V ± 4 %)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)
- HIGH NOISE IMMUNITY ON RESET DELAY CAPACITOR

L387A particularly suitable for microprocessor systems. This output provides a reset signal when power is applied (after an external programmable delay) and goes low when power is removed, inhibiting the microprocessor. An hysteresis on reset delay capacitor raises the immunity to the ground noise.



Pentawatt®

ORDER CODE : L387A

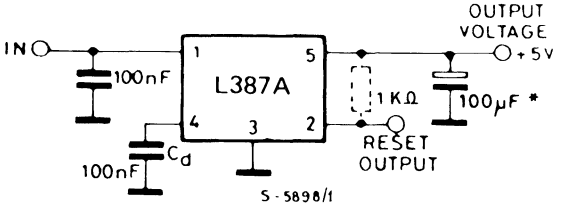
DESCRIPTION

The L387A is a very low drop voltage regulator in a Pentawatt® package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the

ABSOLUTE MAXIMUM RATINGS

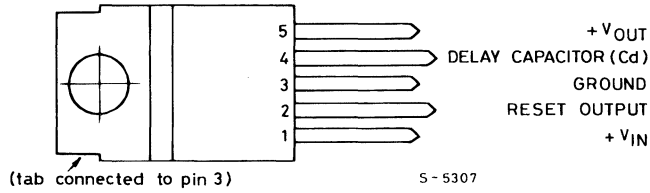
Symbol	Parameter	Value	Unit
V_i	Forward Input Voltage	35	V
T_{op}	Operating Temperature Range	– 40 to + 125	°C
T_{stg}, T_J	Storage and Junction Temperature	– 40 to + 150	°C

APPLICATION CIRCUIT

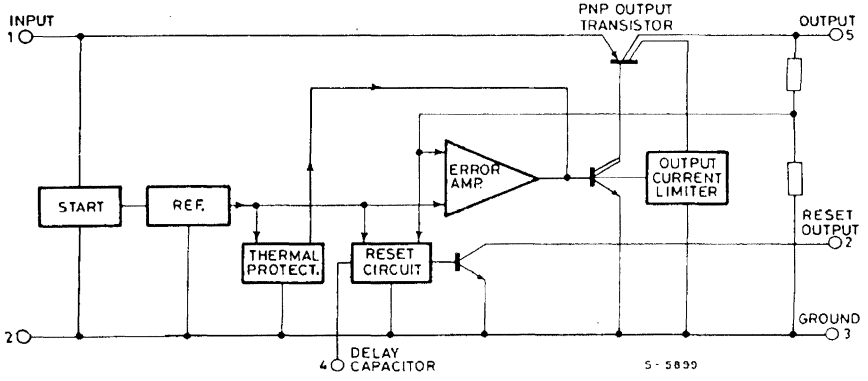


* Min 33 µF and max. ESR ≤ 3 Ω over temperature range.

CONNECTION DIAGRAM (top views)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14.4 V, T_j = 25 °C, C_o = 100 µF; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 5 mA to 500 mA T_j = 25 °C $-40 \le T_j \le 125$ °C	4.80 4.75	5.00 5.00	5.20 5.25	V
V_I	Operating Input Voltage	(*), Over Full T Range (– 40 to 125 °C) (see note **)			26	V
ΔV_o	Line Regulation	V_i = 6 V to 26 V I_o = 5 mA		5	50	mV
ΔV_o	Load Regulation	I_o = 5 mA to 500 mA		15	60	mV
$V_I - V_o$	Dropout Voltage	I_o = 350 mA I_o = 500 mA $V_O = V_{O\ NOM} - 100$ mV		0.40 0.60	0.65 0.8	V
I_q	Quiescent Current	I_o = 0 mA I_o = 150 mA I_o = 350 mA I_o = 500 mA		5 20 60 100	15 35 100 160	mA
		V_i = 6.2 V I_o = 500 mA		160	180	
$\frac{\Delta V_o}{\Delta T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Voltage Rejection	I_o = 350 mA f = 120 Hz C_o = 100 µF V_i = 12 V ± 5 V_{pp}		60		dB
I_{SC}	Output Short Circuit Current			1.2	1.6	A
V_R	Reset Output Voltage	I_R = 3 mA 1 < V_o < 4.75 V I_R = 16 mA 1.5 < V_o < 4.75 V Over Full T (– 40 °C ≤ T_j ≤ 125 °C)			0.5 0.8	V
I_R	Reset Output Leakage Current	V_o in Regulation Over Full T Range			50	µA
t_d	Delay Time for Reset Output	Cd = 100 nF Over Full T Range		25		ms
$V_{RT\ (off)}$		V_o @ Reset out H to L Transition, Over Full T Range	4.75	V_o – 0.15		V
I_{C4}	Charging Current (current generator)	V_4 = 3 V	10	20	30	µA
$V_{RT\ (on)}$	Power on V_o Threshold	V_o @ Reset out L to H Transition , Over Full T Range		$V_{RT\ (off)}$ + 0.05 V	V_o – 0.04 V	V
V_4	Comparator Threshold (pin 4)	V_4 @ Reset out H to L Transition	3.2		3.9	V
		V_4 @ Reset out L to H Transition	3.7		4.3	V
V_H	Hysteresis Voltage	Over Full T Range		450		mV

(*) For a DC voltage 26 < Vi < 35 V the device is not operating.
(**) Design limits are guaranteed (but not 100 % production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Figure 1 : Dropout Voltage vs. Output Current.

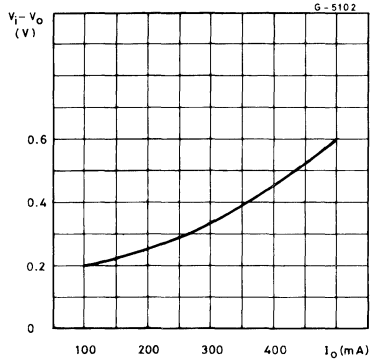


Figure 2 : Quiescent Current vs. Output Current.

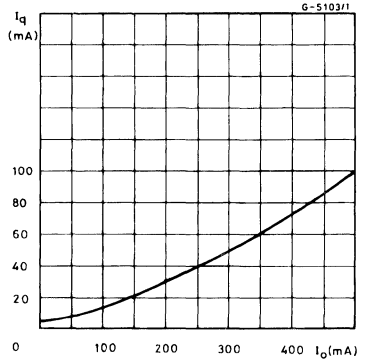
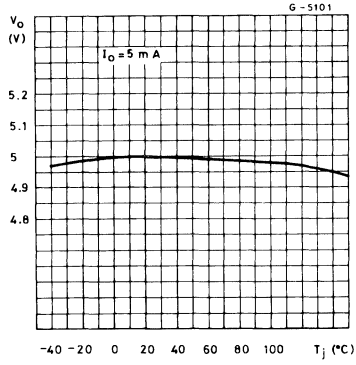


Figure 3 : Output Voltage vs. Temperature.



SGS-THOMSON MICROELECTRONICS

L601-L603
L602-L604

DARLINGTON ARRAYS

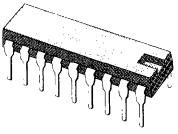
- EIGHT DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 400 mA PER DRIVER (500 mA PEAK)
- OUTPUT VOLTAGE 90 V ($V_{CE\ (sus)}$ = 70 V)
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL / CMOS / PMOS / DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

The four versions interface to all common logic families :

L601	General purpose
L602	14 - 25 V PMOS
L603	5 V TTL, CMOS
L604	6 - 15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads, including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The L601, L602, L603 and L604 are supplied in 18 pin plastic DIP packages with a copper leadframe to reduce thermal resistance.



DIP-18
(Plastic)

ORDER CODES : L601C, L603B
L602B, L604B

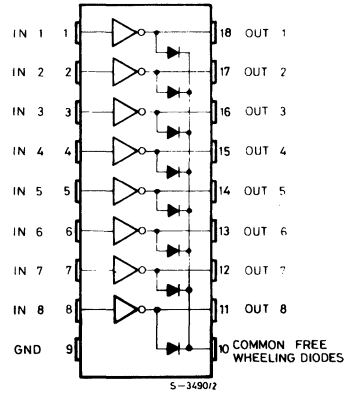
DESCRIPTION

The L601, L602, L603 and L604 are high voltage, high current darlington arrays each containing eight open collector darlington pairs with common emitters. Each channel is rated at 400 mA and can with stand peak currents of 500 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

ABSOLUTE MAXIMUM RATINGS

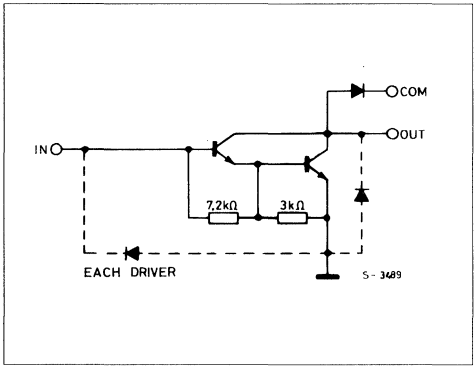
Symbol	Parameter	Value	Unit
V_{CEX}	Collector Emitter Voltage (input open)	90	V
I_C	Collector Current	0.4	A
I_C	Collector Peak Current	0.5	A
V_i	Input Voltage (for L602, L603 and L604)	30	V
I_i	Input Current (for L601 only)	25	mA
P_{tot}	Total Power Dissipation a T_{amb} = 25°C	1.8	W
T_{op}	Operating Junction Temperature	– 25 to 150	°C

PIN CONNECTIONS (top view)

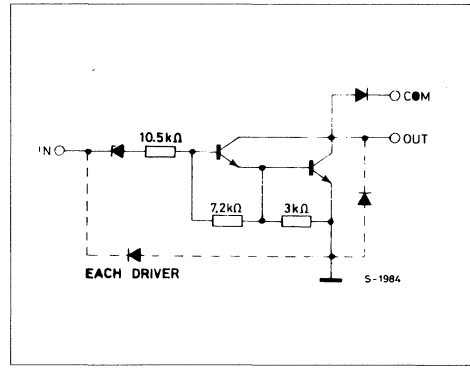


SCHEMATIC DIAGRAMS

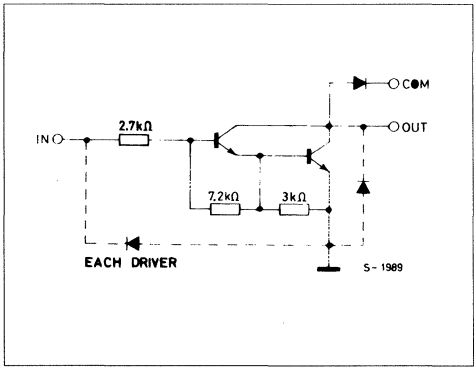
L601



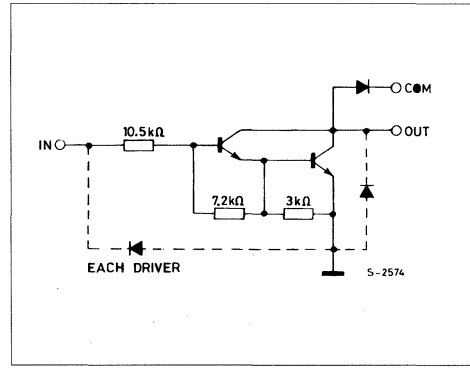
L602



L603



L604



THERMAL DATA

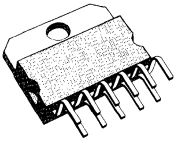
$R_{th\,j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

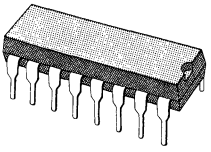
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current	V_{CE} = 90 V			10	µA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage	I_C = 300 mA I_B = 500 µA I_C = 200 mA I_B = 350 µA I_C = 100 mA I_B = 250 µA			2 1.7 1.2	V V V
h_{FE}	DC Forward Current Gain (L601 only)	V_{CE} = 3 V I_C = 300 mA	1000			–
V_i	Minimum Input Voltage (ON condition)	V_{CE} = 3 V I_C = 300 mA for L602 for L603 for L604			 11.5 2.5 5	 V V V
V_i	Maximum Input Voltage (OFF condition)	V_{CE} = 90 V I_C = 25 µA for L601 for L602 for L603 for L604	 0.55 7 0.75 1			 V V V V
I_R	Clamp Diode Reverse Current	V_R = 90 V			50	µA
V_F	Clamp Diode Forward Voltage	I_F = 300 mA		2	2.4	V
t_{on}	Turn-on Delay	0.5 V_i to 0.5 V_o		0.4		µs
t_{off}	Turn-off Delay	0.5 V_i to 0.5 V_o		0.4		µs

2A QUAD DARLINGTON SWITCH

- SUSTAINING VOLTAGE : 70 V
- 2 A OUTPUT
- HIGH CURRENT GAIN
- IDEAL FOR DRIVING SOLENOIDS, DC MOTORS, STEPPER MOTORS, RELAYS, DISPLAYS, ETC.



Multiwatt-11



Powerdip 8 + 8

ORDER CODES : L702B - Powerdip
L702N - Multiwatt

DESCRIPTION

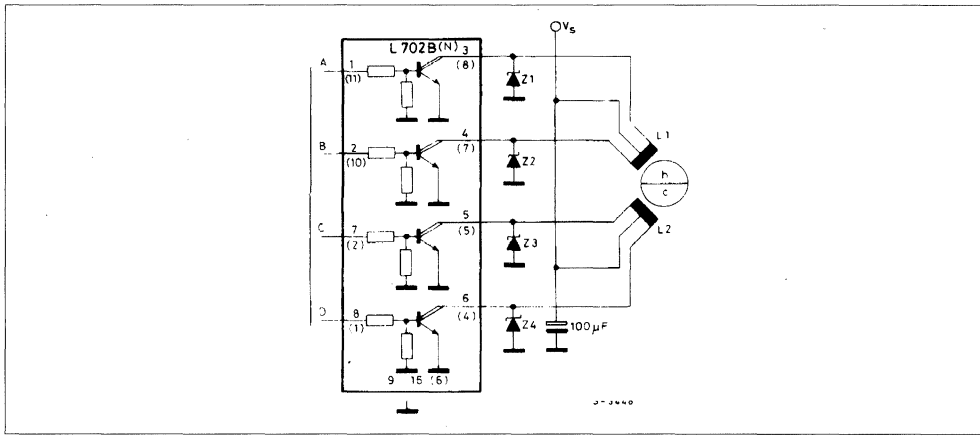
The L702 is a monolithic integrated circuit for high current and high voltage switching applications. It comprises four darlington transistors with common emitter and open collector suitable for current sinking applications mounted on the new POWERDIP and Multiwatt® packages.

This circuit reduces components, sizes and costs ; it can provide direct interface between low level logic and a variety of high current applications.

ABSOLUTE MAXIMUM RATINGS

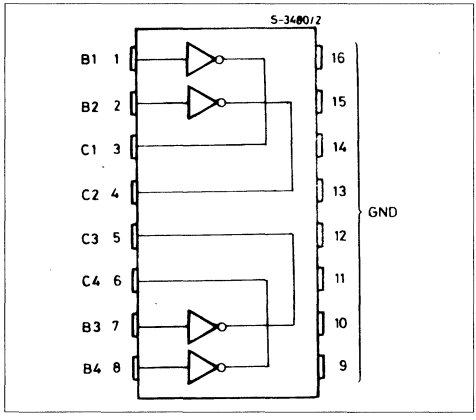
Symbol	Parameter		Value	Unit
V_{CEX}	Collector-emitter Voltage (input open)		90	V
V_i	Input Voltage		30	V
I_C	Collector Current		3	A
P_{tot}	Total Power Dissipation at T_{pin} 9 to 16 ≤ 90 °C	Powerdip	4	W
	Total Power Dissipation at T_{amb} ≤ 70 °C	Powerdip	1.1	W
	Total Power Dissipation at T_{case} ≤ 90 °C	Multiwatt	20	W
T_{stg}	Storage Temperature		– 55 to 150	°C
T_j	Operating Junction Temperature		– 25 to 150	°C

STEPPING MOTOR BUFFER

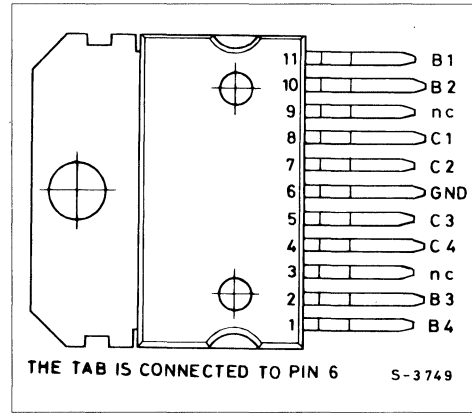


CONNECTION DIAGRAMS (top view)

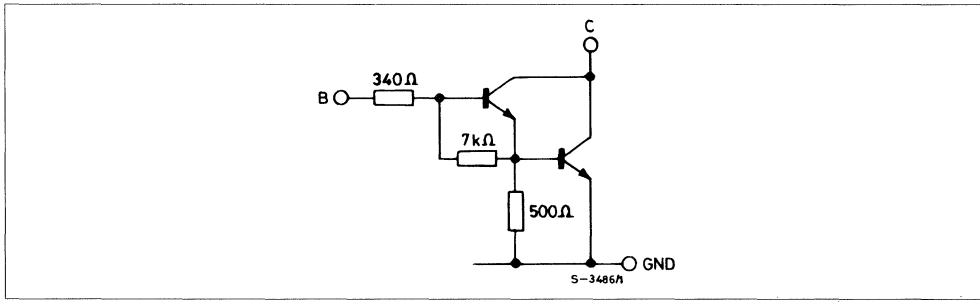
Powerdip



Multiwatt



SCHEMATIC DIAGRAM (each Darlington)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient	} Powerdip	Max	70	°C/W
$R_{th\ j\text{-}pins\ 9/16}$	Thermal Resistance Junction Pins 9 to 16		Max	14	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Multiwatt	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter		Test conditions		Min.	Typ.	Max.	Unit
I_{CEX}	Output Leakage Current		V_{CE} = 90 V			10	50	µA
$V_{CE(sust)}$	Collector Emitter (*) Sustaining Voltage		I_C = 100 mA		70			V
$V_{CE(sat)}$	Collector Emitter Saturation Voltage		I_C = 1.25 A I_i = 2 mA			1.3	1.9	V
h_{FE}	DC Forward Current Gain		I_C = 1 A V_{CE} = 3 V		1 000	4 000		
I_i	Input Current		V_i = 3.75 V V_i = 2.4 V Open Collector			7 3	11 6	mA mA
V_i	Input Voltage	Off Condition	V_{CE} = 70 V	$I_C \leq$ 0.1 mA			0.4	V
		On Condition	V_{CE} = 3 V	$I_C \geq$ 1 A	2.4			V
T_{on}	Turn On Time		V_s = 12 V			0.3		µs
T_{off}	Turn Off Time		R_L = 10 Ω			1		µs

Figure 1 : Switching Time.

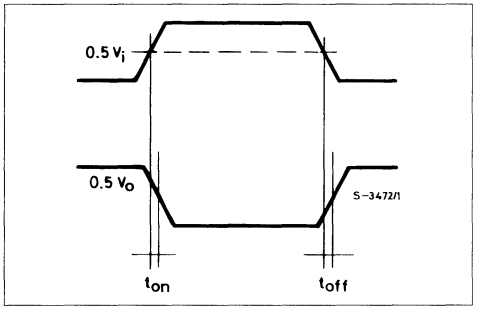


Figure 2 : t_{on} and t_{off} Test Circuit.

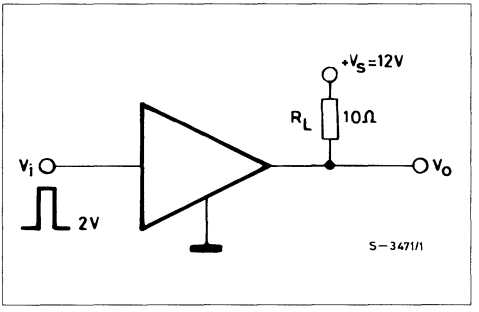


Figure 3 : Peak Collector Current vs. Duty Cycle and Number of Outputs (L702B only).

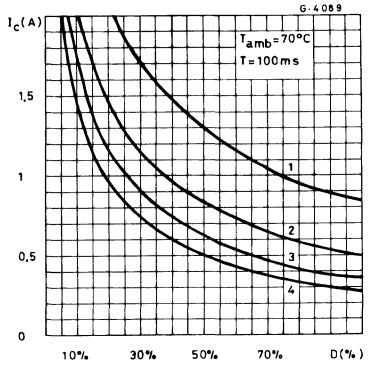


Figure 4 : Collector Emitter Saturation Voltage vs. Collector Current.

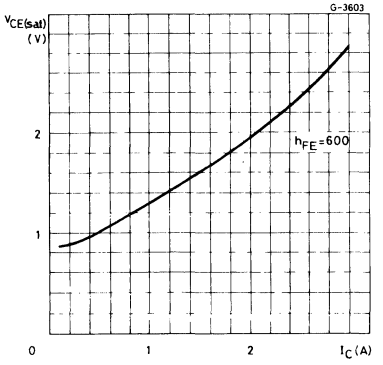


Figure 5 : Collector Current vs. Input Voltage.

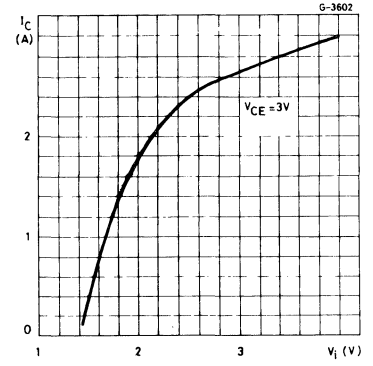


Figure 6 : Input Current vs. Input Voltage.

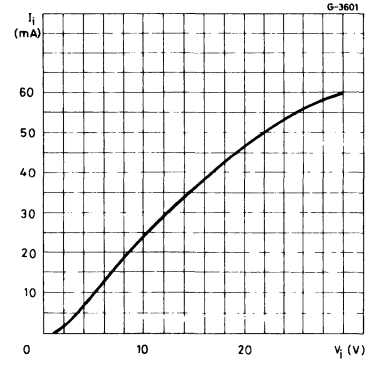


Figure 7 : Safe Operating Areas (L702B).

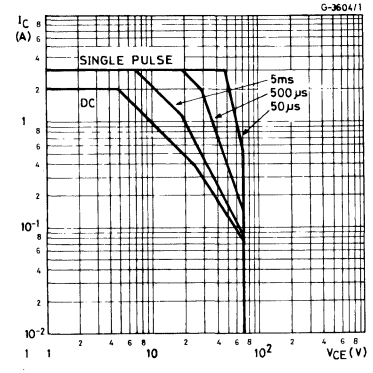
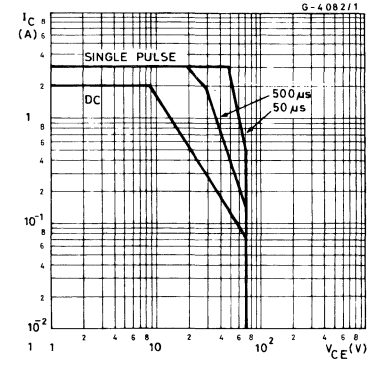


Figure 8 : Safe Operating Areas (L702N).



LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

PRELIMINARY DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

Powerdip (8 + 8) | **Minidip Plastic** | **SIP-9**

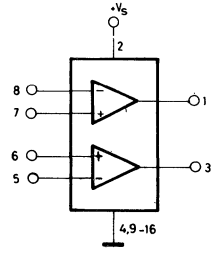
ORDERING NUMBERS:

L2720 L2722 L2724

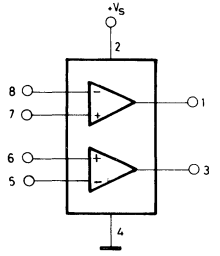
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C (**L2720**), T_{amb} = 50°C (**L2722**)	1	W
	T_{case} = 75°C (**L2720**)	5	W
	T_{case} = 50°C (**L2724**)	10	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

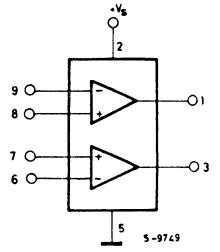
BLOCK DIAGRAMS



L2720

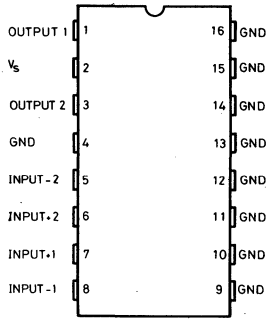


L2722

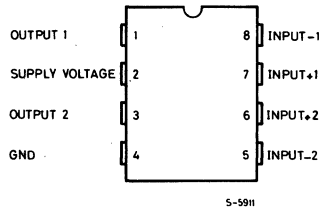


L2724

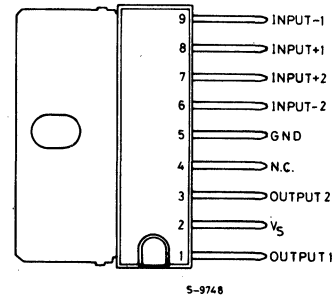
CONNECTION DIAGRAMS
(Top view)



L2720

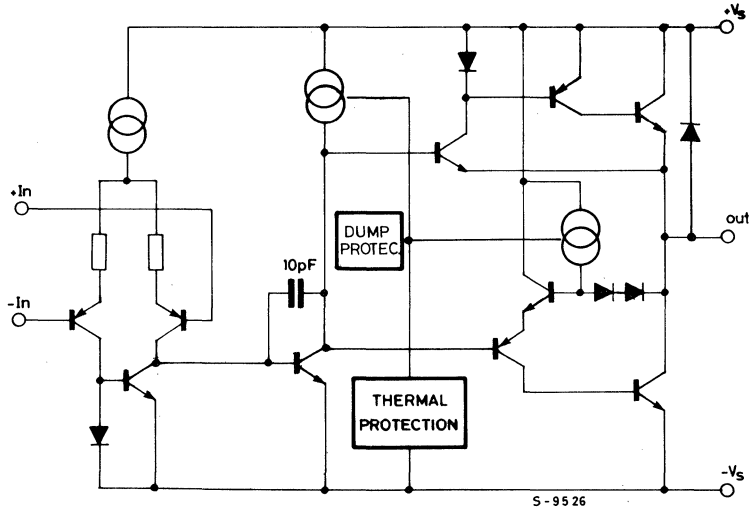


L2722



L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	
I_s	Quiescent drain current	$V_O = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

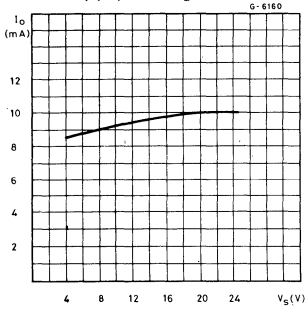


Fig. 2 - Open loop gain vs. frequency

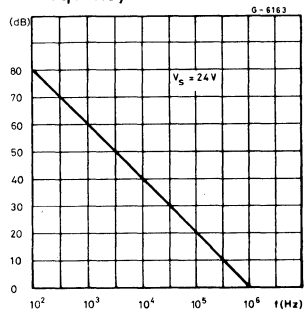


Fig. 3 - Common mode rejection vs. frequency

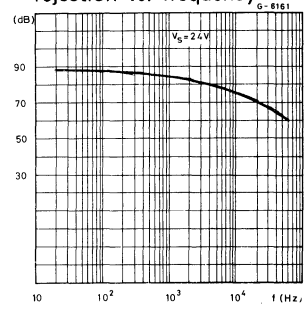


Fig. 4 - Output swing vs. load current (V_s = ± 5V)

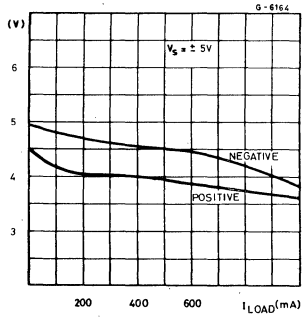


Fig. 5 - Output swing vs. load current (V_s = ± 12V)

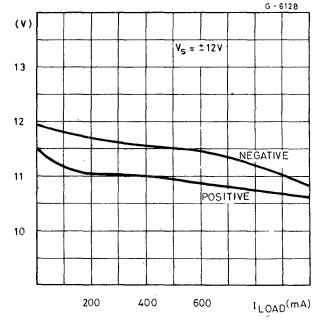


Fig. 6 - Supply voltage rejection vs. frequency

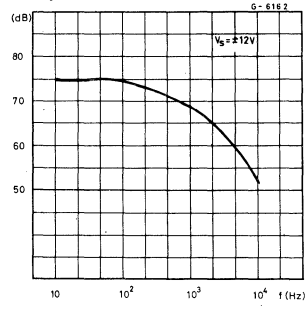
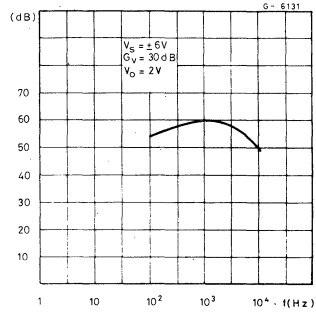


Fig. 7 - Channel separation vs. frequency

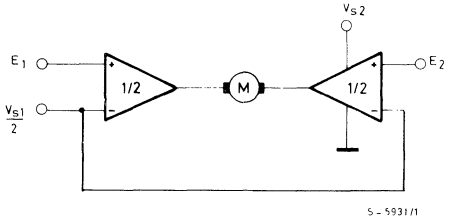


APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

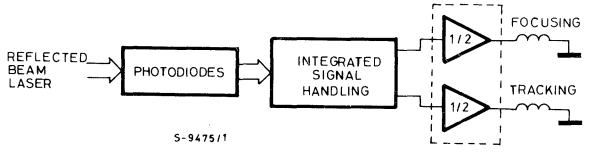


Fig. 10 - Capstan motor control in video recorders

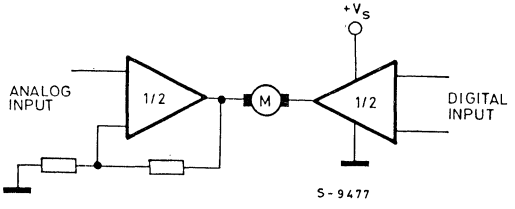
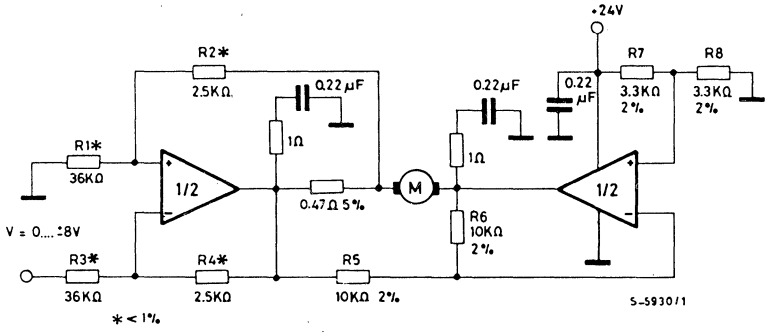


Fig. 11 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2 (V_I - \frac{V_s}{2}) + |R_o|. I_M$ where $|R_o| = \frac{2R \circ R1}{R_X}$ and I_M is the motor current.

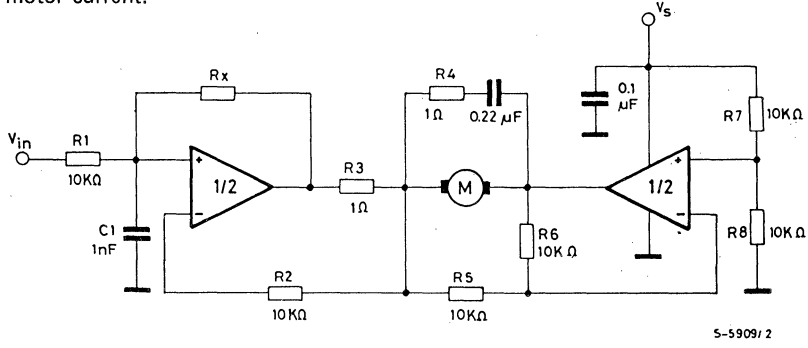
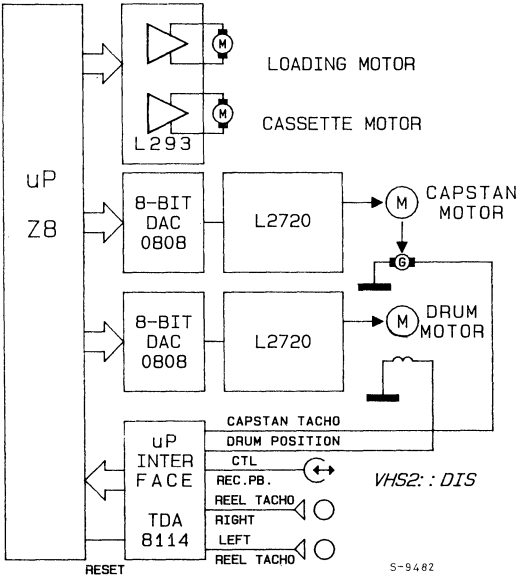


Fig. 13 - VHS-VCR Motor control circuit



LOW DROP DUAL POWER OPERATIONAL AMPLIFIER

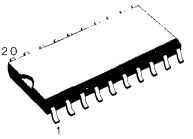
ADVANCE DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE

The L2726 is a monolithic integrated circuit in SO-20 package intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

It is particularly indicated for driving inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



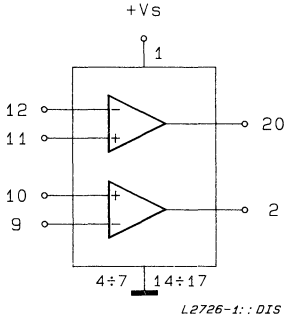
SO-20
(12+4+4)

ORDER NUMBER: L2726

ABSOLUTE MAXIMUM RATINGS

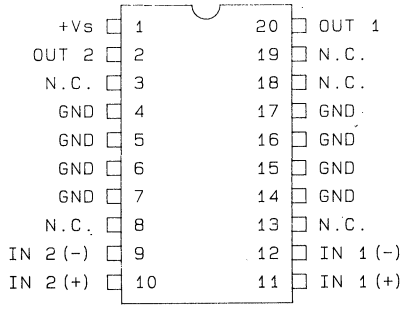
V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 85°C$	1	W
	$T_{case} = 75°C$	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM



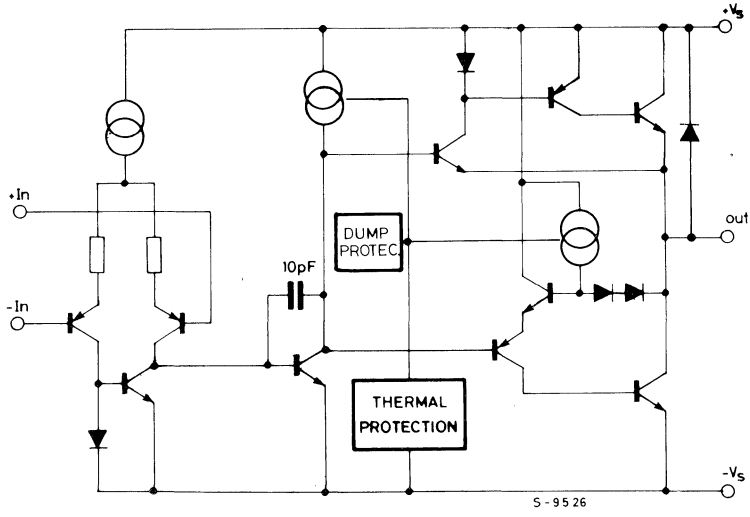
L2726-1: : DIS

CONNECTION DIAGRAM
(Top view)



L2726-2::DIS

SCHEMATIC DIAGRAM (one section)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	15.0	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (*)	max	65	°C/W

(*) With 4 sq. cm copper area heatsink

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input bias current				0.2	1	µA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/µs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		µV
I_N	Input noise current				200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ±12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		V_s = ±2.5V to ±12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

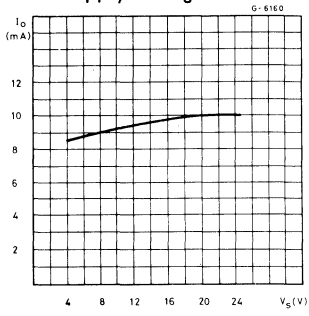


Fig. 2 - Open loop gain vs. frequency

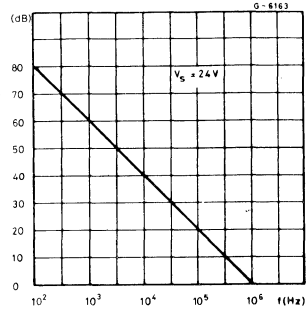


Fig. 3 - Common mode rejection vs. frequency

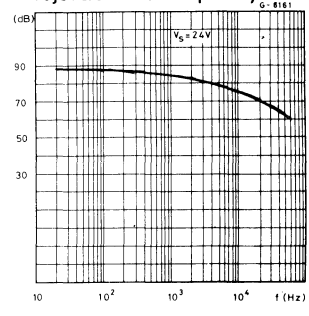


Fig. 4 - Output swing vs. load current (V_S = ± 5V)

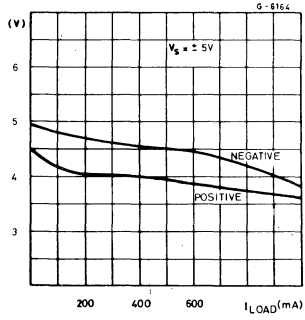


Fig. 5 - Output swing vs. load current (V_S = ± 12V)

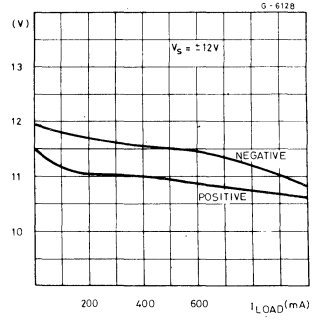


Fig. 6 - Supply voltage rejection vs. frequency

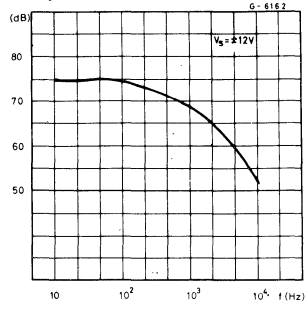
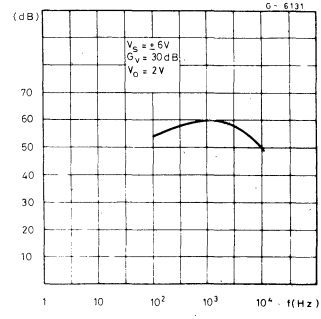


Fig. 7 - Channel separation vs. frequency



PRINTER SOLENOID DRIVER

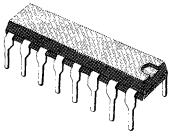
The L3654S is a printer solenoid driver containing ten open-collector driver outputs and a ten-bit serial-in, parallel-out register.

Data is clocked into the shift register serially and transferred to the open-collector outputs by an enable input. Serial input data is loaded by the rising edge of the clock. A serial output from the tenth bit is provided which changes at the falling edge of the clock. This output is not controlled by the enable input and remains active at all time.

The L3654S is pin to pin compatible with the standard L3654, but can work with V_s down to 4.75V.

Each output is rated at 250mA (sink) and is clamped to ground internally at 50V to dissipate stored energy in inductive loads.

The L3654S is supplied in a 16 lead dual in-line plastic package, and its main fields of application comprise thermal printers, cash registers and printing pocket calculators.



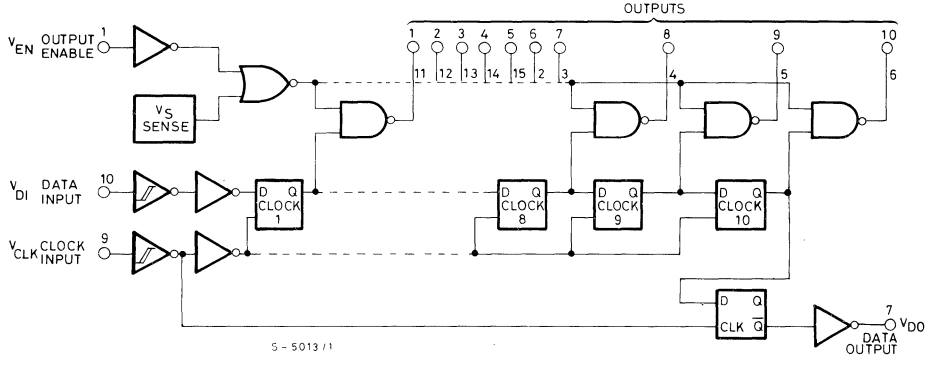
DIP-16 Plastic
(0.25)

ORDERING NUMBER: L3654S

ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	9.5	V
V_i	Input voltage	9.5	V
V_E	External supply voltage	45	V
I_o	Output current (single output)	0.4	A
I_g	Ground current	4.0	A
P_{tot}	Total power dissipation (T_{amb} = 70°C)	1	W
T_{stg}, T_j	Storage and junction temperature	-65 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM
(top view)

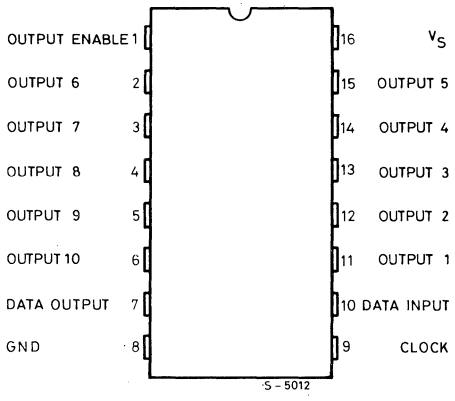
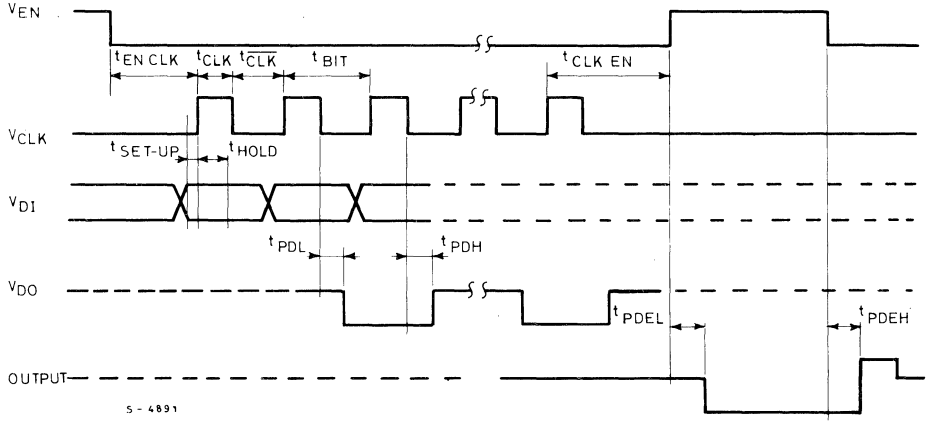


Fig. 1 - Timing diagram



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS ($V_s = 5V$, $V_E = 30V$, $T_{amb} = 0°$ to $70°C$, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_s	Supply voltage			4.75		9.5	V
I_S	Supply current	$T_{amb} = 25°C$	$V_{EN} = 0V$; $V_{DO} = 0V$		27	40	mA
		$V_s = 9.5V$	$V_{EN} = 2.6V$ $I_o = 250$ mA (each bit)		55	70	mA
V_E	External operating supply voltage					40	V
I_{leak}	Output leakage current (each output)	$V_E = 40V$	$V_{EN} = 0V$			1	mA
V_z	Internal clamp voltage	$I_z = 0.3A$ *	$V_{EN} = 0V$	45	50	65	V
$V_{CE\ sat}$	Output saturation voltage	$I_o = 250$ mA	$V_{EN} = 2.6V$			1.6	V
V_{DI} V_{CLK} V_{EN}	Input logic levels (pins 1, 9, 10)	Low State (L)				0.8	V
		High state (H)		2.6			
I_{DI}	Data input current	$V_{DI} = 2.6V$	$T_{amb} = 70°C$	0.3	0.57		mA
			$T_{amb} = 0°C$		0.57	0.75	
		$V_{DI} = 1V$	$T_{amb} = 70°C$		220		μA
I_{CLK}	Clock input current	$V_{CLK} = 2.6V$	$T_{amb} = 70°C$	0.2	0.33		mA
			$T_{amb} = 0°C$		0.33	0.5	
		$V_{CLK} = 1V$	$T_{amb} = 70°C$		125		μA
I_{EN}	Enable input current	$V_{EN} = 2.6V$	$T_{amb} = 70°C$	0.2	0.33		mA
			$T_{amb} = 0°C$		0.33	0.5	
		$V_{EN} = 1V$	$T_{amb} = 70°C$		125		μA
R_{IN}	Input pull-down resistance Clock input	$T_{amb} = 25°C$	$V_{CLK} < V_s$		8		KΩ
	Enable input	$T_{amb} = 25°C$	$V_{EN} < V_s$		8		
	Data input	$T_{amb} = 25°C$	$V_{DI} < V_s$		4.5		
V_{DO}	Output logic levels (pin 7)	Low state (L) $V_{DI} = 0V$	I_{DO}(pin 7) = 0		0.01	0.5	V
		High state (H) $V_{DI} = 2.6V$ I_{DO} (pin 7) = -0.75 mA		2.6	3.4		V
R_{DO}	Output pull-down resistance (pin 7)	$V_{DI} = 0V$	$V_{DO} = 1V$		14		KΩ

* Pulsed: pulse duration = 300μs, duty cycle = 2%

ELECTRICAL CHARACTERISTICS (see fig. 1 and the section "definition of terms")

Parameter		Test conditions	Min.	Typ.	Max.	Unit
Clock, data and enable input	t_{CLK}		4			µs
	$\overline{t_{CLK}}$		5.5			
	t_{SET-UP}		1			
	t_{HOLD}		3			
Glock to enable delay	$t_{CLK\ EN}$		2 t_{BIT}			
Enable to clock delay	$t_{EN\ CLK}$		t_{BIT}			
Data output delay	t_{PDH}, t_{PDL}	R_L= 5KΩ, $C_L \leqslant$ 10 pF		0.8	2.5	µs
Output delay	t_{PDEL}			3		µs
	t_{PDEH}			3.5		
Output rise time		R_L= 100 Ω, $C_L <$ 100 pF		1.2		µs
Output fall time		R_L= 100 Ω, $C_L <$ 100 pF		1.2		µs
V_{DO} rise time				0.4		µs
V_{DO} fall time				0.4		µs

DEFINITION OF TERMS

V_{ss} : External power supply voltage. The return for open-collector relay driver outputs.

V_{DI}, V_{CLK}, V_{EN} : The voltages at the data, clock and enable inputs respectively.

V_{DO} : The voltage at data output.

t_{BIT} : Period of the incoming clock.

t_{CLK} : The portion of t_{BIT} when $V_{CLK} \geqslant 2.6V$.

$\overline{t_{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leqslant 0.8V$.

t_{HOLD} : The time following the start of t_{CLK} required to transfer data within the shift register.

t_{SET-UP} : The time prior to the end of $\overline{t_{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.

SGS-THOMSON MICROELECTRONICS

L4901A

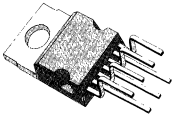
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 400mA, I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly tor supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



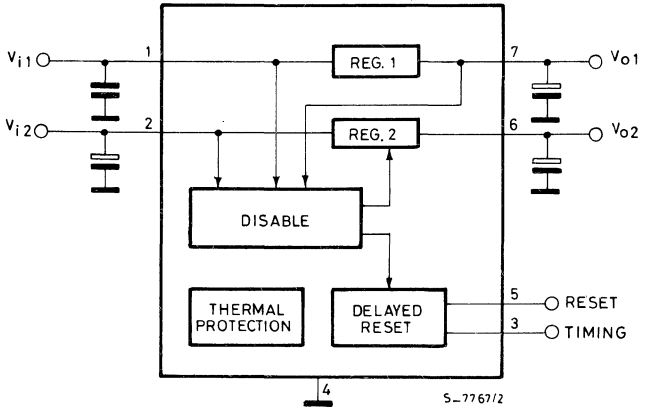
Heptawatt

ORDERING NUMBER: L4901A

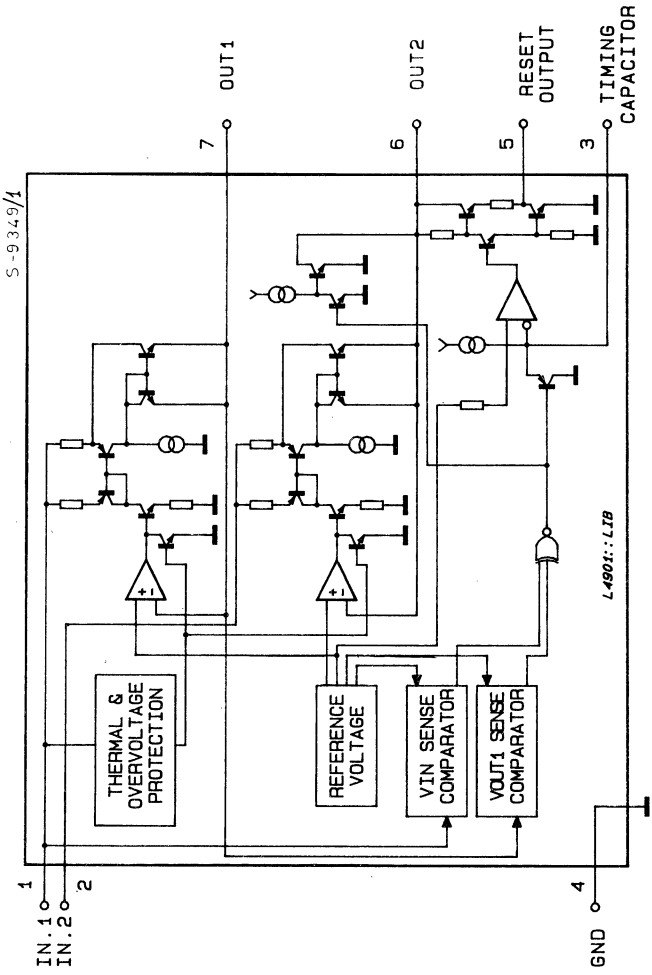
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

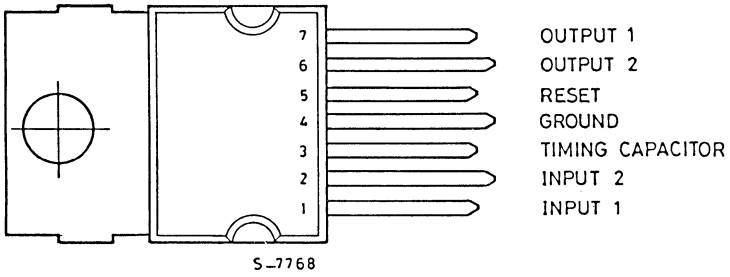
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



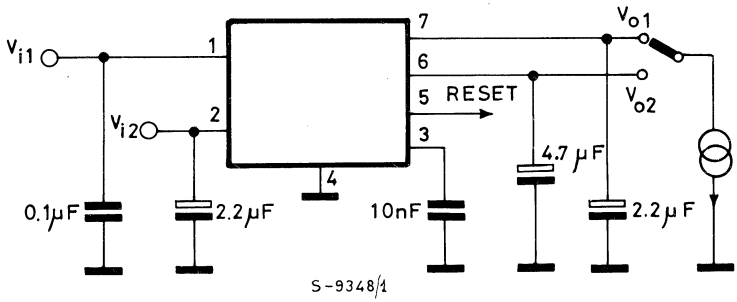
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 400mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 400mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14{,}4V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4,95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	400			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq 3V$			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	400			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 400mA		50	100	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ⩽ T_{amb} ⩽ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ⩽ T_{amb} ⩽ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

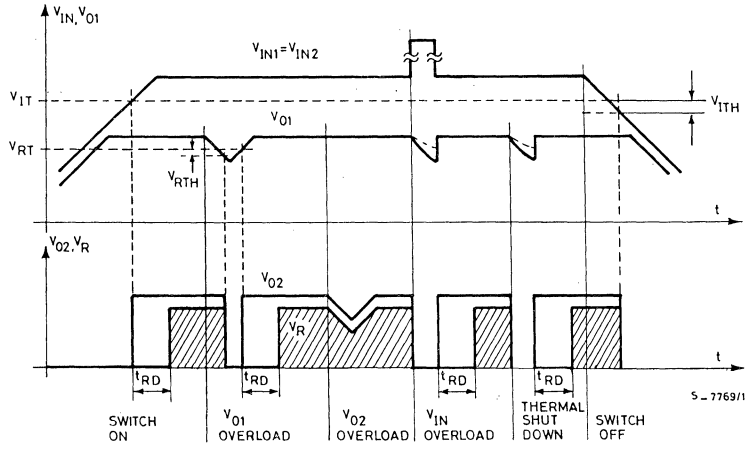
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901A is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_1 occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

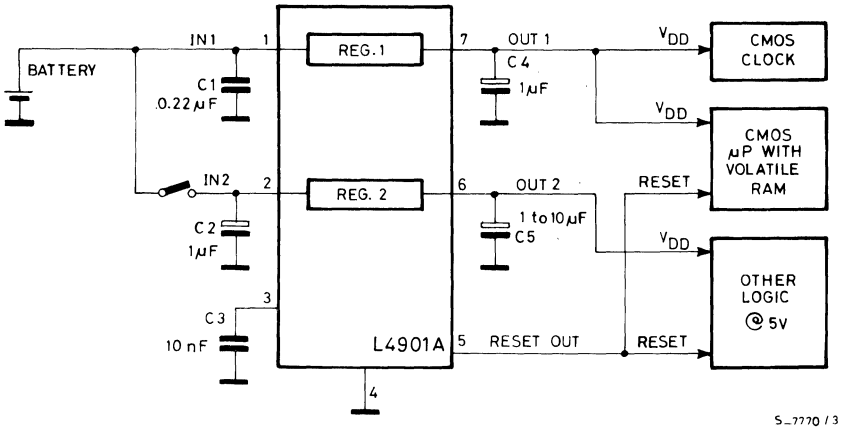
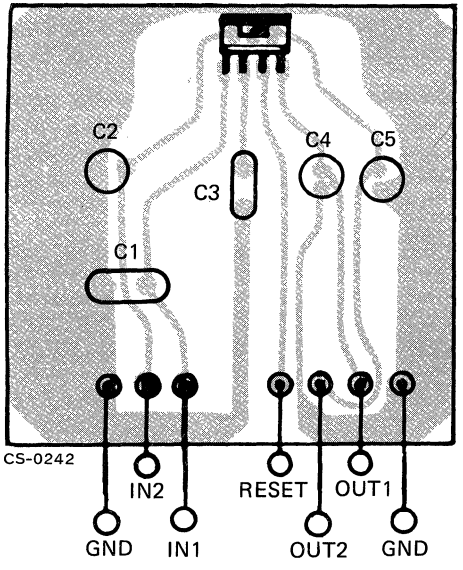


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

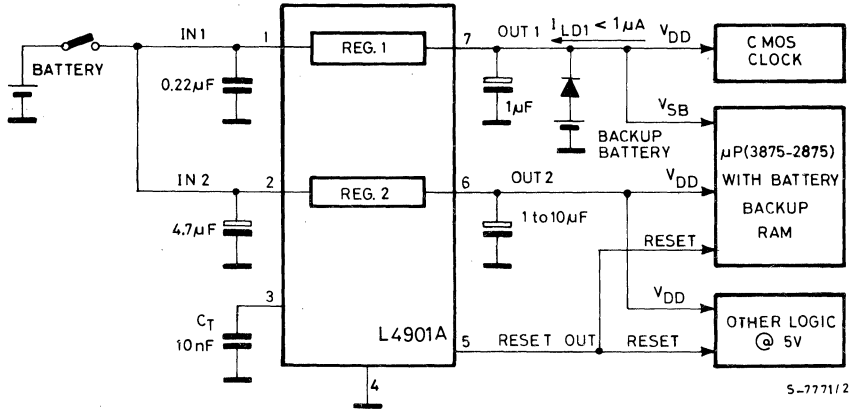
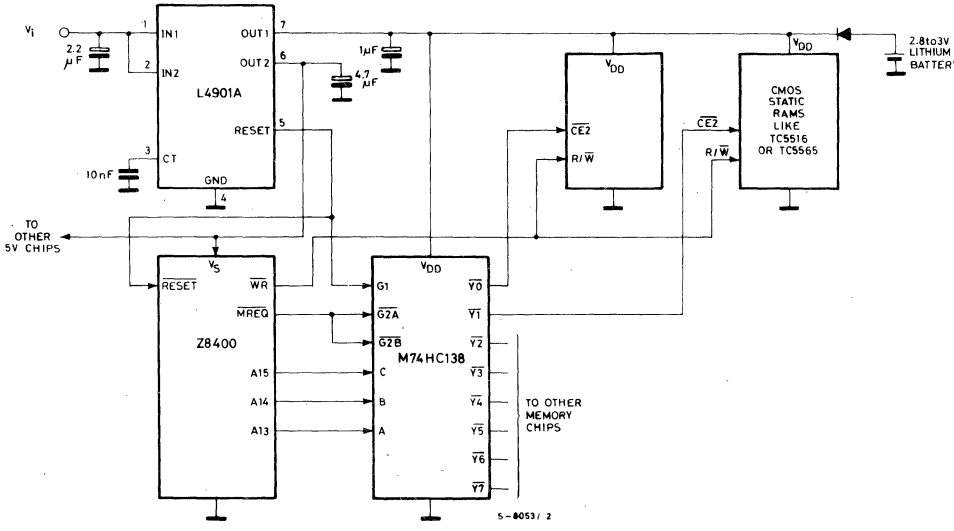


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

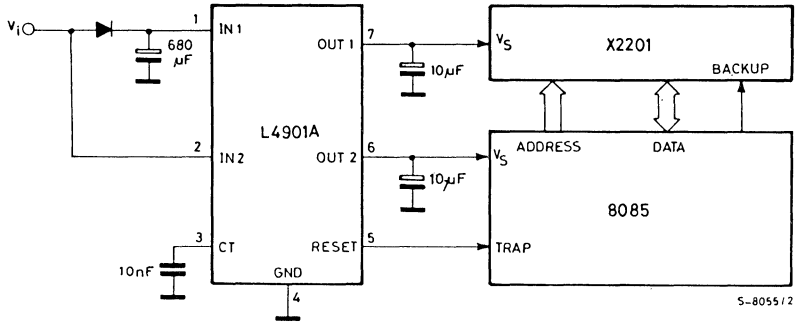


Fig. 7 - Quiescent current (Reg. 1) vs. output current

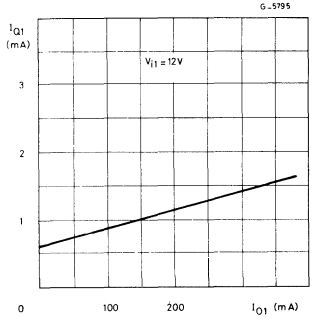


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

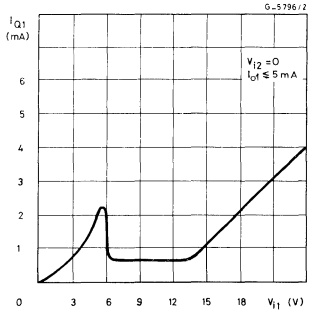


Fig. 9 - Total quiescent current vs. input voltage

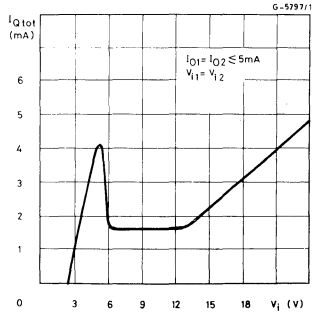


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

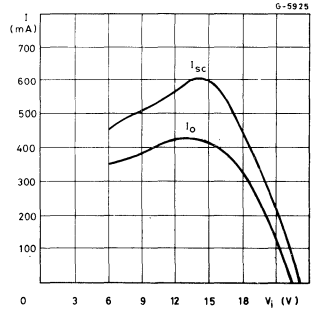


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

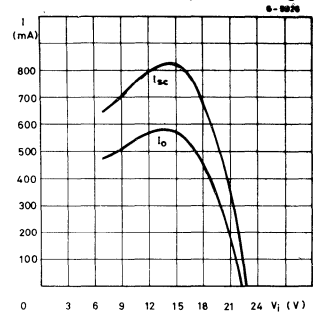
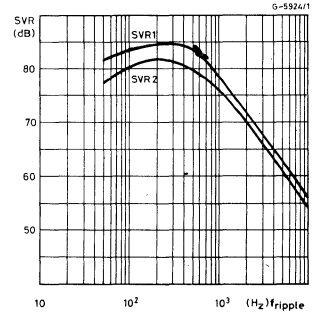


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence

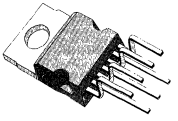


DUAL 5V REGULATOR WITH RESET AND DISABLE

PRELIMINARY DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



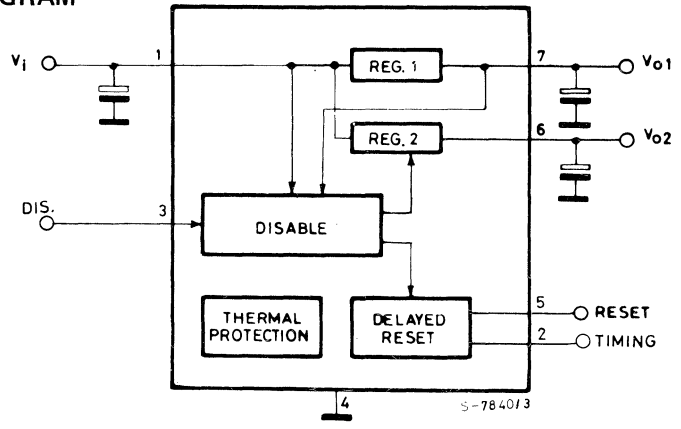
Heptawatt

ORDERING NUMBER: L4902A

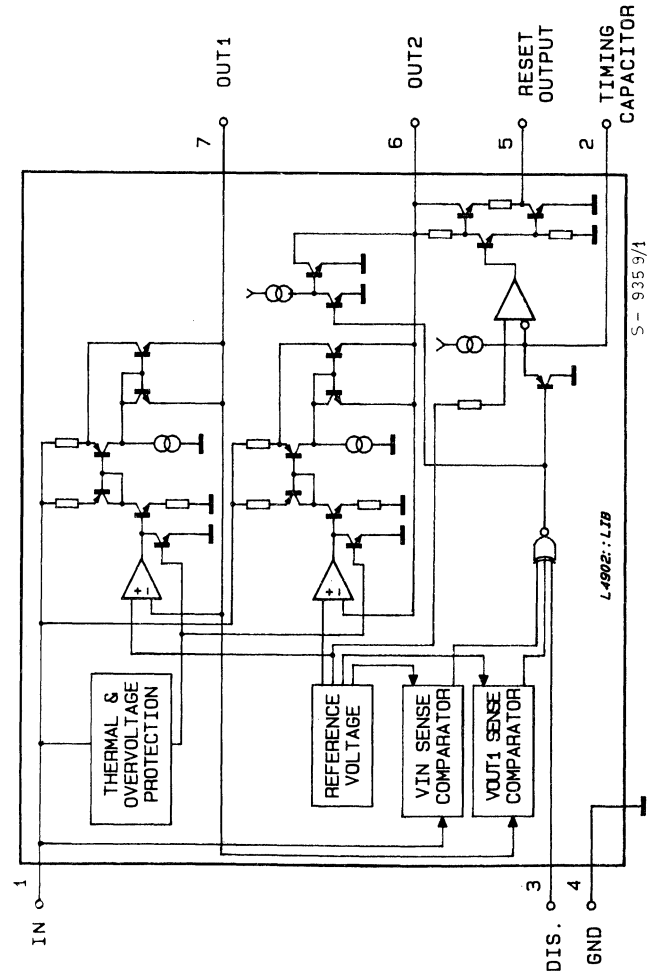
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

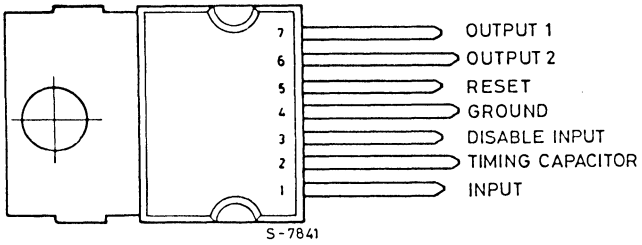
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



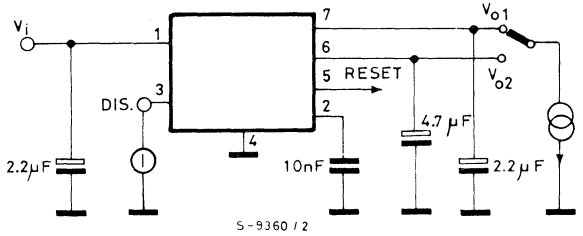
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) = C_t (nF).
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max.	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max.	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{iTH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	80	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -1mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 -30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

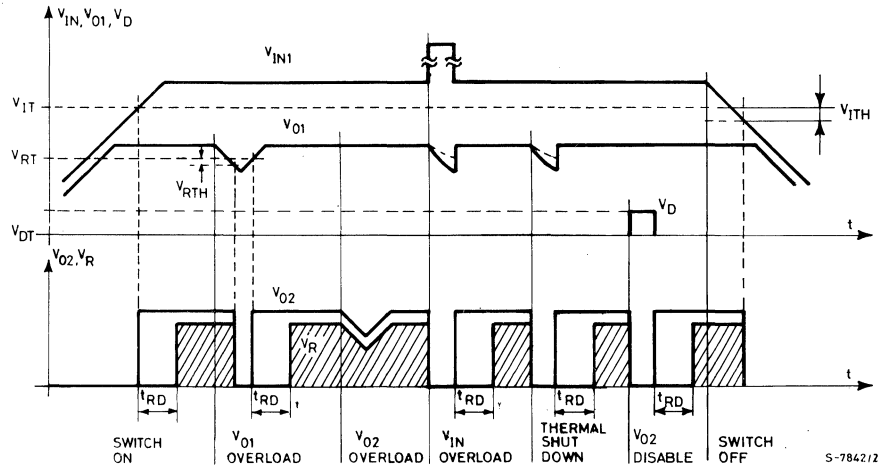
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrate how the L4902A's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902A is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

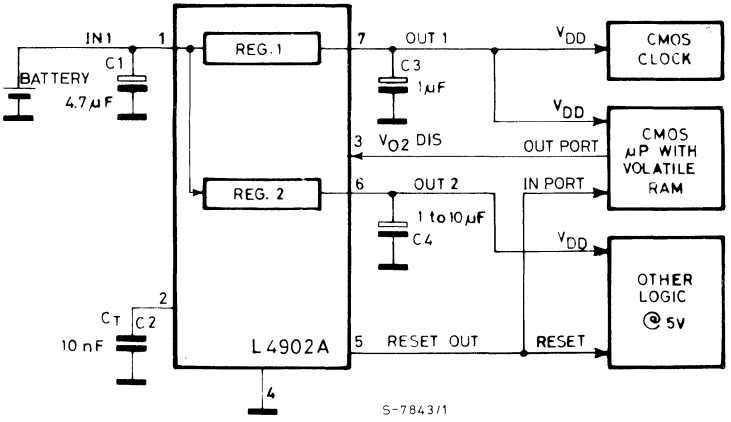
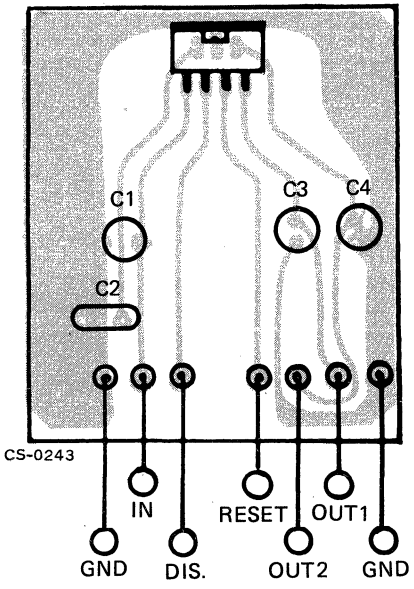


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

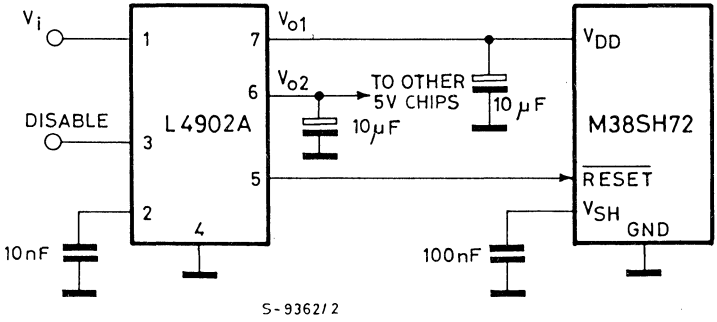
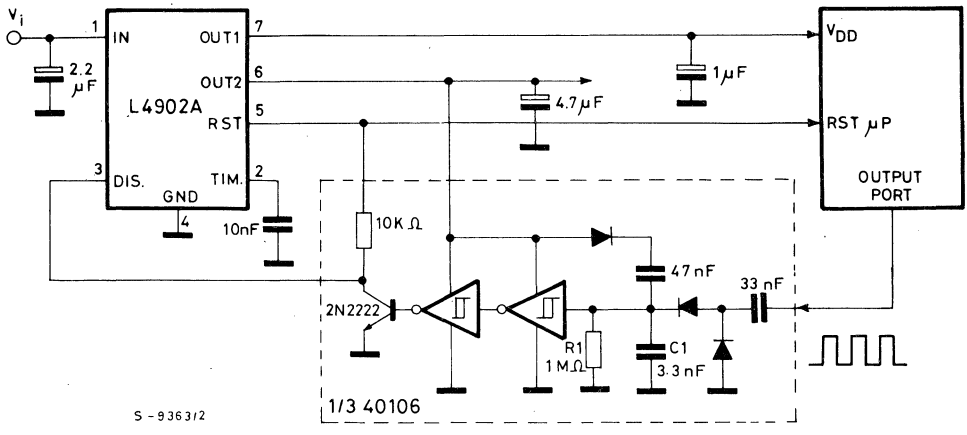


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

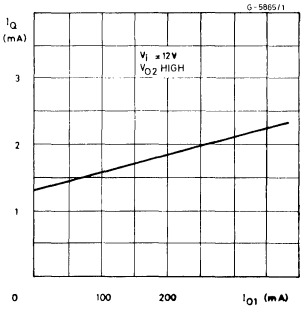


Fig. 7 - Quiescent current vs. input voltage

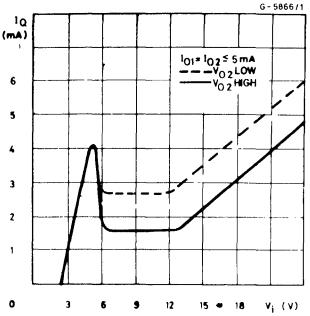
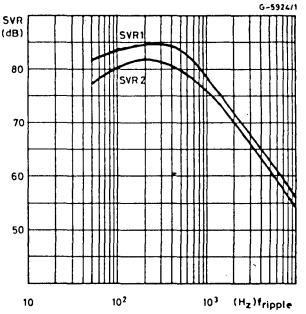


Fig. 8 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



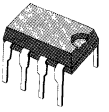
DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA, I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.



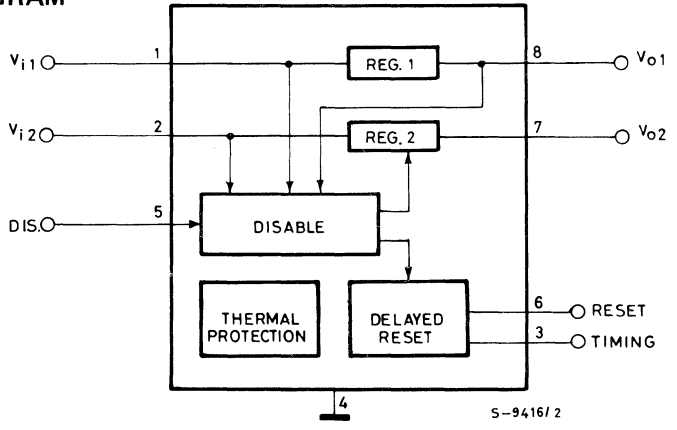
Minidip Plastic

ORDERING NUMBER: L4903

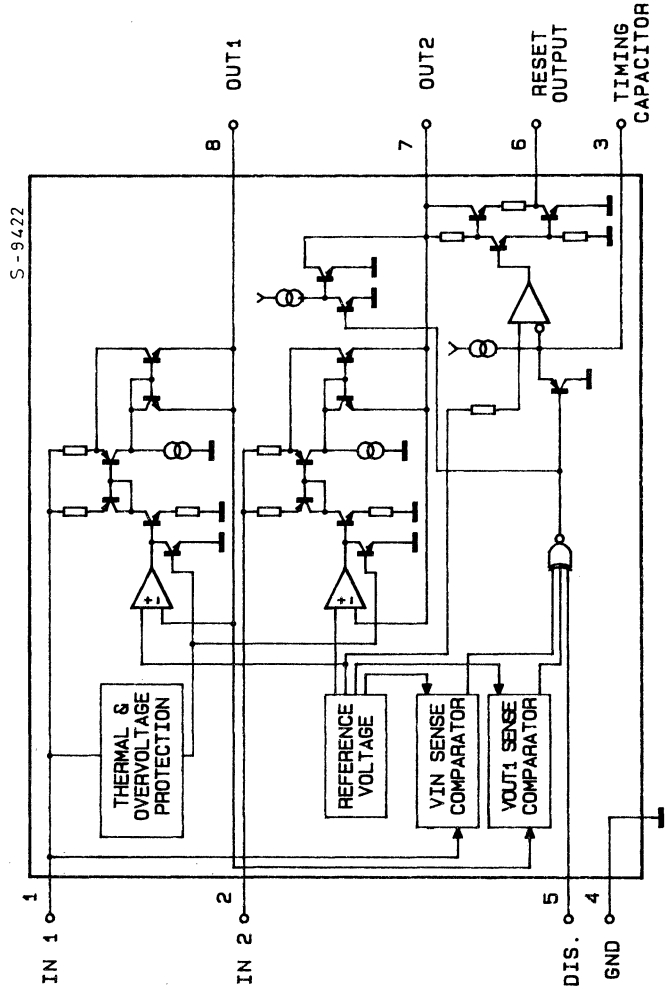
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40 ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

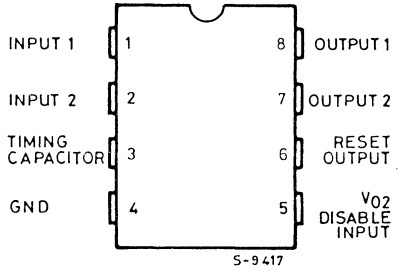
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



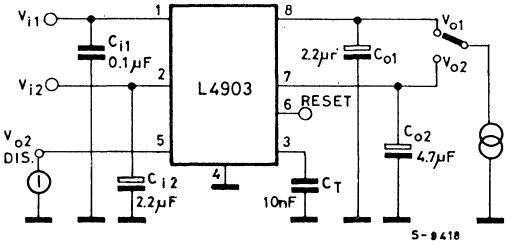
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disables output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t (\frac{5V}{10\mu A})$; t_{RD} (ms) = C_t (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if V_O 1 $> V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

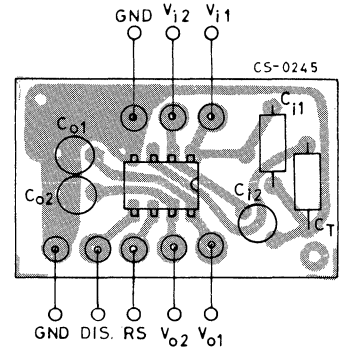
THERMAL DATA

$R_{th\ j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis			30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level ($> V_{DT}$) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

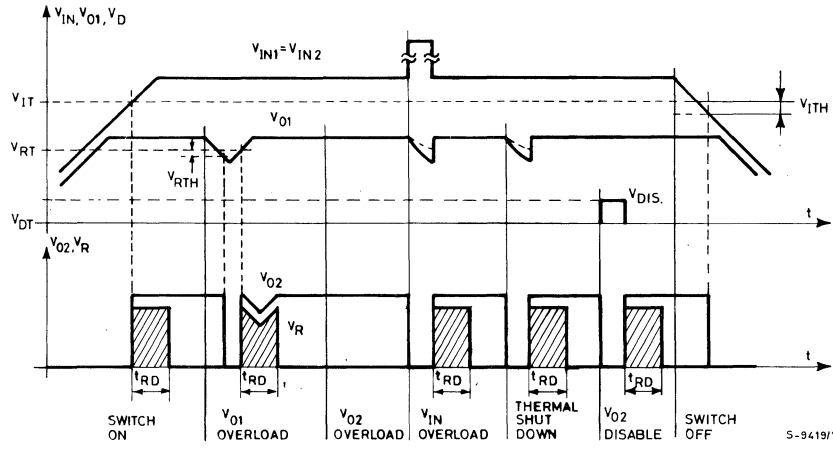
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



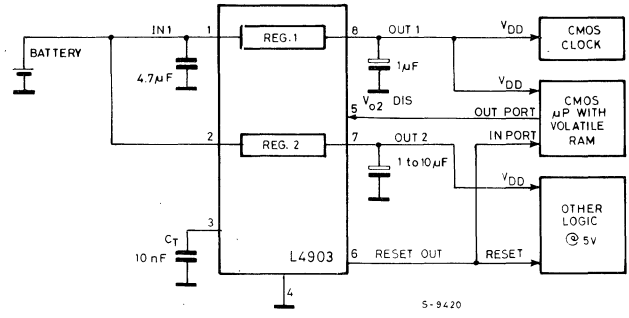
APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2



APPLICATION SUGGESTIONS (continued)

Fig. 3 - Quiescent current (Reg. 1) vs. output current

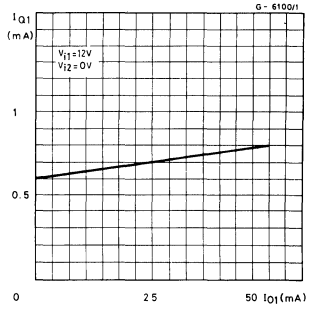


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

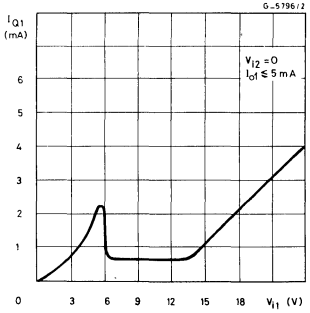


Fig. 5 - Total quiescent current vs. input voltage

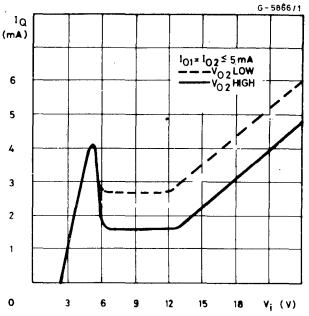
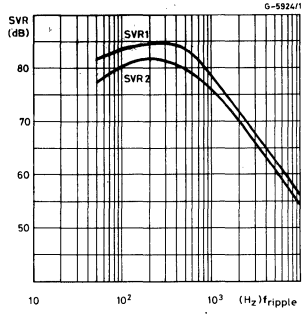


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



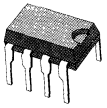
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA, I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



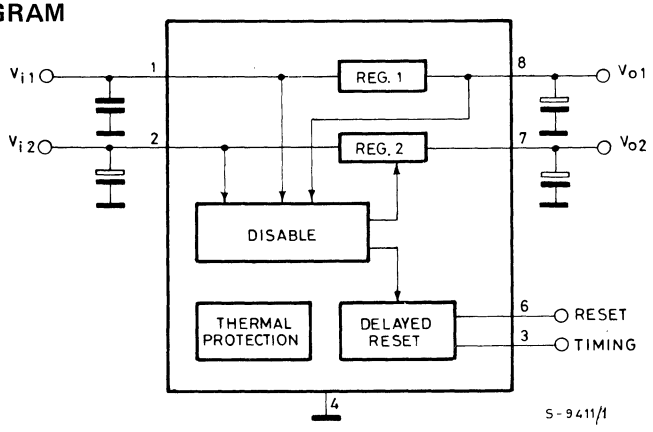
Minidip Plastic

ORDERING NUMBER: L4904A

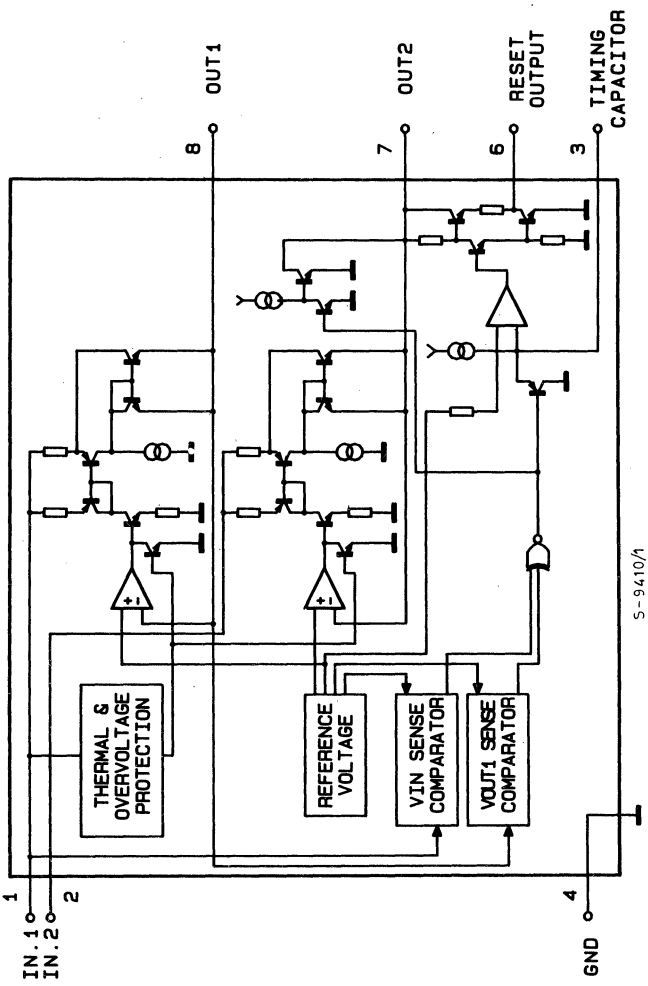
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

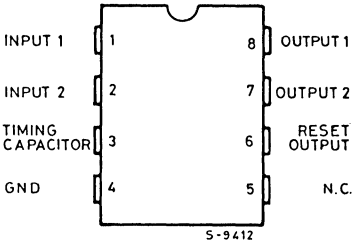
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



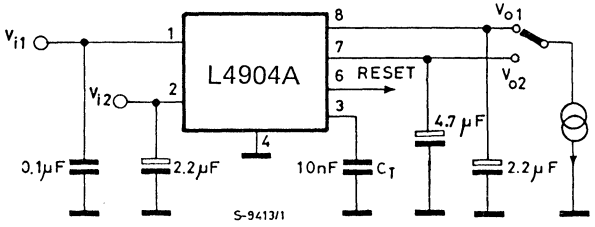
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \ (\frac{5V}{10\mu A})$; t_{RD} (ms) $= C_t$ (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

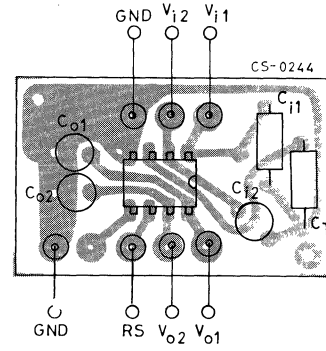
THERMAL DATA

$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01} -0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	100			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01} +1.2	6.4	V_{01} +1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3		11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904A makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01} regulator also features low consumption (0.6mA

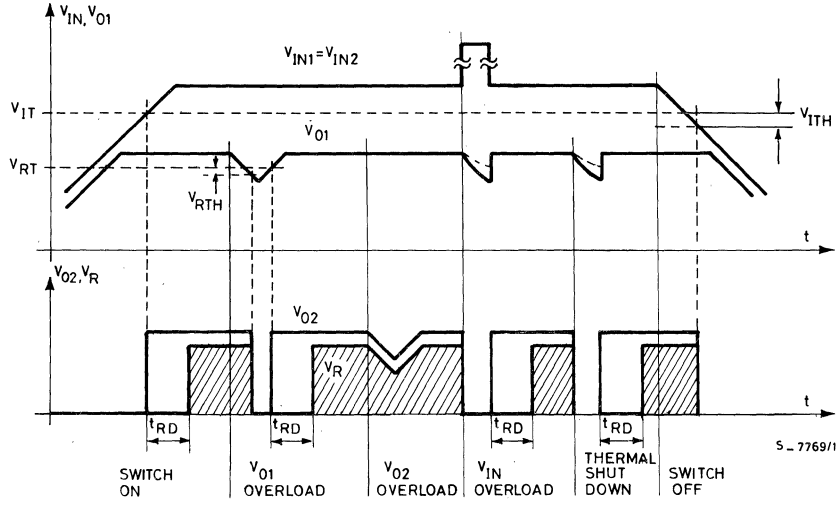
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

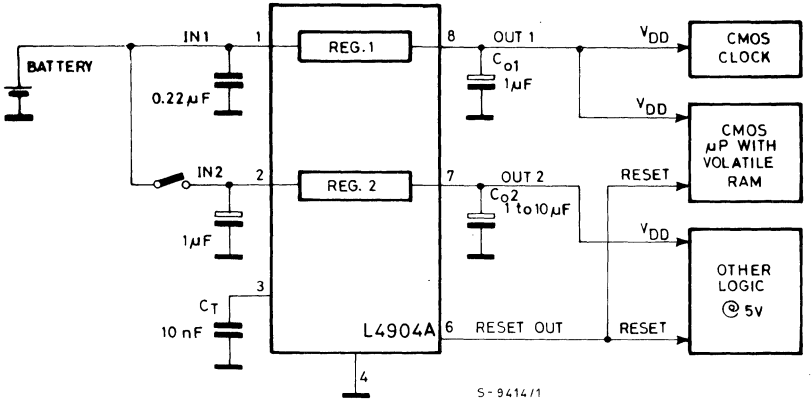
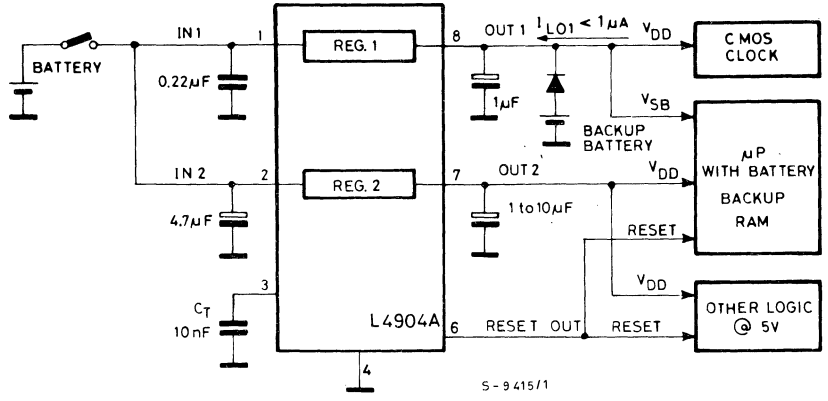


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

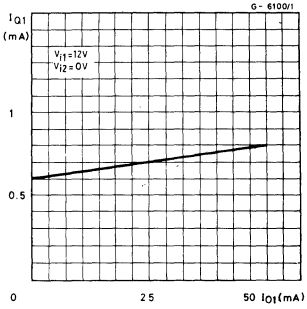


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

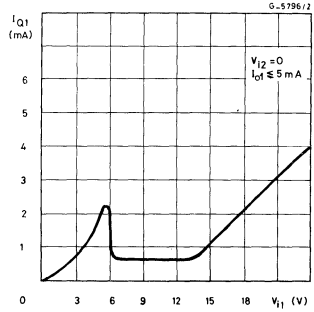


Fig. 6 - Total quiescent current vs. input voltage

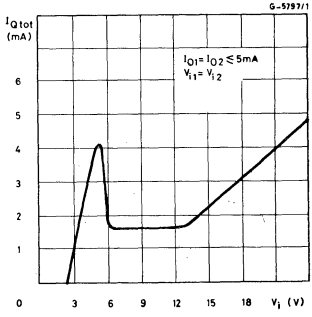
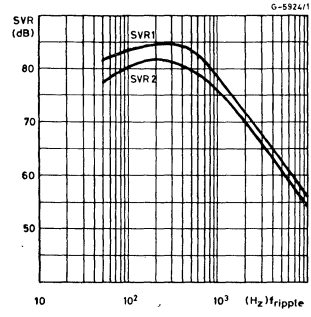


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



SGS-THOMSON MICROELECTRONICS

L4905

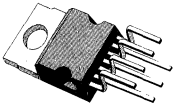
DUAL 5V REGULATOR WITH RESET

ADVANCE DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: $I_{01} = 200mA$ $I_{02} = 300mA$
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 1%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCIENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4905 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



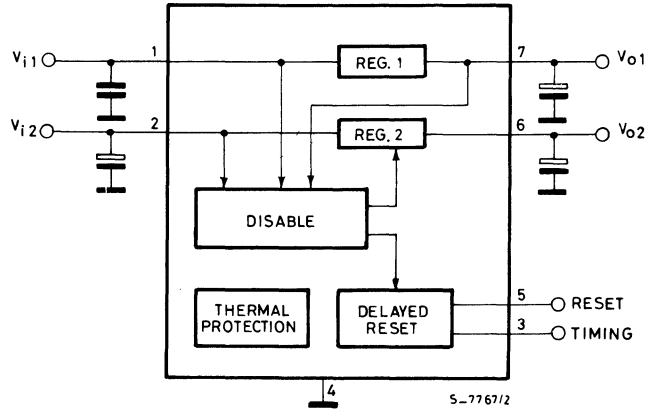
Heptawatt

ORDERING NUMBER: L4905

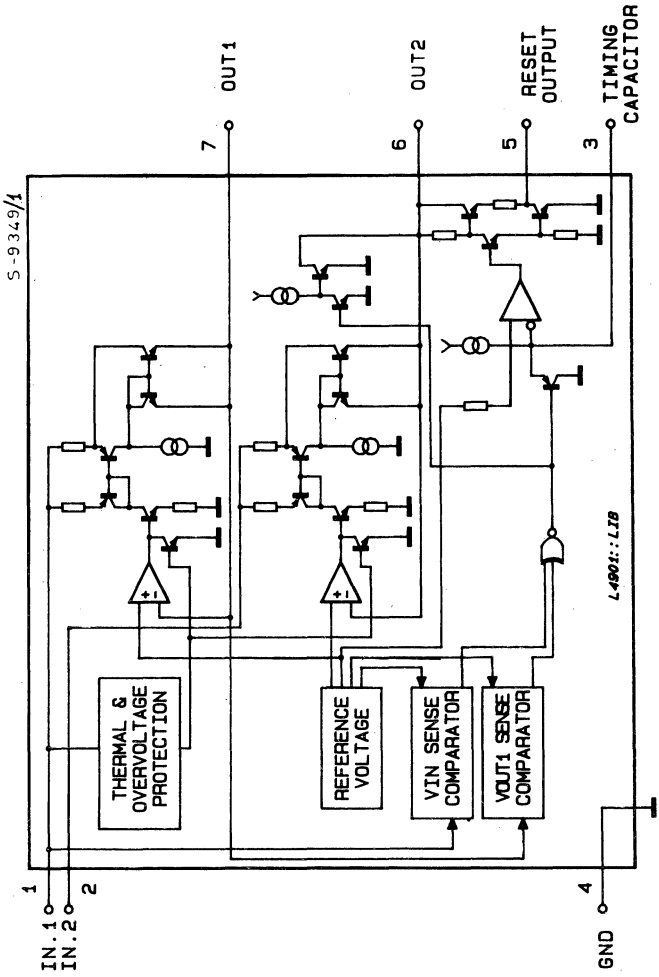
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

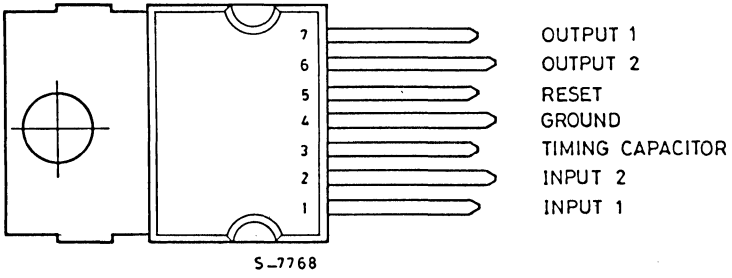
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



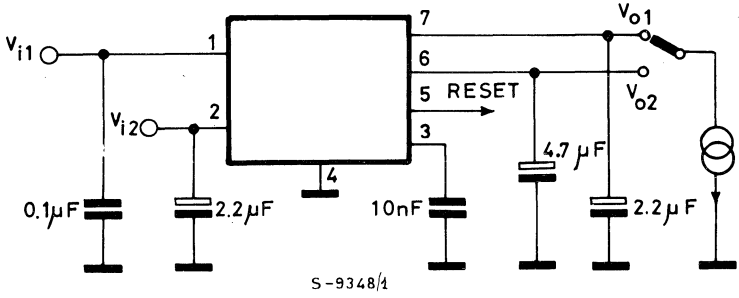
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 200mA regulator input.
2	INPUT 2	300mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 200mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2} = 14{,}4V$, $T_{amb} = 25°$ unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	5.0	5.05	5.1	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	200			mA
I_{L01}	Leakage output 1 current	$V_{IN} = 0$ $V_{01} \leq 3V$			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 200mA		0.7 0.8 1.05	0.8 1 1.3	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	$7V < V_{IN} < 24V$ I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 200mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	100	mV
I_Q	Quiescent current	$0 < V_{IN} < 13V$ $7V < V_{IN} < 13V$ $I_{02} = I_{01} \leq 5mA$		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	$6.3V < V_{IN1} < 13V$ $V_{IN2} = 0$ $I_{01} \leq 5mA$ $I_{02} = 0$		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V, I_o = 100mA	54 50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4905 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;
- permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

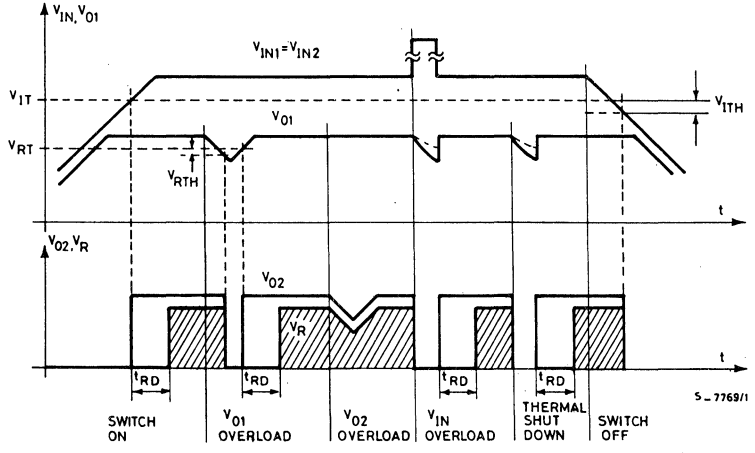
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4905 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTION (continued)

Fig. 2

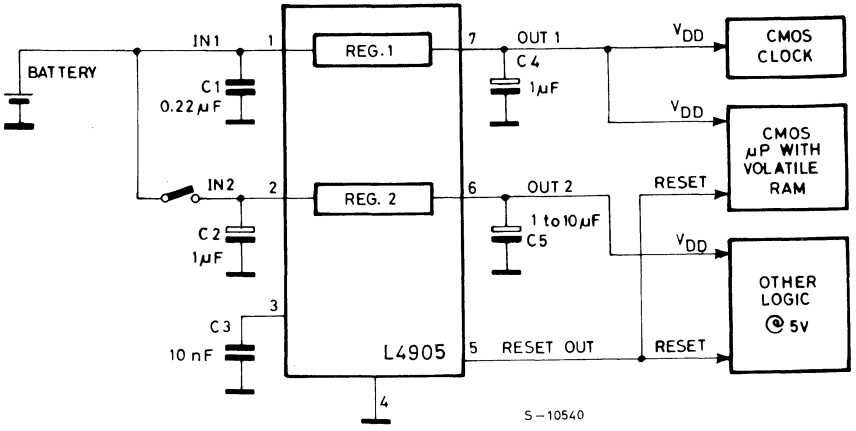
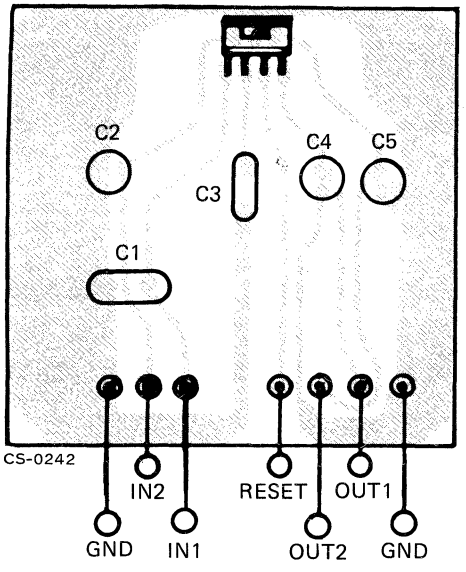


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

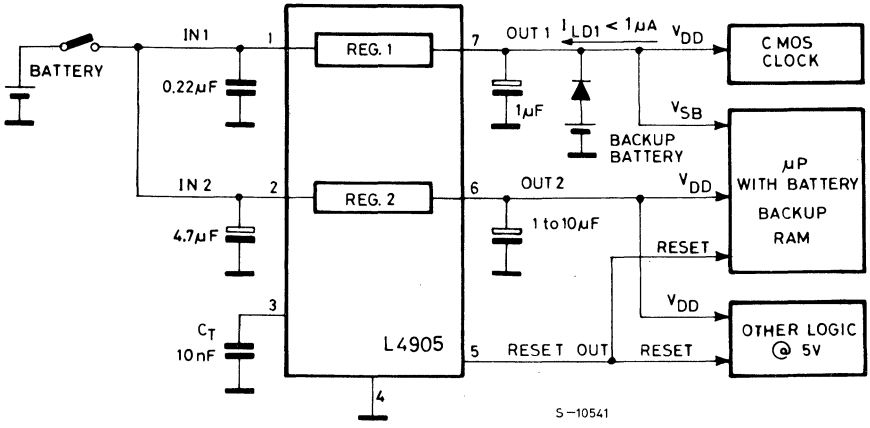


Fig. 5 - Quiescent current (Reg. 1) vs. output current

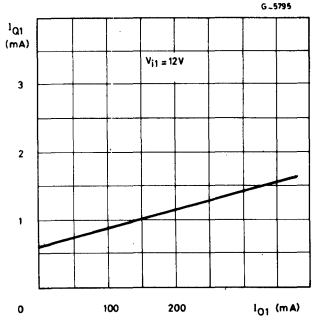


Fig. 6 - Quiescent current (Reg. 1) vs. input voltage

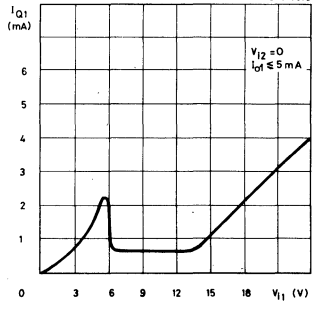
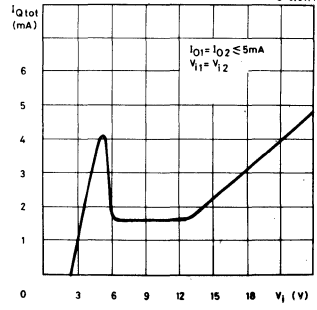


Fig. 7 - Total quiescent current vs. input voltage

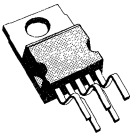


VERY LOW DROP ADJUSTABLE REGULATORS

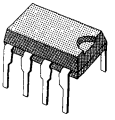
PRELIMINARY DATA

- VERY LOW DROP VOLTAGE
- ADJUSTABLE OUTPUT VOLTAGE FROM 1.25 V TO 20 V
- 400 mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION
- + 60/ – 60 V TRANSIENT PEAK VOLTAGE
- SHORT CIRCUIT PROTECTION WITH FOLDBACK CHARACTERISTICS
- THERMAL SHUT-DOWN

These regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.
In battery backup and standby applications the low consumption of these devices extends battery life.



Pentawatt



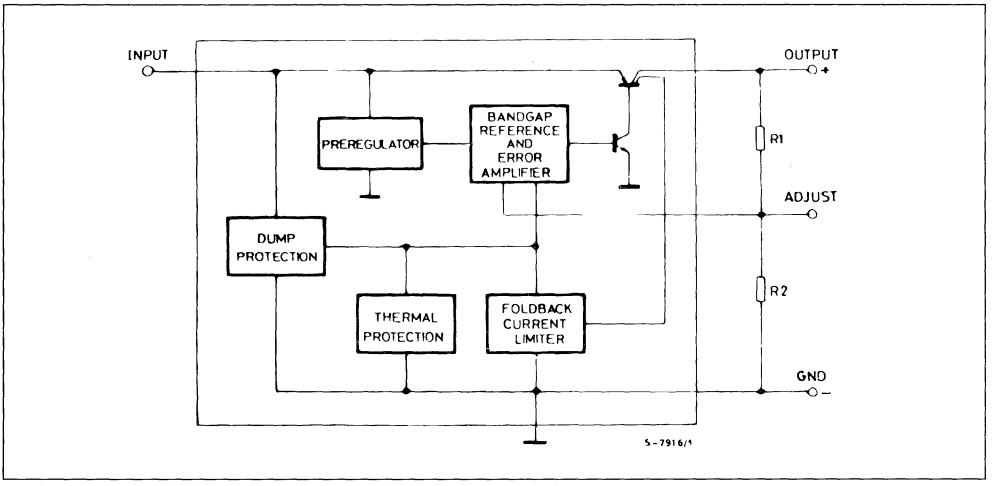
Minidip (4 + 4)

ORDER CODES : L4920
L4921

DESCRIPTION

The L4920 and L4921 are adjustable voltage regulators with a very low voltage drop (0.4 V typ. at 0.4 A T_j = 25 °C), low quiescent current and comprehensive on-chip protection.
These devices are protected against load dump transients of ± 60 V, input overvoltage, polarity reversal and over heating.
A foldback current limiter protects against load short circuits.
The output voltage is adjustable through an external divider from 1.25 V to 20 V. The minimum operating input voltage is 5.2 V (T_J = 25 °C).

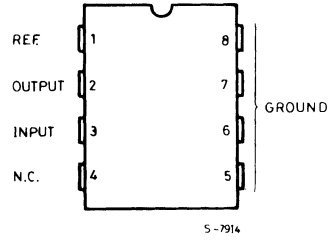
BLOCK DIAGRAM

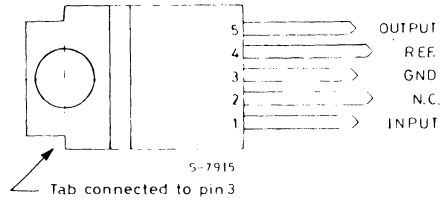


ABSOLUTE MAXIMUM RATINGS

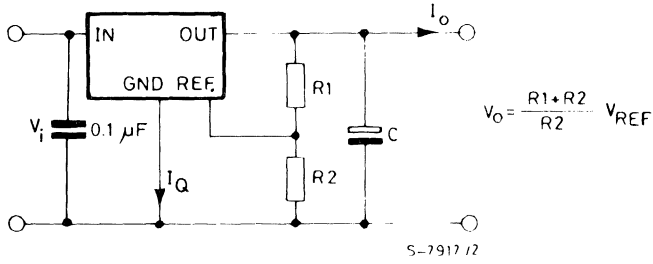
Symbol	Parameter	Value	Unit
V_i	DC Input Operating Voltage	35	V
V_t	Positive Transient Peak Voltage (t = 300 ms 1 % duty cycle)	+ 60	V
V_t	Negative Transient Peak Voltage (t = 100 ms 1 % duty cycle)	− 60	V
V_i	Reverse Input Voltage	− 18	V
T_j, T_{stg}	Junction and Storage Temperature Range	− 55 to 150	°C

PIN CONNECTIONS (top view)





TEST AND APPLICATION CIRCUIT



c = 100 µF is required for stability (ESR ≤ 3 Ω over T range)
R2 = 6.2 KΩ.

THERMAL DATA

			Minidip (4 + 4)	Pentawatt
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	60 °C/W
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	15 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W

ELECTRICAL CHARACTERISTICS (for V_I = 14.4 V; $-40 \leq T_j \leq 125$ °C (note 1), V_o = 5 V ; C_o = 100 µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	$V_o \geq 4.5$ V I_o = 400 mA	V_o + 0.9		26	V
		$V_{REF} \leq V_o < 4.5$ V I_o = 400 mA	5.4		26	V
V_{REF}	Reference Voltage	5.4 V < V_i < 26 V	1.17	1.25	1.33	V
ΔV_o	Line Regulation	V_o + 1.2 V < V_i < 26 V $V_o \geq 4.5$ V I_o = 5 mA		2	15	mV/V
ΔV_o	Load Regulation	5 mA < I_o < 400 mA (*) $V_o \geq 4.5$ V		5	25	mV/V
V_D	Dropout Voltage	 I_o = 150 mA I_o = 400 mA		 0.25 0.5	 0.5 0.9	 V V
I_D	Quiescent Current	I_o = 0 mA V_o + 1.2 V < V_i < 26 V		1.2	3	mA
		I_o = 400 mA (*) V_o + 1.2 V < V_i < 26 V		80	140	mA
I_o	Maximal Output Current			870		mA
I_{OSC}	Short Circuit Output Current (*)			230		mA

(*) Foldback protection.

Note : 1. Design limits are guaranteed (but not 100 % production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

ELECTRICAL CHARACTERISTICS (for V_I = 14.4 V, T_j = 25 °C, V_o = 5 V, C_o = 100 µF, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Operating Input Voltage	$V_o \geq 4.5$ V I_o = 400 mA	V_o + 0.7		26	V
		$V_{REF} \leq V_o < 4.5$ V I_o = 400 mA	5.2		26	V
V_{REF}	Reference Voltage	5.2 V < V_i < 26 V 5 mA $\leq I_o \leq$ 400 mA (*)	1.20	1.25	1.30	V
ΔV_o	Line Regulation	V_o + 1 V < V_i < 26 V $V_o \geq 4.5$ V I_o = 5 mA		1	10	mV/V
ΔV_o	Load Regulation	5 mA < I_o < 400 mA (*) $V_o \geq 4.5$ V		3	15	mV/V
V_D	Dropout Voltage	I_o = 10 mA I_o = 150 mA I_o = 400 mA		0.05 0.2 0.4	 0.4 0.9	V V V
I_D	Quiescent Current	I_o = 0 mA V_o + 1 V < V_i < 26 V		0.8	2	mA
		I_o = 400 mA (*) V_o + 1 V < V_i < 26 V		65	90	mA
I_o	Maximal Output Current			800		mA
I_{OSC}	Short Circuit Output Current (*)			350	500	mA

(*) Foldback protection.

Figure 1 : Output Voltage vs. Temperature.

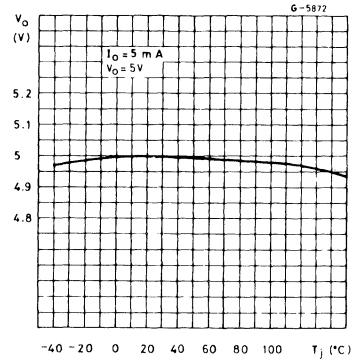


Figure 2 : Foldback Current Limiting.

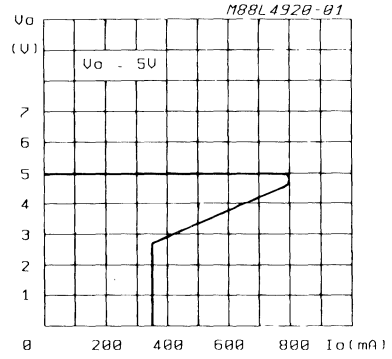
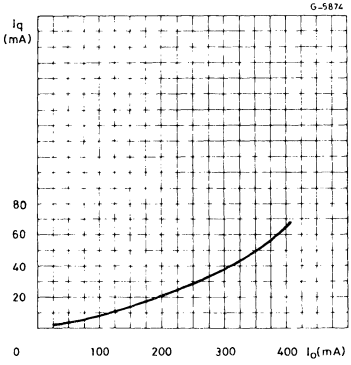


Figure 3 : Quiescent Current vs. Output Current (V_o = 5 V).



APPLICATION INFORMATION

1) The L4920 and L4921 have $V_{REF} \cong 1.25$ V. Then the output voltage can be set down to V_{REF} but V_i must be greater than 5.2 V (T_j = 25 °C).
2) As the regulator reference voltage source works in closed loop, the reference voltage may change in foldback condition.
3) For applications with high V_I, the total power dissipation of the device with respect to the thermal resistance of the package may be limiting the application. The total power dissipation is :

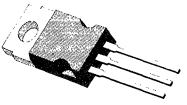
$$P_{tot} = V_i I_q + (V_i - V_o) I_o$$

A typical curve giving the quiescent current I_q as a function of the output current I_o is shown in fig. 3.

VERY LOW DROP 1.5A REGULATORS

PRELIMINARY DATA

- PRECISE 5V, 8.5V, 10V, 12V OUTPUTS
- LOW DROPOUT VOLTAGE (500mV TYP AT 1.5A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION

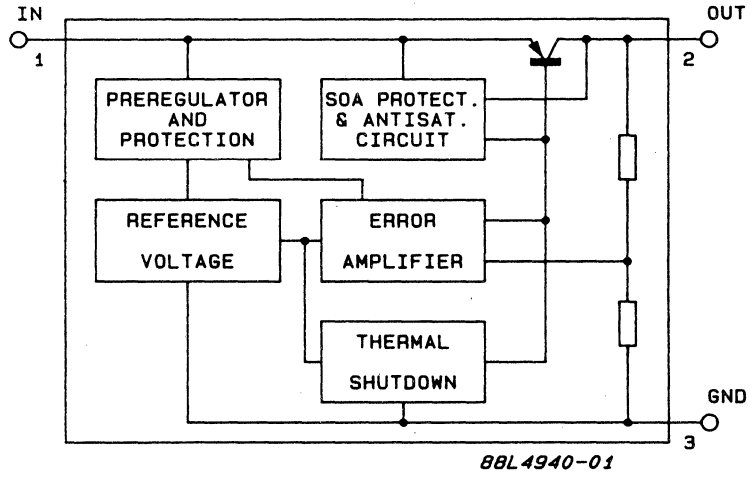


TO-220

INTRODUCTION

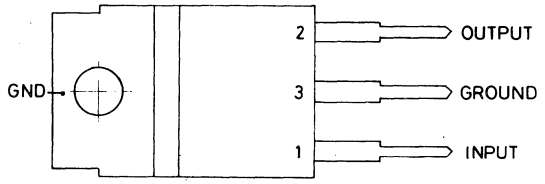
The L4940 series of three terminal positive regulators is available in TO-220 package and with several fixed output voltages, making it useful in a wide range of industrial and consumer applications. Thanks to its very low input/output voltage drop, these devices are particularly suitable for battery powered equipments, reducing consumption and prolonging battery life. Each type employs internal current limiting, antisaturation circuit, thermal shut-down and safe area protection.

BLOCK DIAGRAM



CONNECTION DIAGRAM AND ORDERING NUMBERS

(Top view)



S-2568/1

ORDERING NUMBERS	OUTPUT VOLTAGE
L4940V5	5V
L4940V85	8.5V
L4940V10	10V
L4940V12	12V

ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage			30	V
V_{iR}	Reverse input voltage	(V_O = 5V	R_O = 100Ω)	-15	V
		(V_O = 8.5V	R_O = 180Ω)		
		(V_O = 10V	R_O = 200Ω)		
		(V_O = 12V	R_O = 240Ω)		
I_O	Output current			Internally limited	
P_{tot}	Power dissipation			Internally limited	
T_j, T_{stg}	Junction and storage temperature			-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

TEST CIRCUITS

Fig. 1 - DC Parameters

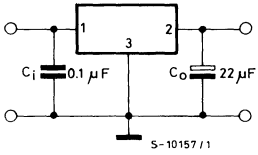


Fig. 2 - Load Regulation

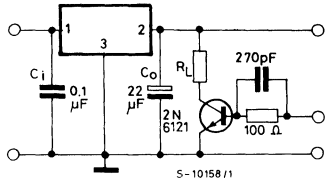
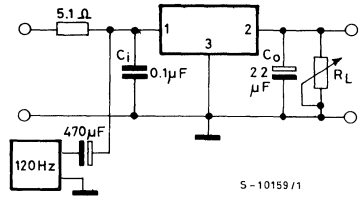


Fig. 3 - Ripple Rejection



ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25°C$, $C_i = 0.1\mu F$, $C_o = 22\mu F$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE				5			8.5		V
INPUT VOLTAGE (unless otherwise specified)				7			10.5		V
V_o	Output voltage	I_o = 0.5A	4.9	5	5.1	8.3	8.5	8.7	V
		I_o = 5 mA to 1.5A	4.8 (V_i= 6.5 to 16V)	5	5.2	8.15 (V_i= 10.2 to 16V)	8.5	8.85	V
V_i	Operating input voltage	I_o = 5 mA			17			17	V
ΔV_o	Line regulation	I_o = 5 mA		4 (V_i= 6V to 17V)	10		4 (V_i= 9.5 to 17V)	9	mV
ΔV_o	Load regulation	I_o = 5 mA to 1.5A		8	25		12	30	mV
		I_o = 0.5A to 1A		5	15		8	16	
I_Q	Quiescent current	I_o = 5 mA		5	8		4	8	mA
		I_o = 1.5 A		30 (V_i = 6.5V)	50		30 (V_i = 10.2V)	50	
ΔI_Q	Quiescent current change	I_o = 5 mA			3			2.5	mA
		I_o = 1.5 A			15 (V_i= 6.5 to 16V)			15 (V_i= 10.2 to 16V)	
V_d	Dropout voltage	I_o = 0.5A		200	400		200	400	mV
		I_o = 1.5A		500	900		500	900	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			0.5			0.8		mV/°C
SVR	Supply voltage rejection	f = 120 Hz I_o = 1A	58	68		58	66		dB
I_{sc}	Short circuit current limit	V_i = 14V		2	2.7		2	2.7	A
				2.2 (V_i = 6.5V)	2.9		2.2 (V_i = 10.2V)	2.9	
Z_o	Output impedance	f = 1 KHz I_o = 0.5A		30			32		mΩ
e_N	Output noise	B = 100 Hz to 100 KHz		30			30		$\mu V/V_o$

ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25°C$, $C_i = 0.1\mu F$, $C_o = 22\mu F$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE				10			12		V
INPUT VOLTAGE (unless otherwise specified)				12			14		V
V_o	Output voltage	I_o = 0.5A	9.8	10	10.2	11.75	12	12.25	V
		I_o = 5 mA to 1.5A	9.6 (V_i= 11.7 to 16V)	10	10.4	11.5 (V_i= 13.8 to 17V)	12	12.5	
V_i	Operating input voltage	I_o = 5 mA			17			17	V
ΔV_o	Line regulation	I_o = 5 mA		3 (V_i = 11 to 17V	8		3 (V_i = 13 to 14V)	7	mV
ΔV_o	Load regulation	I_o = 5 mA to 1.5A		15	35		15	35	mV
		I_o = 0.5A to 1A		10	20		10	25	
I_Q	Quiescent current	I_o = 5 mA		4	8		4	8	mA
		I_o = 1.5A		30 (V_i = 11.7V)	50		30 (V_i = 13.8V)	50	
ΔI_Q	Quiescent current change	I_o = 5 mA			2			1.5	mA
		I_o = 1.5A			13 (V_i= 11.7 to 16V)			10 (V_i = 13.8V)	
V_d	Dropout voltage	I_o = 0.5A		200	400		200	400	mV
		I_o = 1.5A		500	900		500	900	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			1			1.2		mV/°C
SVR	Supply voltage rejection	f = 120 Hz I_o = 1A	56	62		55	61		dB
I_{sc}	Short circuit current limit	V_i = 14V		2	2.7		2	2.7	A
		V_i = 11.7V		2.2	2.9		—	—	
Z_o	Output impedance	f = 1KHz I_o = 0.5A		36			40		mΩ
e_N	Output noise voltage	B = 100 Hz to 100 KHz		30			30		$\mu V/V_o$

Fig. 4 - Dropout voltage vs. output current

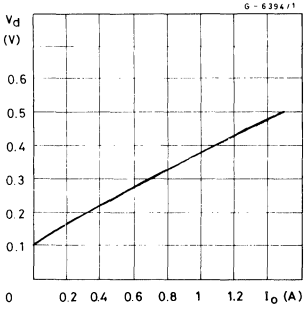


Fig. 5 - Dropout voltage vs. temperature

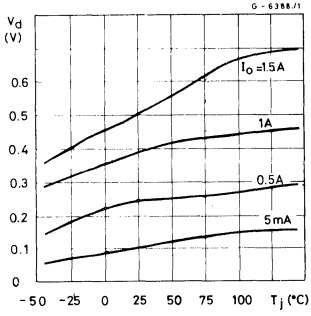


Fig. 6 - Output voltage vs. temperature (L4940V5)

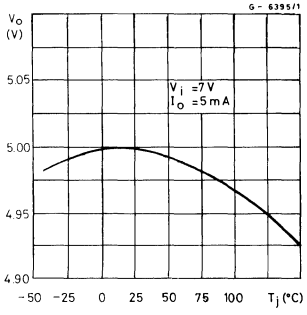


Fig. 7 - Output voltage vs. temperature (L4940V85)

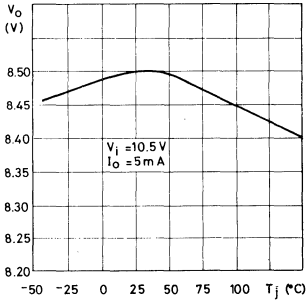


Fig. 8 - Output voltage vs. temperature (L4040V10)

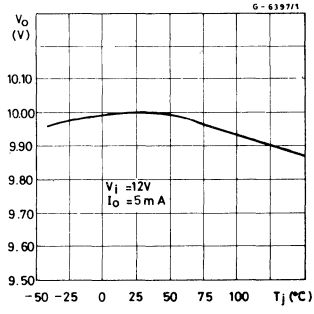


Fig. 9 - Output voltage vs. temperature (L4940V12)

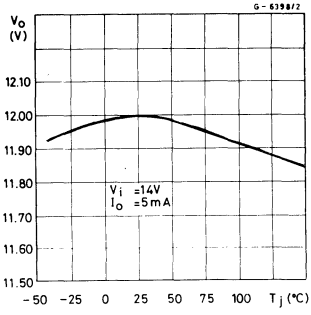


Fig. 10 - Quiescent current vs. temperature (L4940V5)

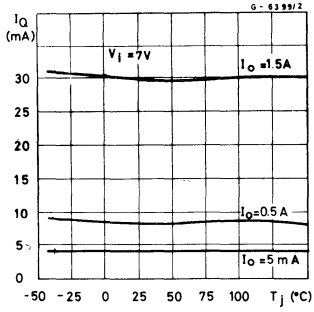


Fig. 11 - Quiescent current vs. input voltage (L4940V5)

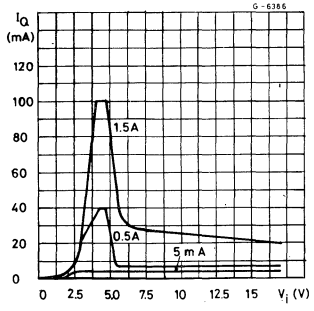


Fig. 12 - Quiescent current vs. output current (L4940V5)

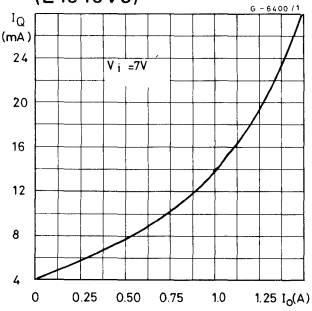


Fig. 13 - Short circuit current vs. temperature (L4940V5)

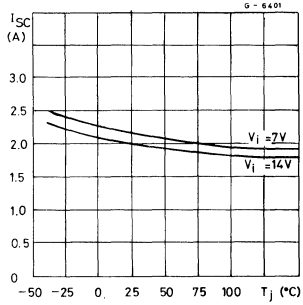


Fig. 14 - Peak output current vs. input/output differential voltage (L4940V5)

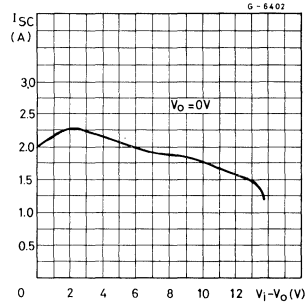


Fig. 15 - Low voltage behavior (L4940V5)

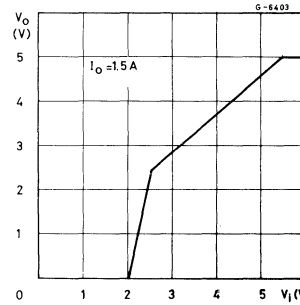


Fig. 16 - Low voltage behavior (L4940V85)

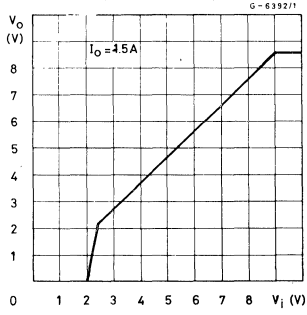


Fig. 17 - Low voltage behavior (L4940V10)

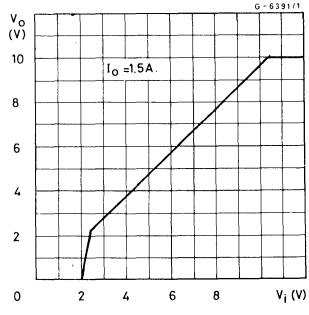


Fig. 18 - Low voltage behavior (L4940V12)

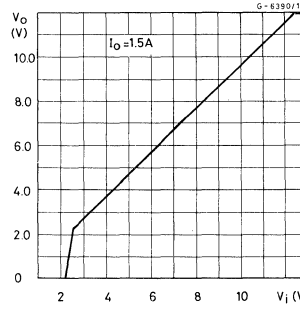


Fig. 19 - Supply voltage rejection vs. frequency (L4940V5)

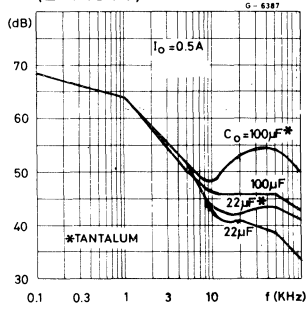


Fig. 20 - Supply voltage rejection vs. output current

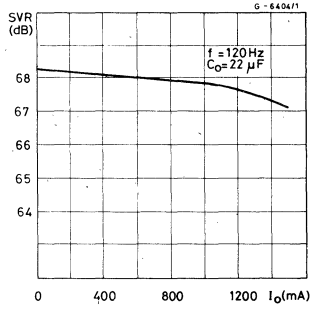


Fig. 21 - Load dump characteristics (L4940V5)

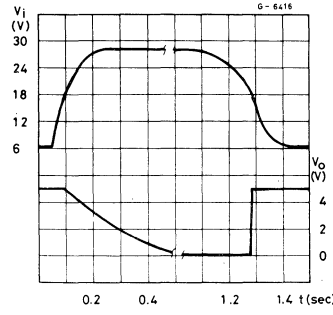


Fig. 22 - Line transient response (L4940V5)

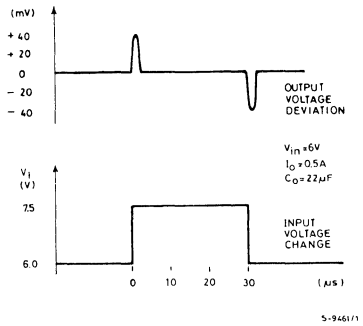


Fig. 23 - Load transient response

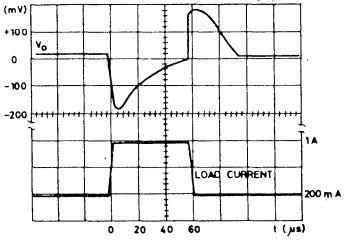


Fig. 24 - Total power dissipation

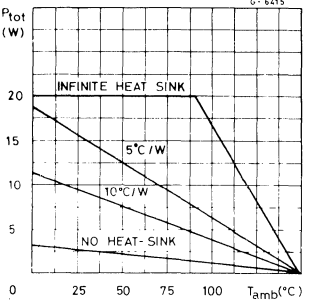


Fig. 25 - Distributed supply with on-card L4940 and L4941 low-drop regulators

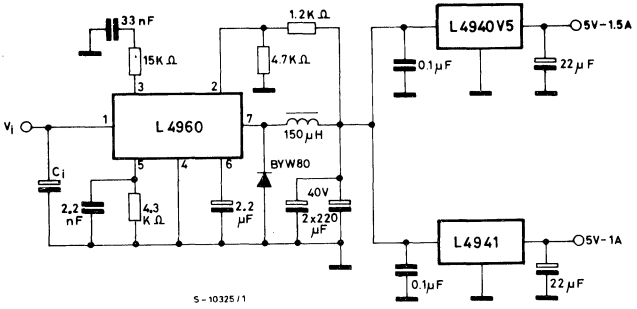
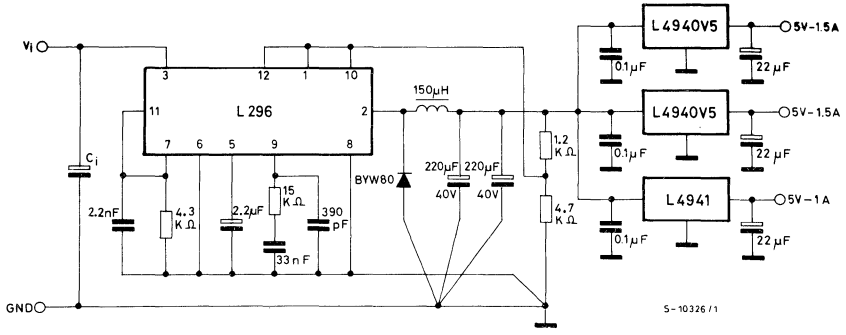


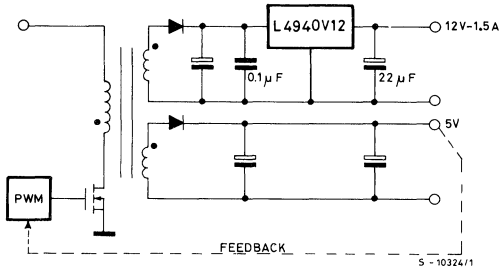
Fig. 26 - Distributed supply with on-card L4940 and L4941 low-drop regulators



ADVANTAGES OF THESE APPLICATIONS ARE:

- On card regulation with short circuit and thermal protection on each output.
- Very high total system efficiency due to the switching preregulation and very low-drop postregulations.

Fig. 27



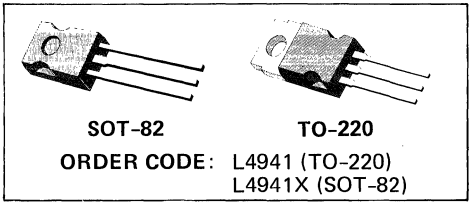
ADVANTAGES OF THIS CONFIGURATION ARE:

- Very high regulation (line and load) on both the output voltages.
- 12V output short-circuit and thermally protected.
- Very high efficiency on the 12V output due to the very low drop regulator.

VERY LOW DROP 1A REGULATOR

PRELIMINARY DATA

- LOW DROPOUT VOLTAGE (450mV TYP AT 1A)
- VERY LOW QUIESCENT CURRENT
- THERMAL SHUTDOWN
- SHORT CIRCUIT PROTECTION
- REVERSE POLARITY PROTECTION



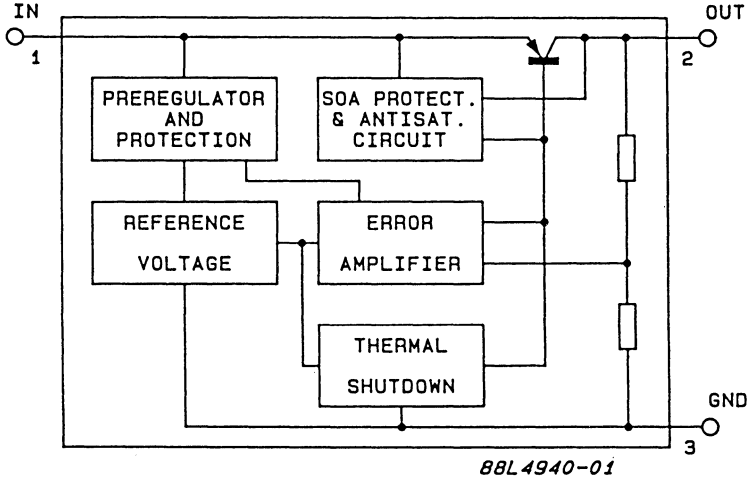
SOT-82 TO-220

ORDER CODE: L4941 (TO-220)
L4941X (SOT-82)

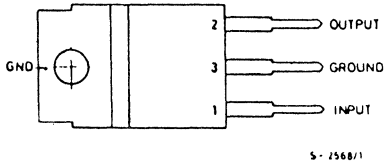
INTRODUCTION

The L4941/X is a three terminal 5V positive regulator available in TO-220 and SOT-82 packages; making it useful in a wide range of the industrial and consumer applications. Thanks to its very low input/output voltage drop, this device is particularly suitable for battery powered equipment, reducing consumption and prolonging battery life. It employes internal current limiting, antisaturation circuit, thermal shutdown and safe area protection.

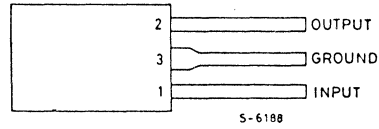
BLOCK DIAGRAM



PIN CONNECTIONS



TO-220



SOT-82

ABSOLUTE MAXIMUM RATINGS

V_i	Forward input voltage	30	V
V_{iR}	Reverse input voltage (R_O = 100Ω)	-15	V
I_O	Output current	Internally limited	
P_{tot}	Power dissipation	Internally limited	
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

THERMAL DATA

			SOT-82	TO-220
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	8 °C/W	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100 °C/W	50 °C/W

TEST CIRCUITS

Fig. 1 - DC Parameters

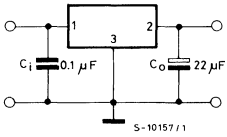


Fig. 2 - Load Regulation

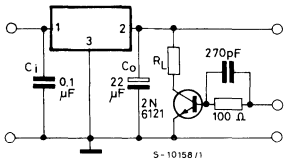
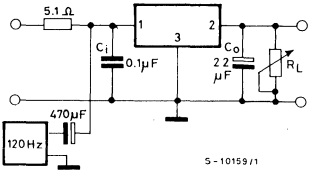


Fig. 3 - Ripple Rejection



ELECTRICAL CHARACTERISTICS (Refer to the test circuits $T_j = 25°C$, $C_i = 0.1\mu F$, $C_o = 22\mu F$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE					5		
INPUT VOLTAGE (unless otherwise specified)					7		
V_o	Output voltage	I_o = 5mA to 1A V_i = 6V to 14V		4.8	5	5.2	V
V_i	Operating input voltage	I_o = 5mA				16	V
ΔV_o	Line regulation	V_i = 6V to 16V I_o = 5mA			5	20	mV
ΔV_o	Load regulation	I_o = 5mA to 1A I_o = 0.5A to 1A			8 5	20 15	mV
I_Q	Quiescent current	V_i = 6V	I_o = 5mA		4	8	mA
			I_o = 1A		20	40	
ΔI_Q	Quiescent current change	V_i = 6V to 14V	I_o = 5mA			3	mA
			I_o = 1A			-10	
V_d	Dropout voltage	I_o = 0.5A			250	450	mV
		I_o = 1A			450	700	
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift				0.6		mV/°C
SVR	Supply voltage rejection	f = 120Hz I_o = 0.5A		58	68		dB
I_{sc}	Short circuit current limit	V_i = 14V			1.6	2.0	A
		V_i = 6V			1.8	2.2	
Z_o	Output impedance	f = 1KHz I_o = 0.5A			30		mΩ
e_N	Output noise voltage	B = 100Hz to 100KHz			30		µV/V_o

Fig. 4 - Dropout voltage vs. output current

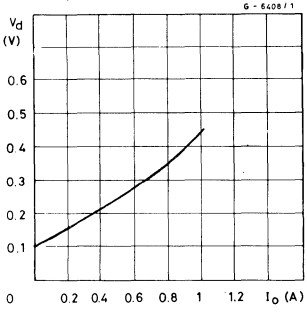


Fig. 5 - Dropout voltage vs. temperature

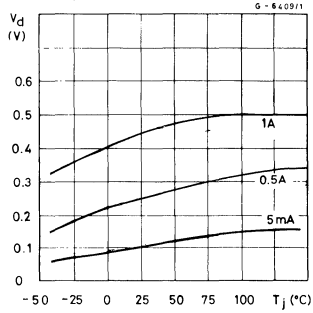


Fig. 6 - Output voltage vs. temperature

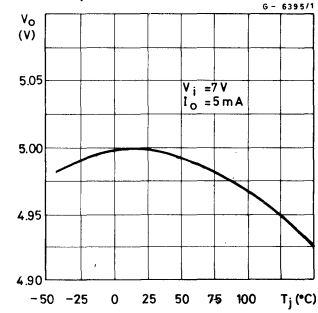


Fig. 7 - Quiescent current vs. temperature

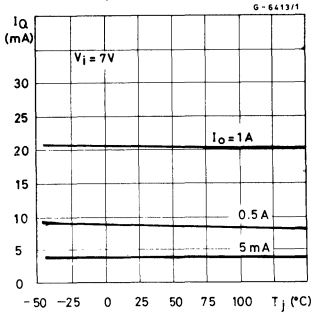


Fig. 8 - Quiescent current vs. input voltage

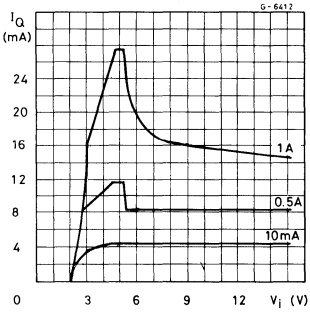


Fig. 9 - Quiescent current vs. output current

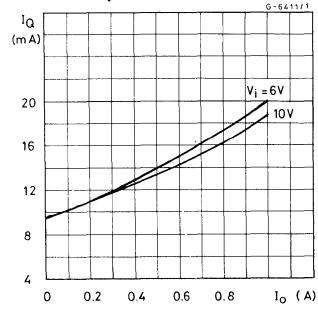


Fig. 10 - Short circuit current vs. temperature

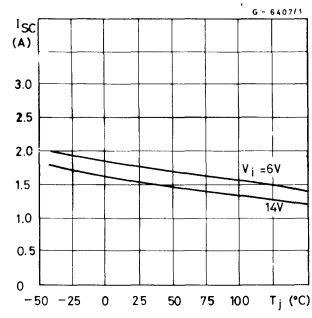


Fig. 11 - Peak output current vs. input/output differential voltage

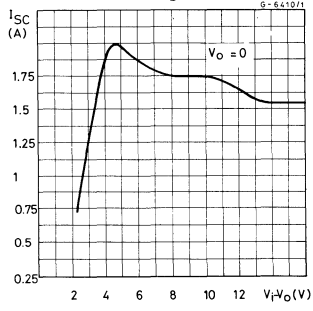


Fig. 12 - Low voltage behavior

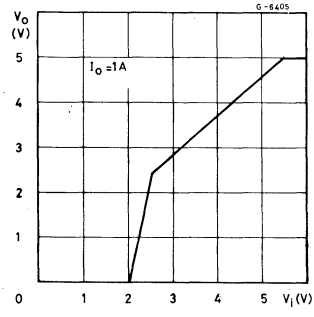


Fig. 13 - Supply voltage rejection vs. frequency

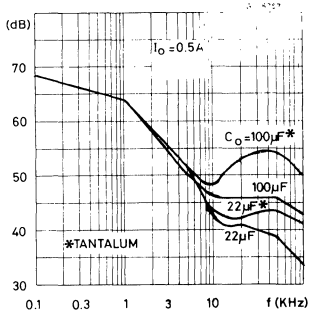


Fig. 14 - Supply voltage rejection vs. output current

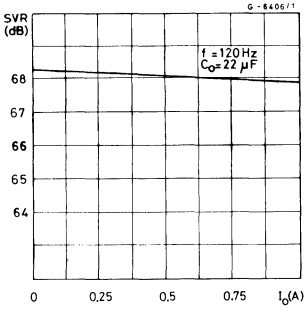


Fig. 15 - Load dump characteristics

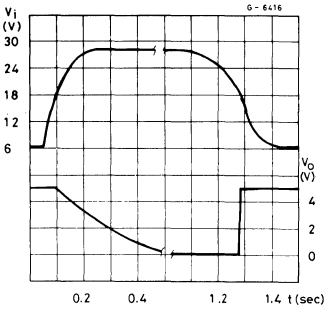


Fig. 16 - Line transient response

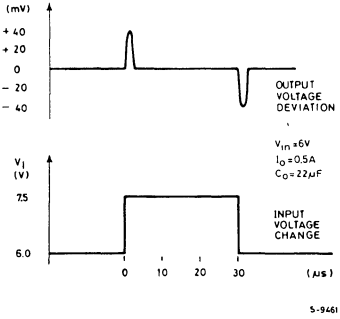


Fig. 17 - Load transunt response

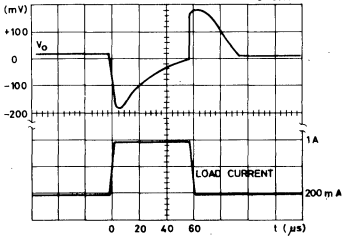


Fig. 18 - Totale power dissipation (TO-220)

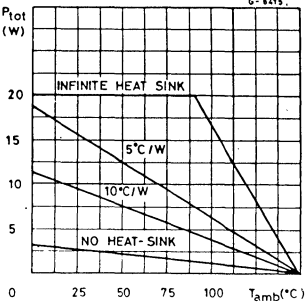
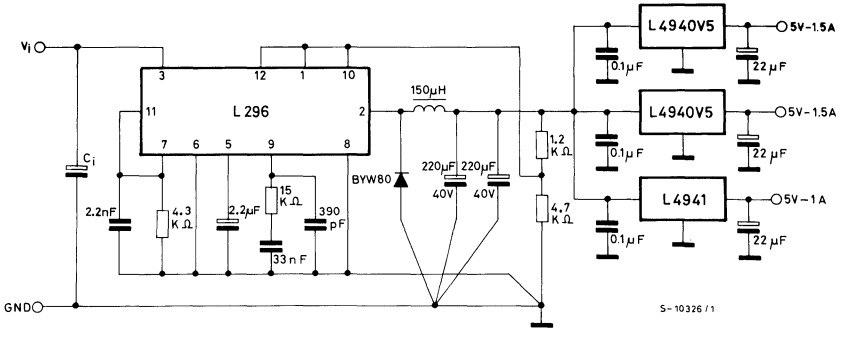


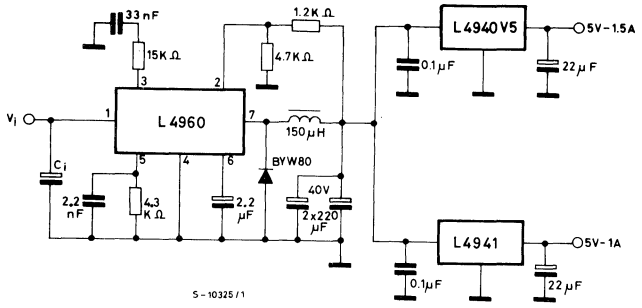
Fig. 19 - Distributed supply with on-card L4940 and L4941 low-drop regulators



ADVANTAGES OF THESE APPLICATIONS ARE:

- On card regulation with short circuit and thermal protection on each output.
- Very high total system efficiency due to the switching preregulation and very low-drop postregulations.

Fig. 20 - Distributed supply with on-card L4940 and L4941 low-drop regulators



2.5A POWER SWITCHING REGULATOR

PRELIMINARY DATA

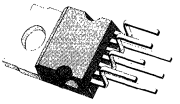
- 2.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2%) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4960 is a monolithic power switching regulator delivering 2.5A at a voltage variable from 5V to 40V in step down configuration.

Features of the device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operation mode.

The L4960 is mounted in a Heptawatt plastic power package and requires very few external componénts.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



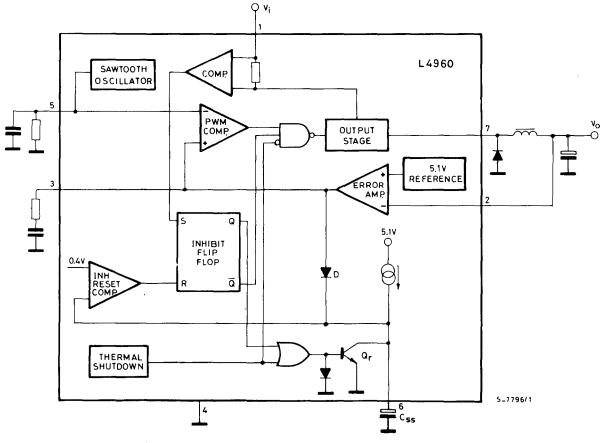
Heptawatt

ORDERING NUMBER: L4960 (Vertical)
L4960H (Horizontal)

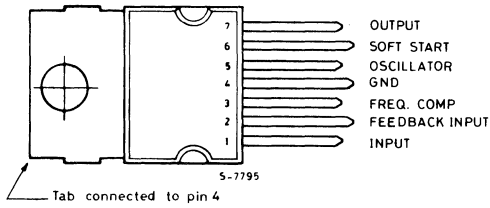
ABSOLUTE MAXIMUM RATINGS

V_1	Input voltage	50	V
$V_1 - V_7$	Input to output voltage difference	50	V
V_7	Negative output DC voltage	-1	V
	Negative output peak voltage at t = 0.1μs; f = 100KHz	-5	V
V_3, V_6	Voltage at pin 3 and 6	5.5	V
V_2	Voltage at pin 2	7	V
I_3	Pin 3 sink current	1	mA
I_5	Pin 5 source current	20	mA
P_{tot}	Power dissipation at $T_{case} \leqslant 90°C$	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

BLOCK DIAGRAM



CONNECTION DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	GROUND	Common ground terminal.
5	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency.
6	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
7	OUTPUT	Regulator output.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_i = 35V$, unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS						
V_o	Output voltage range	$V_i = 46V$ $I_o = 1A$	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V $I_o = 2.5A$	9		46	V
ΔV_o	Line regulation	$V_i = 10V$ to 40V $V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$ $I_o = 0.5A$ to 2A		10	30	mV
V_{ref}	Internal reference voltage (pin 2)	$V_i = 9V$ to 46V $I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to $125°C$ $I_o = 1A$		0.4		mV/°C
V_d	Dropout voltage	$I_o = 2A$		1.4	3	V
I_{om}	Maximum operating load current	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V	2.5			A
I_{7L}	Current limiting threshold (pin 7)	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V	3		4.5	A
I_{SH}	Input average current	$V_i = 46V$; output short-circuit		30	60	mA
η	Efficiency	f = 100KHz $V_o = V_{ref}$		75		%
		$I_o = 2A$ $V_o = 12V$		85		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$ $I_o = 1A$	50	56		dB
f	Switching frequency		85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	$V_i = 9V$ to 46V		0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to $125°C$		1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$ $I_o = 2A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature			150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{1Q}	Quiescent drain current	100% duty cycle pins 5 and 7 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{7L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{6SO}	Source current			100	130	150	μA
I_{6SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{3H}	High level output voltage	V_2 = 4.7V	I_3 = 100μA	3.5			V
V_{3L}	Low level output voltage	V_2 = 5.3V	I_3 = 100μA			0.5	V
I_{3SI}	Sink output current	V_2 = 5.3V		100	150		μA
$-I_{3SO}$	Source output current	V_2 = 4.7V		100	150		μA
I_2	Input bias current	V_2 = 5.2V			2	10	μA
G_v	DC open loop gain	V_3 = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_5$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4960 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 2.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 3. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

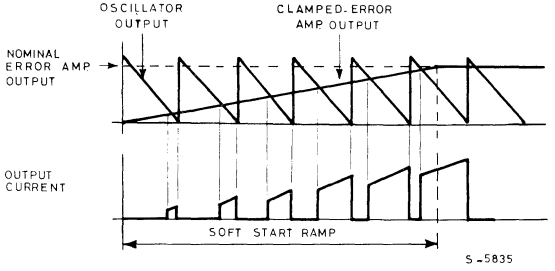


Fig. 2 - Current limiter waveforms

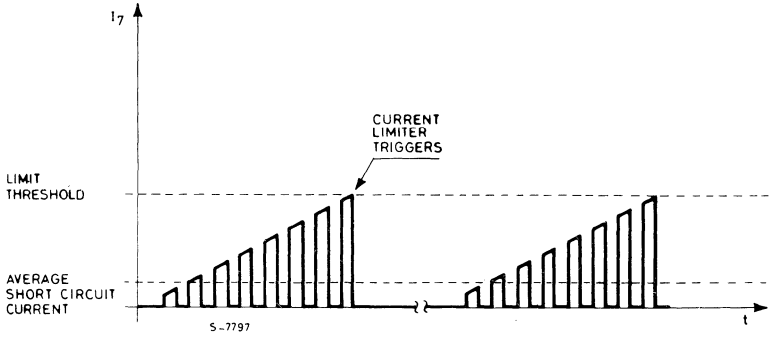
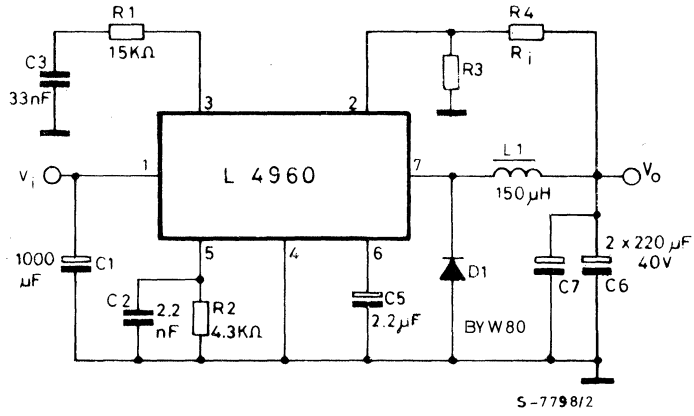


Fig. 3 - Test and application circuit



C6, C7: EKR (ROE)
L1 = 150µH at 5A (COGEMA 946042)
CORE TYPE: MAGNETICS 58206-A2 MPP
N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

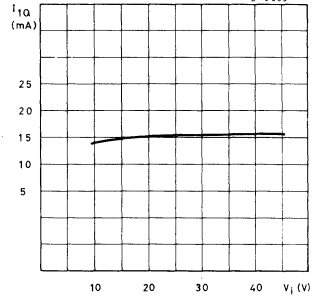


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

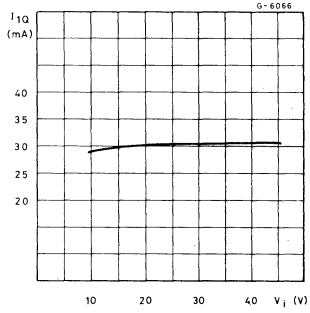


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

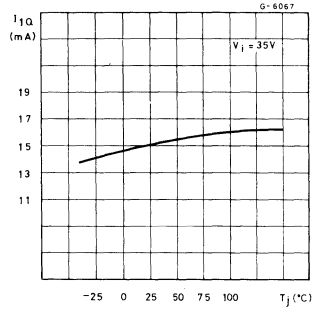


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

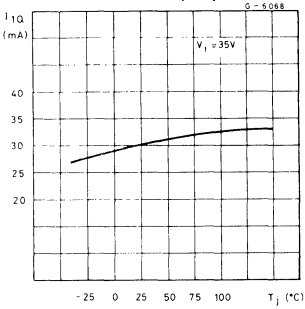


Fig. 8 - Reference voltage (pin 2) vs. V_i

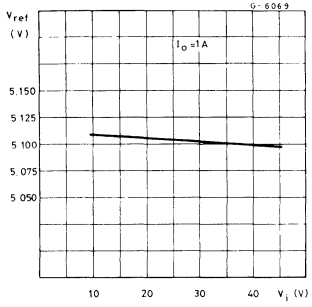


Fig. 9 - Reference voltage vs. junction temperature (pin 2)

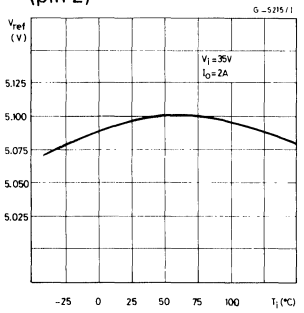


Fig. 10 - Open loop frequency and phase responde of error amplifier

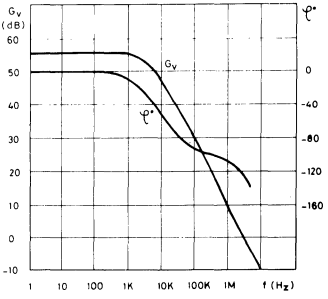


Fig. 11 - Switching frequency vs. input voltage

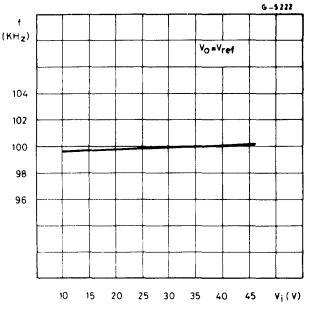


Fig. 12 - Switching frequency vs. junction temperature

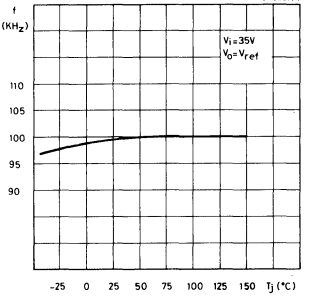


Fig. 13 - Switching frequency vs. R2 (see test circuit)

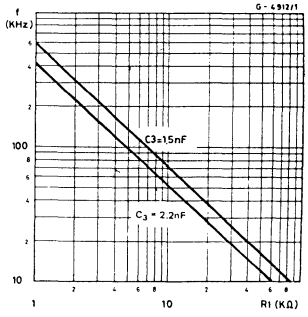


Fig. 14 - Line transient response

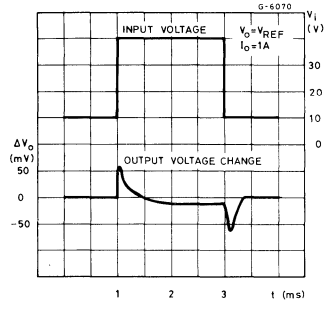


Fig. 15 - Load transient response

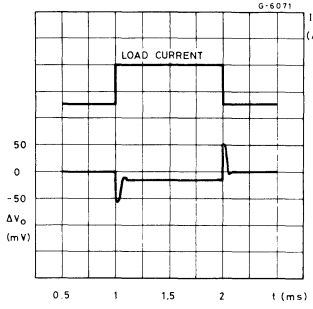


Fig. 16 - Supply voltage ripple rejection vs. frequency

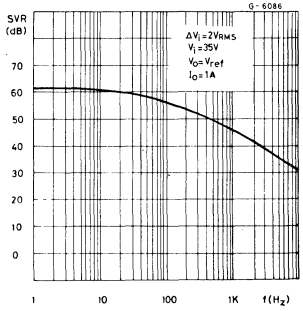


Fig. 17 - Dropout voltage between pin 1 and pin 7 vs. current at pin 7

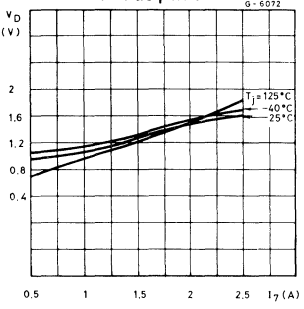


Fig. 18 - Dropout voltage between pin 1 and 7 vs. junction temperature

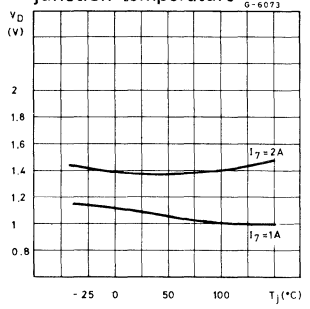


Fig. 19 - Power dissipation derating curve

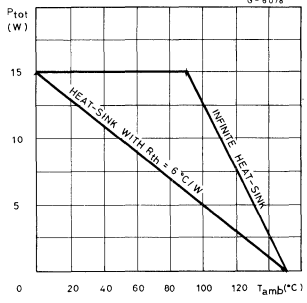


Fig. 20 - Efficiency vs. output current

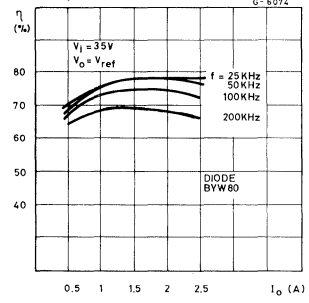


Fig. 21 - Efficiency vs. output current

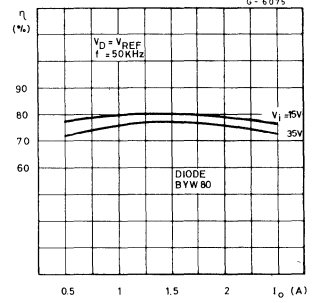


Fig. 22 - Efficiency vs. output current

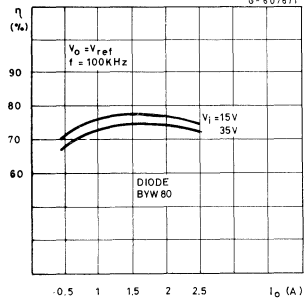
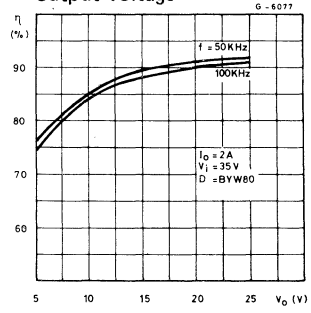
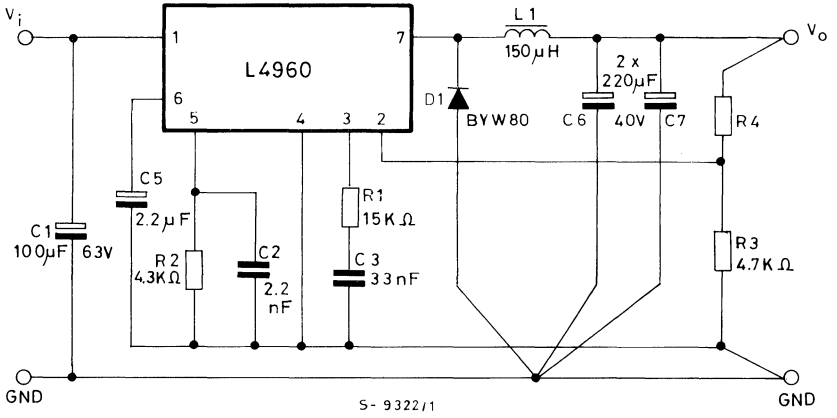


Fig. 23 - Efficiency vs. output voltage



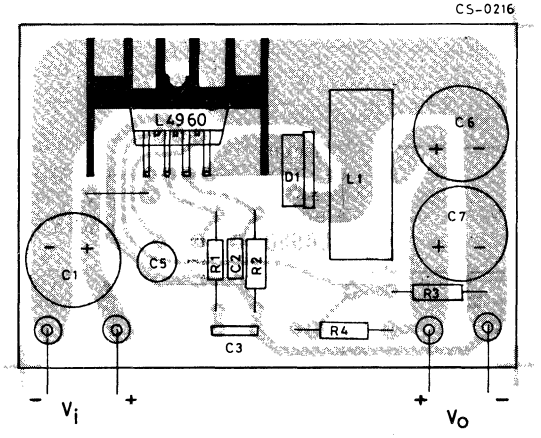
APPLICATION INFORMATION

Fig. 24 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW80 OR 5A SCHOTTKY DIODE
SUGGESTED INDUCTOR: L_1 = 150µH at 5A
CORE TYPE: MAGNETICS 58206 - A2 - MPP
N° TURNS: 45, WIRE GAUGE: 0.8mm (20 AWG), COGEMA 946042
U15/GUP15: N° TURNS: 60, WIRE GAUGE: 0.8mm (20 AWG), AIR GAP: 1mm, COGEMA 969051.

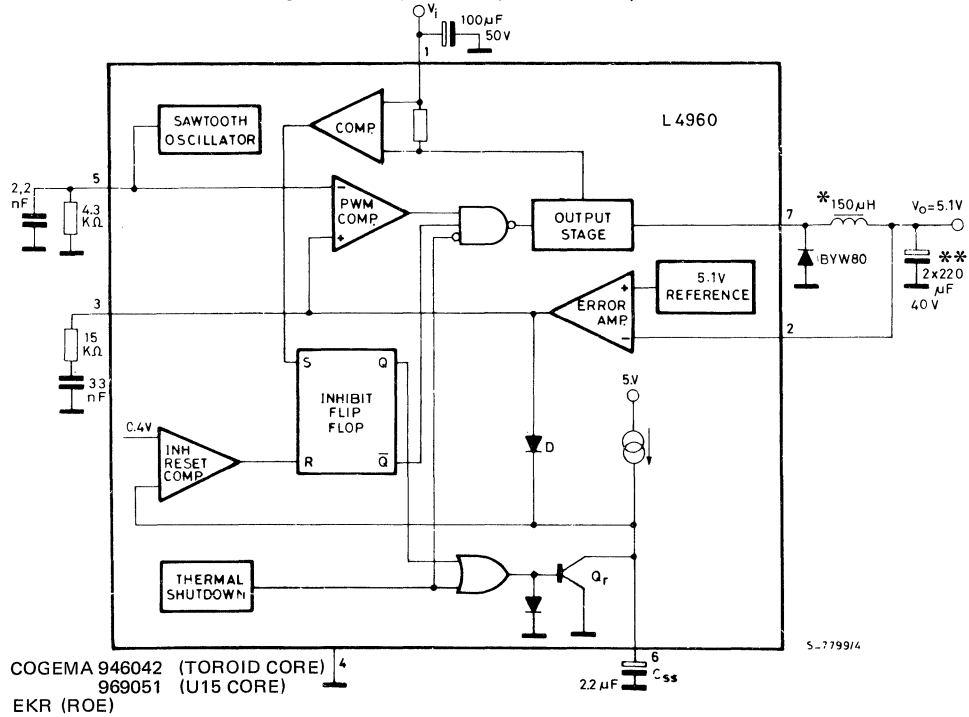
Fig. 25 - P.C. board and component layout of the Fig. 24 (1 : 1 scale)



Resistor values for standard output voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

APPLICATION INFORMATION (continued)

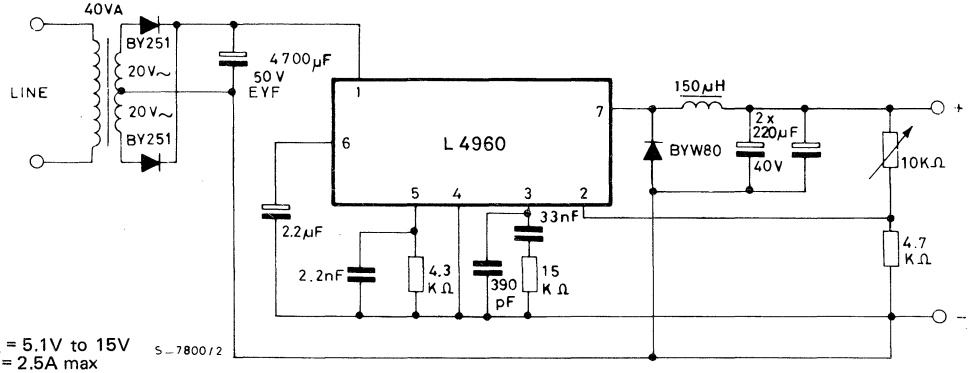
Fig. 26 - A minimal 5.1V fixed regulator; Very few component are required



* COGEMA 946042 (TOROID CORE)
969051 (U15 CORE)

** EKR (ROE)

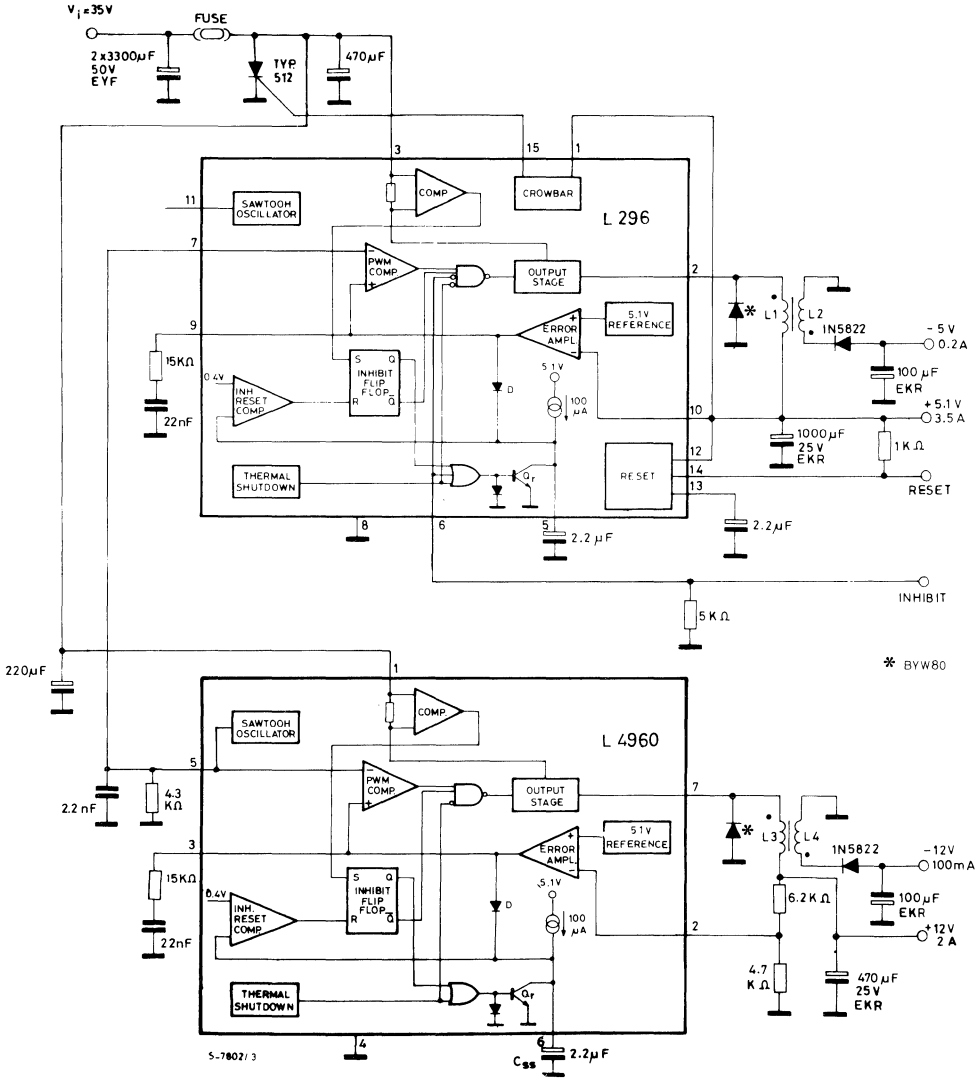
Fig. 27 - Programmable power supply



V_o = 5.1V to 15V
I_o = 2.5A max
Load regulation (1A to 2A) = 10mV (V_o = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_o = 5.1V)

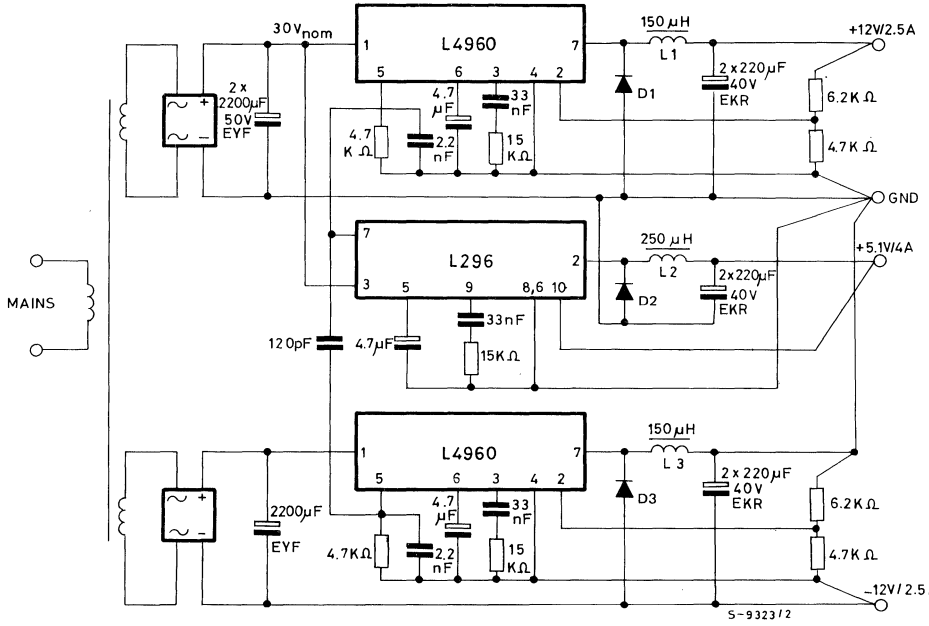
APPLICATION INFORMATION (continued)

Fig. 28 - Microcomputer supply with + 5.1V, -5V, +12V and -12V outputs



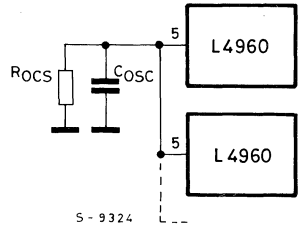
APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/2.5A; a suggestion how to synchronize a negative output



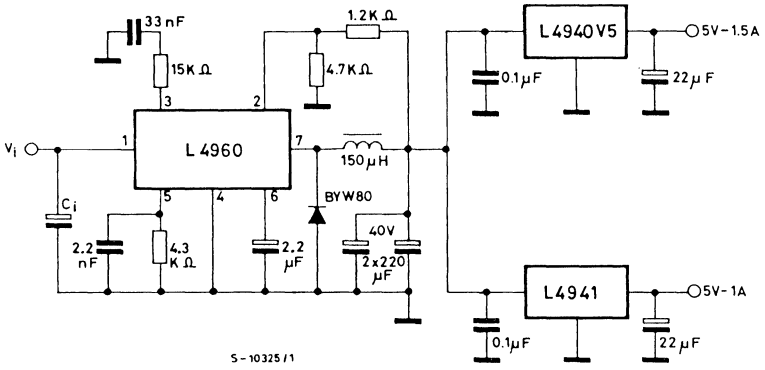
L1, L3 = COGEMA 946042 (969051)
L2 = COGEMA 946044 (946045)
$D_1, D_2, D3$ = BYW80

Fig. 30 - In multiple supplies several L4960s can be synchronized as shown



APPLICATION INFORMATION (continued)

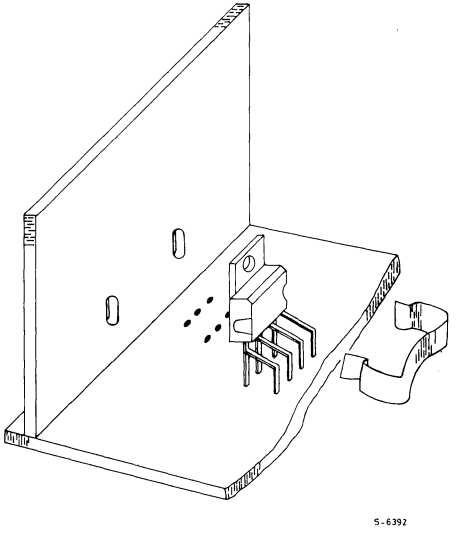
Fig. 31 - Regulator for distributed supplies



MOUNTING INSTRUCTION

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Heptawatt package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact, no electrical isolation is needed between the two surfaces.

Fig. 32 - Mounting example



SGS-THOMSON MICROELECTRONICS

L4962

1.5A POWER SWITHING REGULATOR

PRELIMINARY DATA

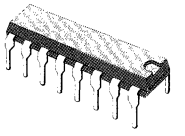
- 1.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- PRECISE (± 2 %) ON-CHIP REFERENCE
- HIGH SWITCHING FREQUENCY
- VERY HIGH EFFICIENCY (UP TO 90%)
- VERY FEW EXTERNAL COMPONENTS
- SOFT-START
- INTERNAL LIMITING CURRENT
- THERMAL SHUTDOWN

The L4962 is a monolithic power switching regulator delivering 1.5A at a voltage veriable from 5V to 40V in step down configuration.

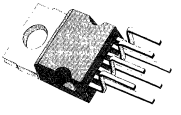
Features of device include current limiting, soft start, thermal protection and 0 to 100% duty cycle for continuous operating mode.

The L4962 is mounted in a 16-lead Powerdip plastic package and Heptawatt package and requires very few external components.

Efficient operation at switching frequencies up to 150KHz allows a reduction in the size and cost of external filter components.



Powerdip
(12 + 2 + 2)



Heptawatt

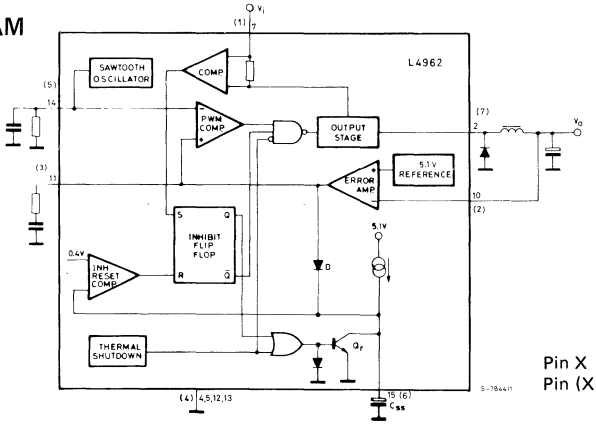
ORDERING NUMBER:

L4962 (12 + 2 + 2 Powerdip)
L4962E (Heptawatt)
L4962EH (Horizontal Heptawatt)

ABSOLUTE MAXIMUM RATINGS

V_7	Input voltage	50	V
$V_7 - V_2$	Input to output voltage difference	50	V
V_2	Negative output DC voltage	-1	V
	Output peak voltage at t = 0.1μs, f = 100KHz	-5	V
V_{11}, V_{15}	Voltage at pin 11, 15	5.5	V
V_{10}	Voltage at pin 10	7	V
I_{11}	Pin 11 sink current	1	mA
I_{14}	Pin 14 source current	20	mA
P_{tot}	Power dissipation at $T_{pins} \leqslant 90°C$ (Powerdip)	4.3	W
	$T_{case} \leqslant 90°C$ (Heptawatt)	15	W
T_j, T_{stg}	Junction and storage temperature	-40 to 150	°C

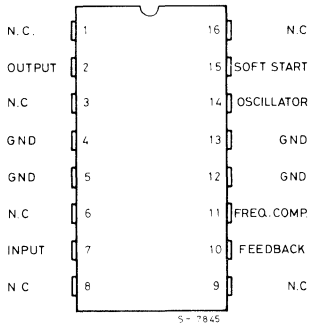
BLOCK DIAGRAM

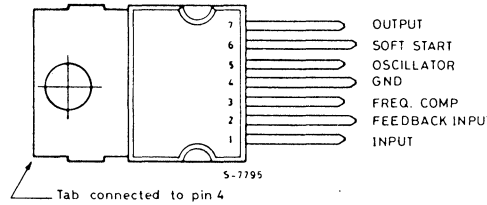


Pin X = Powerdip
Pin (X) = Heptawatt

CONNECTION DIAGRAMS

(Top view)





THERMAL DATA

			Heptawatt	Powerdip
$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4°C/W	–
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	–	14°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	50°C/W	80°C/W*

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

HEPTAWATT	POWERDIP	NAME	FUNCTION
1	7	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
2	10	FEEDBACK INPUT	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
3	11	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
4	4, 5, 12, 13	GROUND	Common ground terminal.
5	14	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
6	15	SOFT START	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. The capacitor also determines the average short circuit output current.
7	2	OUTPUT	Regulator output.
	1, 3, 6, 8, 9, 16		N.C.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_j = 25°C$, $V_i = 35V$, unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS							
V_o	Output voltage range	$V_i = 46V$	$I_o = 1A$	V_{ref}		40	V
V_i	Input voltage range	$V_o = V_{ref}$ to 36V	$I_o = 1.5A$	9		46	V
ΔV_o	Line regulation	$V_i = 10V$ to 40V	$V_o = V_{ref}$ $I_o = 1A$		15	50	mV
ΔV_o	Load regulation	$V_o = V_{ref}$	$I_o = 0.5A$ to 1.5A		8	20	mV
V_{ref}	Internal reference voltage (pin 10)	$V_i = 9V$ to 46V	$I_o = 1A$	5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of refer. voltage	$T_j = 0°C$ to $125°C$ $I_o = 1A$			0.4		mV/°C
V_d	Dropout voltage	$I_o = 1.5A$			1.5	2	V
I_{om}	Maximum operating load current	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V		1.5			A
I_{2L}	Current limiting threshold (pin 2)	$V_i = 9V$ to 46V $V_o = V_{ref}$ to 36V		2		3.3	A
I_{SH}	Input average current	$V_i = 46V$; output short-circuit			15	30	mA
η	Efficiency	f = 100KHz	$V_o = V_{ref}$		70		%
		$I_o = 1A$	$V_o = 12V$		80		%
SVR	Supply voltage ripple rejection	$\Delta V_i = 2V_{rms}$ $f_{ripple} = 100Hz$ $V_o = V_{ref}$	$I_o = 1A$	50	56		dB
f	Switching frequency			85	100	115	KHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	$V_i = 9V$ to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	$T_j = 0°C$ to $125°C$			1		%
f_{max}	Maximum operating switching frequency	$V_o = V_{ref}$	$I_o = 1A$	120	150		KHz
T_{sd}	Thermal shutdown junction temperature				150		°C

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
I_{7Q}	Quiescent drain current	100% duty cycle pins 2 and 14 open	V_I = 46V		30	40	mA
		0% duty cycle			15	20	mA
$-I_{2L}$	Output leakage current	0% duty cycle				1	mA
SOFT START							
I_{15SO}	Source current			100	130	160	μA
I_{15SI}	Sink current			50	70	120	μA
ERROR AMPLIFIER							
V_{11H}	High level output voltage	V_{10} = 4.7V	I_{11} = 100μA	3.5			V
V_{11L}	Low level output voltage	V_{10} = 5.3V	I_{11} = 100μA			0.5	V
I_{11SI}	Sink output current	V_{10} = 5.3V		100	150		μA
$-I_{11SO}$	Source output current	V_{10} = 4.7V		100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V			2	10	μA
G_v	DC open loop gain	V_{11} = 1V to 3V		46	55		dB
OSCILLATOR							
$-I_{14}$	Oscillator source current			5			mA

CIRCUIT OPERATION (refer to the block diagram)

The L4962 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 1.5A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%).

This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.

The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 11. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source. Output overload protection is provided in the form of a current limiter. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V.

The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network. The thermal overload circuit disables circuit operation when the junction temperature reaches about 150°C and has hysteresis to prevent unstable conditions.

Fig. 1 - Soft start waveforms

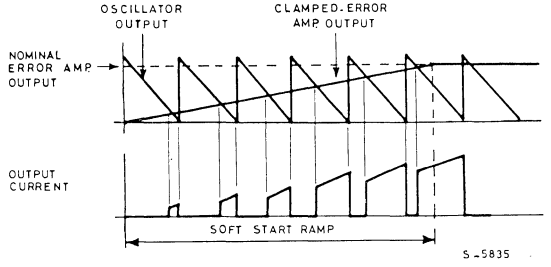


Fig. 2 - Current limiter waveforms

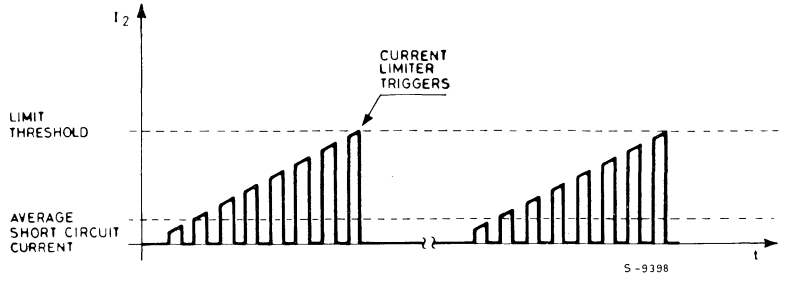
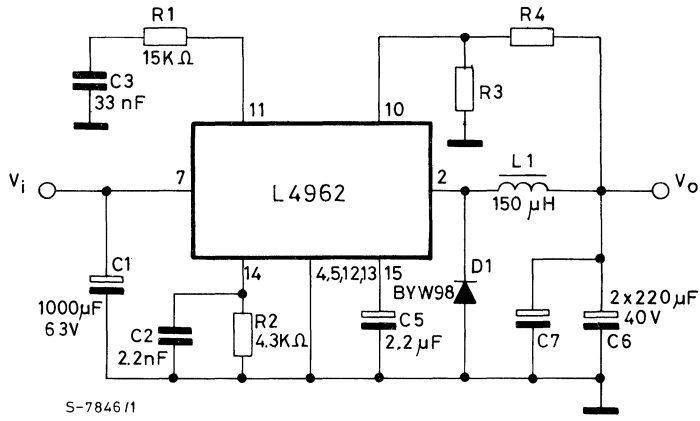


Fig. 3 - Test and application circuit (Powerdip)



1) D_1: BYW98 or 3A Schottky diode, 45V of VRRM;
2) L_1: CORE TYPE - MAGNETICS 58120 - A2 MPP
   N° TURNS 45, WIRE GAUGE: 0.8mm (20 AWG)
3) C_6, C_7: ROE, EKR 220μF 40V

Fig. 4 - Quiescent drain current vs. supply voltage (0% duty cycle)

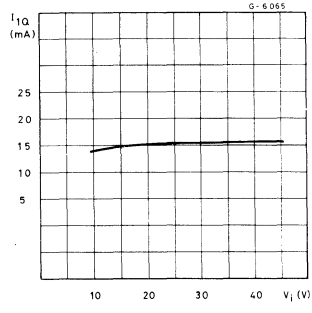


Fig. 5 - Quiescent drain current vs. supply voltage (100% duty cycle)

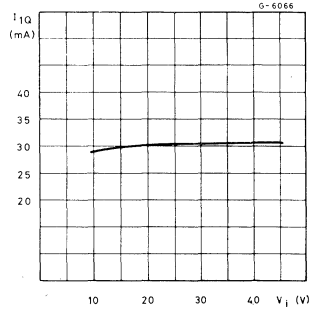


Fig. 6 - Quiescent drain current vs. junction temperature (0% duty cycle)

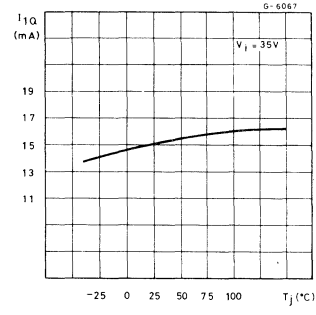


Fig. 7 - Quiescent drain current vs. junction temperature (100% duty cycle)

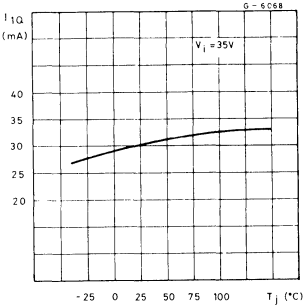


Fig. 8 - Reference voltage (pin 10) vs. V_I rdip) vs. V_i

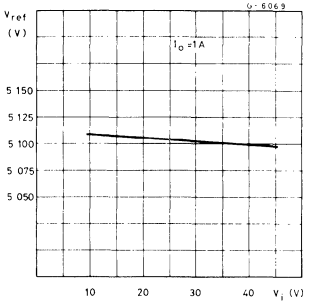


Fig. 9 - Reference voltage (pin 10) vs. junction temperature

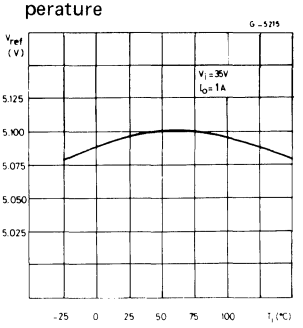


Fig. 10 - Open loop frequency and phase response of error amplifier

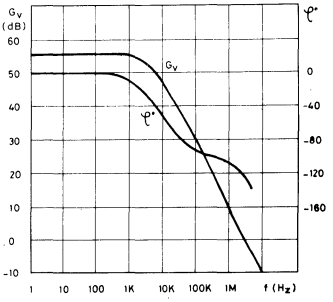


Fig. 11 - Switching frequency vs. input voltage

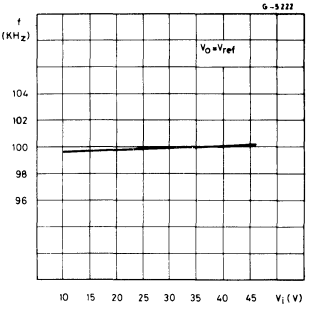


Fig. 12 - Switching frequency vs. junction temperature

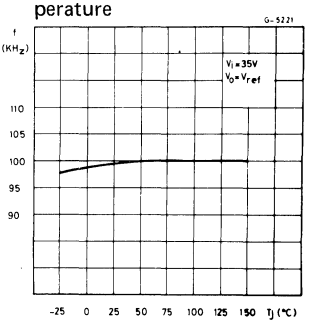


Fig. 13 - Switching frequency vs. R2 (see test circuit)

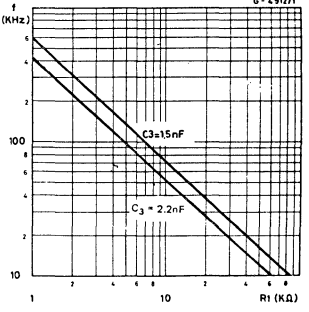


Fig. 14 - Line transient response

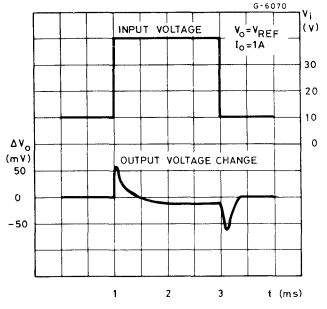


Fig. 15 - Load transient response

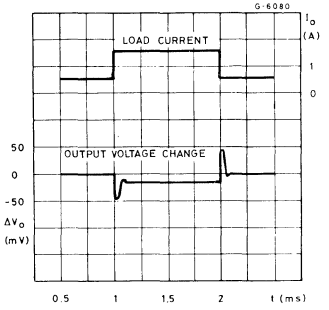


Fig. 16 - Supply voltage ripple rejection vs. frequency

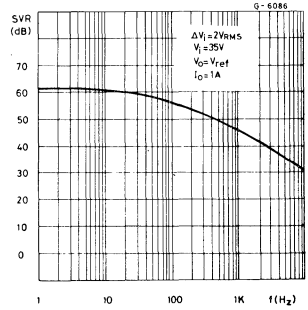


Fig. 17 - Dropout voltage between pin 7 and pin 2 vs. current at pin 2

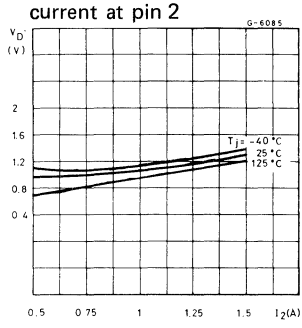


Fig. 18 - Dropout voltage between pin 7 and 2 vs. junction temperature

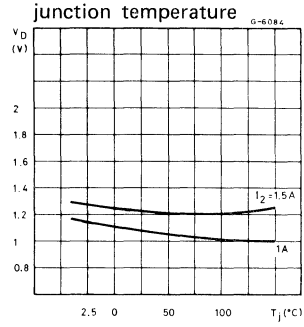


Fig. 19 - Efficiency vs. output current

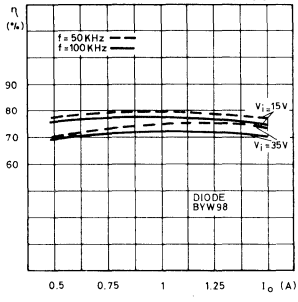


Fig. 20 - Efficiency vs. output current

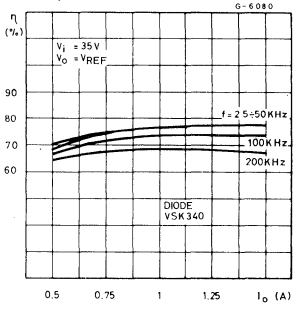


Fig. 21 - Efficiency vs. output current

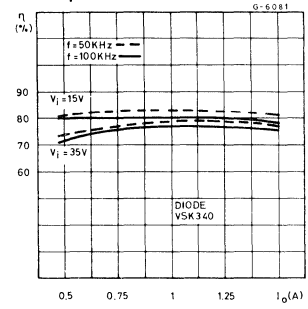


Fig. 22 - Efficiency vs. output voltage

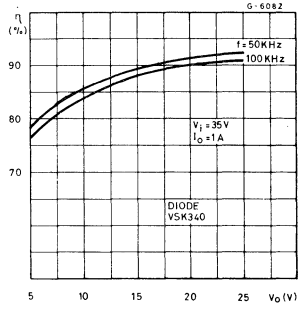


Fig. 23 - Efficiency vs. output voltage

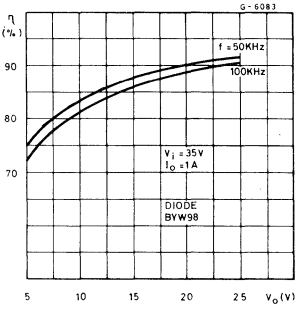
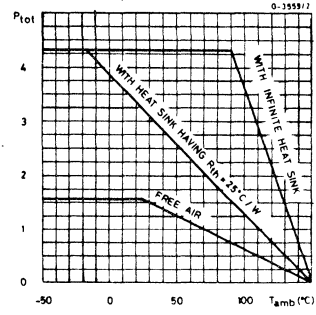
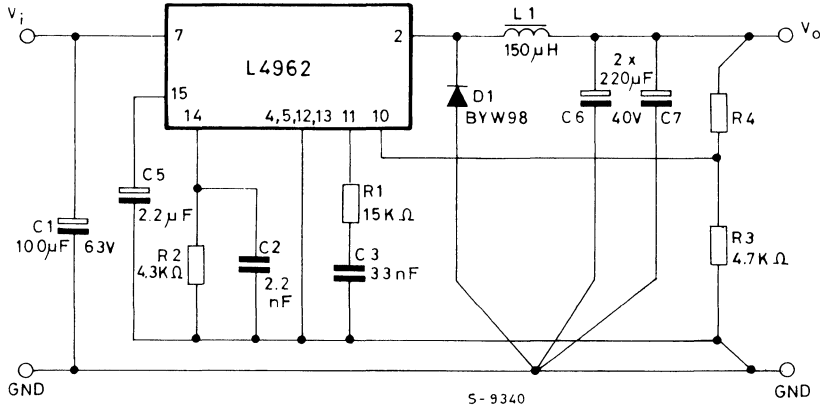


Fig. 24 - Maximum allowable power dissipation vs. ambient temperature (Powerdip)



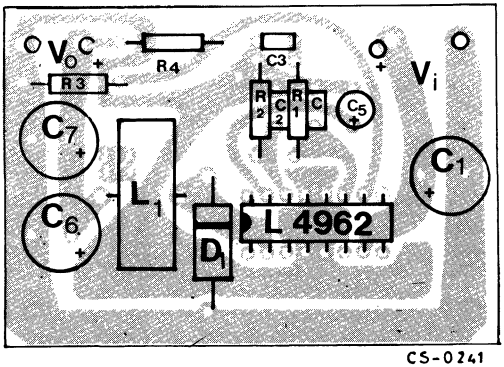
APPLICATION INFORMATION

Fig. 25 - Typical application circuit



C_1, C_6, C_7: EKR (ROE)
D_1: BYW98 OR VISK340 (SCHOTTKY)
SUGGESTED INDUCTORS (L_1): MAGNETICS 58120 - A2MPP - 45 TURNS - WIRE GAUGE 0.8mm (20AWG) - COGEMA 946043
OR U15, GUP15, 60 TURNS 1mm, AIR GAP 0.8mm (20AWG) - COGEMA 969051

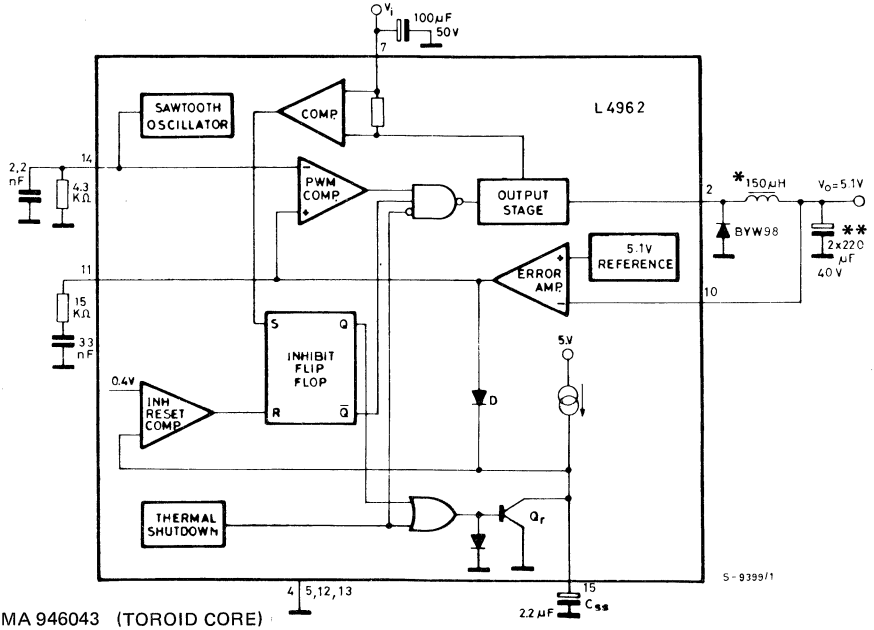
Fig. 26 - P.C. board and component layout of the circuit of Fig. 25 (1 : 1 scale)



Resistor values for standard output 7 voltages		
V_o	R3	R4
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

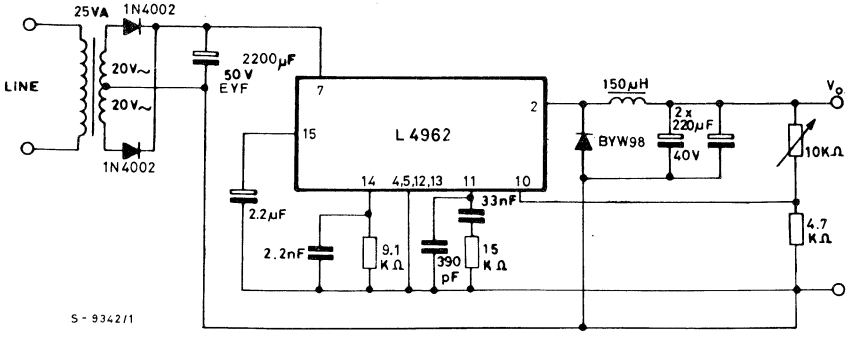
APPLICATION INFORMATION (continued)

Fig. 27 - A minimal 5.1V fixed regulator; very few components are required



* COGEMA 946043 (TOROID CORE)
969051 (U15 CORE)
** EKR (ROE)

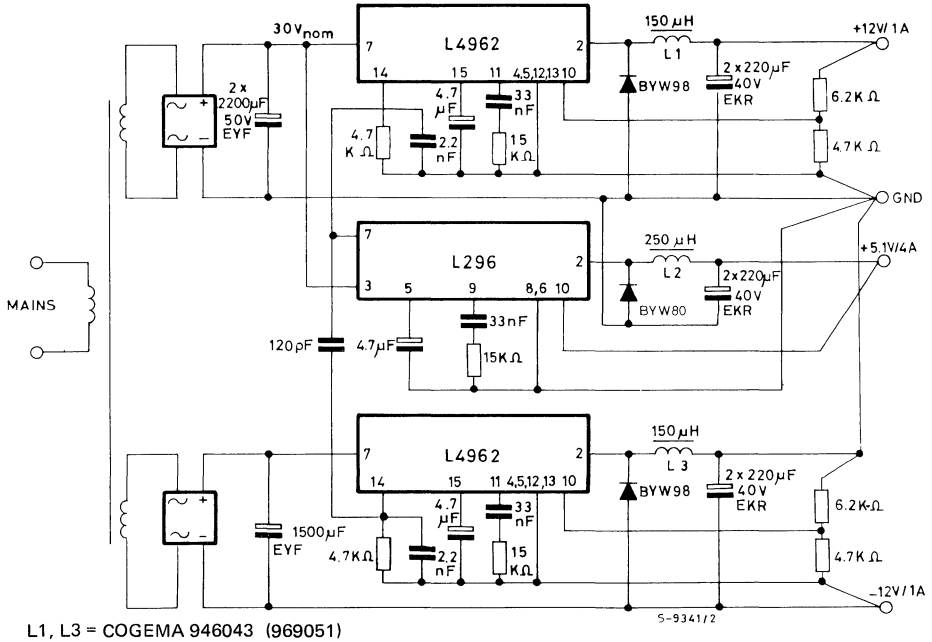
Fig. 28 - Programmable power supply



V_O = 5.1V to 15V
I_O = 1.5A max
Load regulation (0.5A to 1.5A) = 10mV (V_O = 5.1V)
Line regulation (220V ± 15% and to I_O = 1A) = 15mV (V_O = 5.1V)

APPLICATION INFORMATION (continued)

Fig. 29 - DC-DC converter 5.1V/4A, ± 12V/1A. A suggestion how to synchronize a negative output



L1, L3 = COGEMA 946043 (969051)
L2 = COGEMA 946044 (946045)

Fig. 30 - In multiple supplies several L4962s can be synchronized as shown

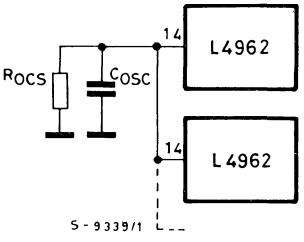
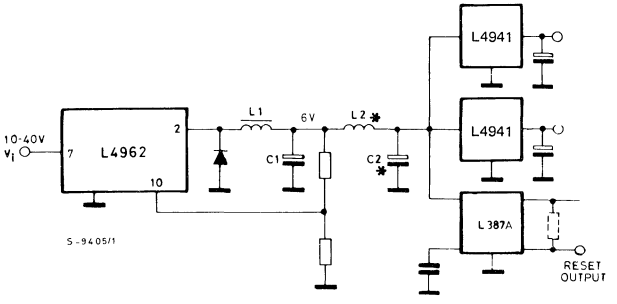


Fig. 31 - Preregulator for distributed supplies



* L2 and C2 are necessary to reduce the switching frequency spikes when linear regulators are remote from L4962

MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L4962 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 32).
The diagram of figure 33 shows the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having the thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 32 - Example of P.C. board copper area which is used as heatsink

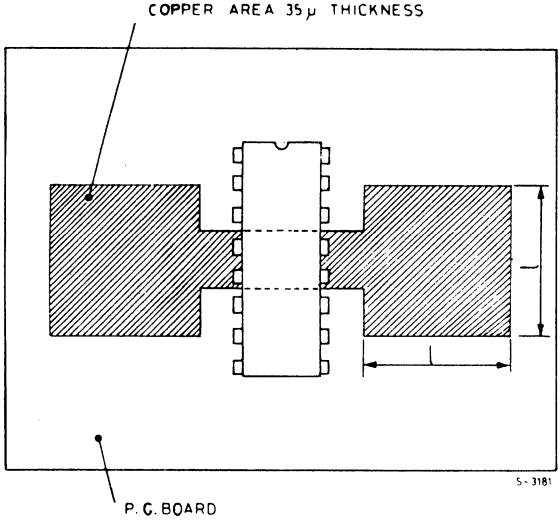
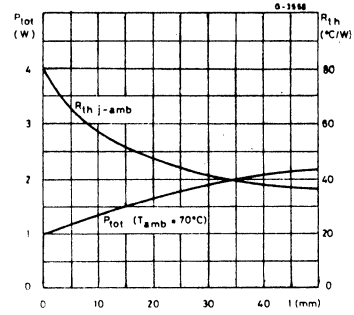


Fig. 33 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"



HIGH CURRENT SWITCHING REGULATOR

- 4 A OUTPUT CURRENT
- 5.1 V TO 28 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (± 3 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 120 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- CURRENT LIMITING
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN

DESCRIPTION

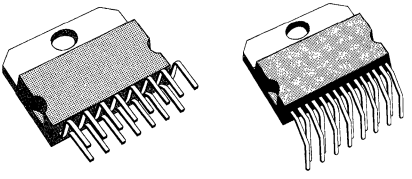
The L4964 is a stepdown power switching regulator delivering 4 A at a voltage variable from 5.1 V to 28 V.

Features of the device include overload protection, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L4964 is mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

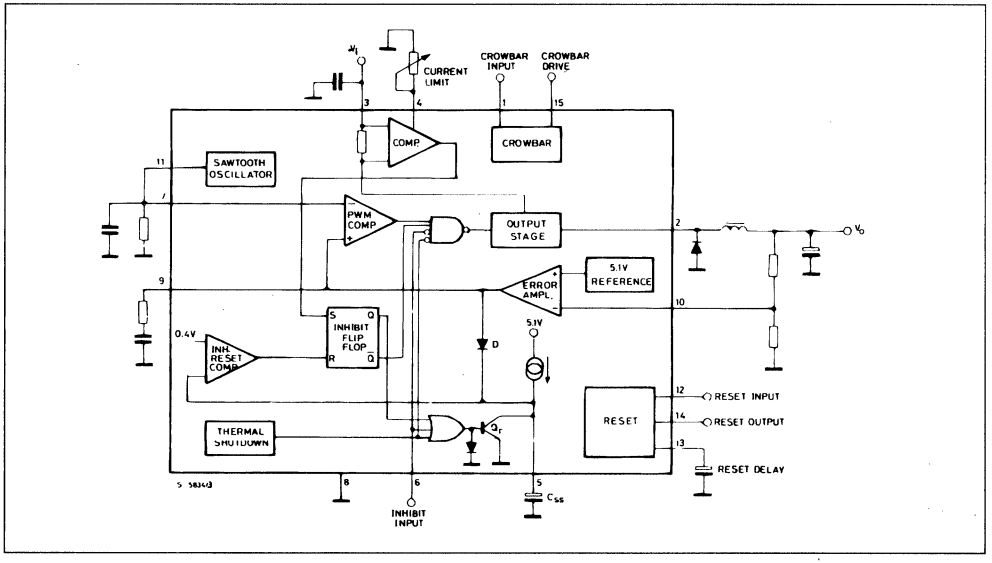
Efficient operation at switching frequencies up to 120 KHz allows a reduction in the size and cost of external filter components.

Multiwatt®
(15-lead)



ORDER CODES : L4964
L4964HT

BLOCK DIAGRAM



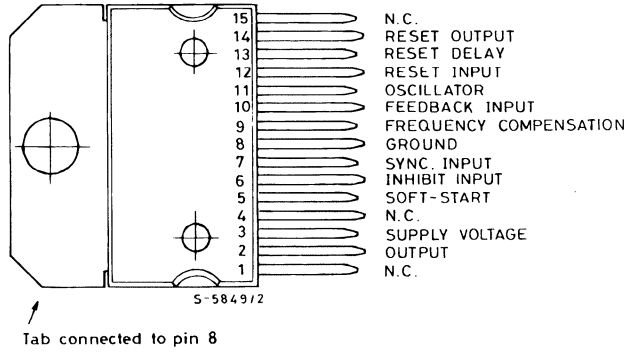
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage (pin 3)	36	V
$V_i - V_2$	Input to Output Voltage Difference	38	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 100 kHz	–1 –7	V V
V_{12}	Voltage at Pin 12	10	V
V_5, V_7, V_9	Voltage at Pins 5, 7 and 9	5.5	V
V_{10}, V_6, V_{13}	Voltage at Pins 10, 6 and 13	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

CONNECTION DIAGRAM (top view)



Note : Pins 1, 4, 15 must not be connected. Leave open circuit.

PIN FUNCTIONS

N°	Name	Function
1	N.C.	Must not be connected. Leave open circuit.
2	OUTPUT	Regulator Output.
3	SUPPLY VOLTAGE	Unregulated Voltage Input. An internal regulator powers the L4964's internal logic.
4	N.C.	Must not be connected. Leave open circuit.
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL - Level Remote Inhibit. A logic high level on this input disables the L4964.
7	SYNC INPUT	Multiple L4964's are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal.
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC network connected to this terminal determines the switching frequency. The pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the beedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open Collector Reset Signal Output. This output is high when the supply is safe.
15	N.C.	Must not be connected. Leave open circuit.

CIRCUIT OPERATION (refer to the block diagram)

The L4964 is a monolithic stepdown switching regulator providing output voltages from 5.1 V to 28 V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1 V on-chip reference (zener zap trimmed to ± 3 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be ajusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1 V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor C_{ss} and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4 V. The output stage is thus re-enable and the output voltage rises under contro of the soft start network. If the overload condition is still present the limiter will trigger again when the thershold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

A TTL - level input is provided for applications such as remote on/off control. This input is activated by high level and disables circuit operation. After an inhibit the L4964 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms.

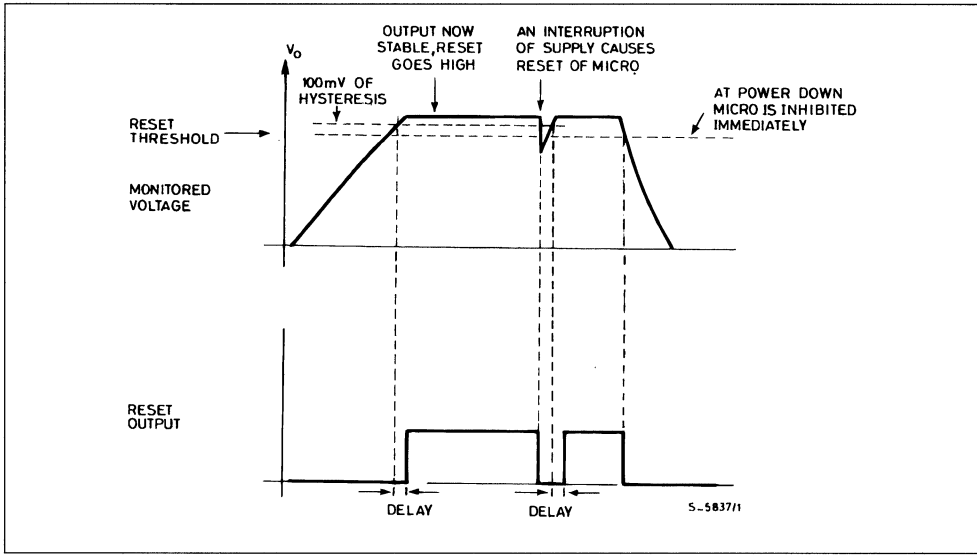


Figure 2 : Soft Start Waveforms.

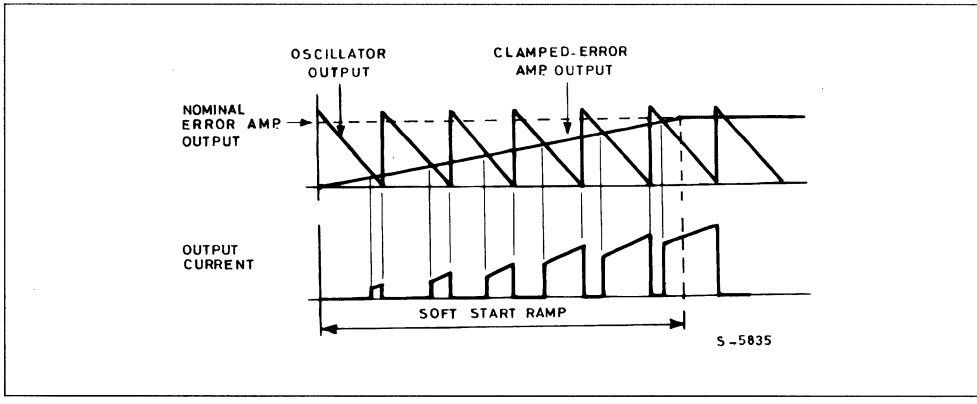
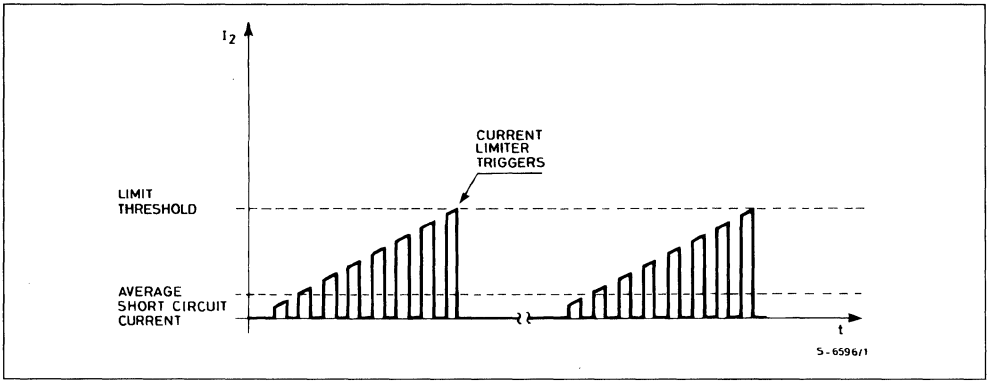


Figure 3 : Current Limiter Waveforms.



ELECTRICAL CHARACTERISTICS (refer to the test circuits T_j = 25 °C, V_i = 25 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)

V_o	Output Voltage Range	V_i = 36 V I_o = 1 A	V_{ref}		28	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 28 V I_o = 3 A	9		36	V	4
ΔV_o	Line Regulation	V_i = 10 V to 30 V, $V_o = V_{ref}$, I_o = 2 A		15	70	mV	4
ΔV_o	Load Regulation	I_o = 1 A to 2 A		10	30	mV	4
		$V_o = V_{ref}$ I_o = 0.5 A to 3 A		15	50	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9 V to 36 V I_o = 2 A	4.95	5.1	5.25	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0 °C to 125 °C I_o = 2 A		0.4		mV/°C	
V_d	Dropout Voltage between Pin 2 and Pin 3	I_o = 3 A		2	3.2	V	4
		I_o = 2 A		1.5	2.4	V	4
Io_m	Maximum Operating Load Current	V_i = 9 V to 36 V, $V_o = V_{ref}$ to 28 V	4			A	4
I_{2L}	Current Limiting Threshold (pin 2)	V_i = 9 V to 36 V $V_o = V_{ref}$ to 28 V	4.5		8	A	4
I_{SH}	Input Average Current	V_i = 36 V ; Output Short-circuited		80	140	mA	4

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.

DYNAMIC CHARACTERISTICS (continued)

η	Effiency	$I_o = 3$ A	$V_o = V_{ref}$		75		%	4
			$V_o = 12$ V		85		%	4
SVR	Supply Voltage Ripple Rejection	$\Delta V_I = 2\ V_{rms}$ $V_o = V_{ref}$	$f_{ripple} = 100$ Hz $I_o = 2$ A	46	56	–	dB	4
f	Switching Frequency			40	50	60	kHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	$V_i = 9$ V to 36 V			0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	$T_j = 0$ °C to 125 °C			1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$ $I_o = 1$ A		120			kHz	–
T_{sd}	Thermal Shutdown Junction Temperature			135	145		°C	–

DC CHARACTERISTICS

I_{3Q}	Quiescent Drain Current	$V_i = 36$ V $V_7 = 0$ V S1 : B S2 : B	$V_6 = 0$		66	100	mA	6a
			$V_6 = 3$ V		30	50	mA	6a
$-I_{2L}$	Output Leakage Current	$V_i = 36$ V, V6 = 3 V, S1 : B, S2 : A, $V_7 = 0$ V				2	mA	6a

SOFT START

I_{5so}	Source Current	$V_6 = 0$ V,	$V_5 = 3$ V	80	130	180	µA	6b
I_{5si}	Sink Current	$V_6 = 3$ V,	$V_5 = 3$ V	40	70	140	µA	6b

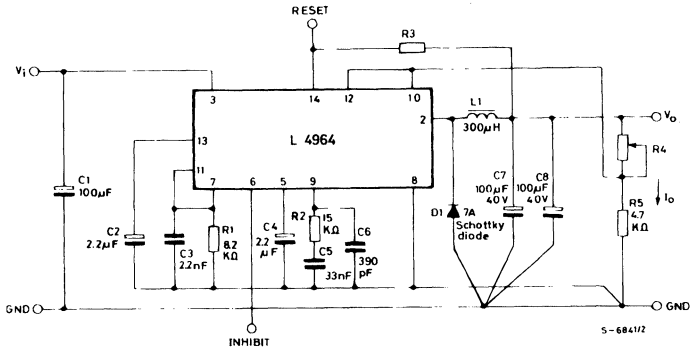
INHIBIT

V_{6L}	Low Input Voltage	$V_i = 9$ V to 36 V $V_7 = 0$ V	S1 : B S2 : B	– 0.3		0.8	V	6a
V_{6H}	High Input Voltage			2		5.5	V	6a
$-I_{6L}$	Input Current with Low Input Voltage	$V_i = 9$ V to 36 V $V_7 = 0$ V	$V_6 = 0.8$ V			20	µA	6a
$-I_{6H}$	Input Current with High Input Voltage	S1 : B S2 : B	$V_6 = 2$ V			10	µA	6a

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
ERROR AMPLIFIER							
V_{9H}	High Level Output Voltage	V_{10} = 4.7 V, I_9 = 100 µA, S1 : A, S2 : A	3.4			V	6c
V_{9L}	Low Level Output Voltage	V_{10} = 5.3 V, I_9 = 100 µA, S1 : A, S2 : E			0.6	V	6c
$I_{9\,si}$	Sink Output Current	V_{10} = 5.3 V, S1 : A, S2 : B	100	150		µA	6c
$-I_{9\,so}$	Source Output Current	V_{10} = 4.7 V, S1 : A, S2 : D	100	150		µA	6c
I_{10}	Input Bias Current	V_{10} = 5.2 V S1 : B		2	20	µA	6c
G_v	DC Open Loop Gain	V_9 = 1 V to 3 V, S1 : A, S2 : C	40	55		dB	6c
OSCILLATOR AND PWM COMPARATOR							
$-I_7$	Input Bias Current of PWM Comparator	V_7 = 0.5 V to 3.5 V			10	µA	6a
$-I_{11}$	Oscillator Source Current	V_{11} = 2 V, S1 : A, S2 : B	4		–	mA	6a
RESET							
V_{12R}	Rising Threshold Voltage	V_i = 9 V to 36 V, S1 : B, S2 : B,	V_{ref} –150mV	V_{ref} –100mV	V_{ref} –50mV	V	6d
V_{12F}	Falling Threshold Voltage		4.75	V_{ref} –150mV	V_{ref} –100mV	V	6d
V_{13D}	Delay Threshold Voltage	V_{12} = 5.3 V, S1 : A, S2 : B	4.3	4.5	4.7	V	6d
V_{13H}	Delay Threshold Voltage Hysteresis			100		mV	6d
V_{14S}	Output Saturation Volt.	I_{14} = 5 mA ; V_{12} = 4.7 V ; S1, S2 : B			0.4	V	6d
I_{12}	Input Bias Current	V_{12} = 0 V to V_{ref}, S1 : B, S2 : B		1	10	µA	6d
$-I_{13\,so}$	Delay Source Current	V_{13} = 3 V, S1 : A, S2 : B; V_{12} = 5.3 V	60	110	150	µA	6d
$I_{13\,si}$	Delay Sink Current	V_{13} = 3 V, S1 : A, S2 : B; V_{12} = 4.7 V	8			mA	6d
I_{14}	Output Leakage Current	V_i = 36 V, V_{12} = 5.3 V, S1 : B, S2 : A			100	µA	6d

Figure 4 : Dynamic Test Circuit.



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A
R = 500 mΩ

Core type : MAGNETICS 58930 - A2 MPP
N° turns : 43 Wire Gauge : 1 mm (18 AWG)

Figure 5 : PC. Board and Component Layout of the Circuit of Fig. 4 (1:1 scale).

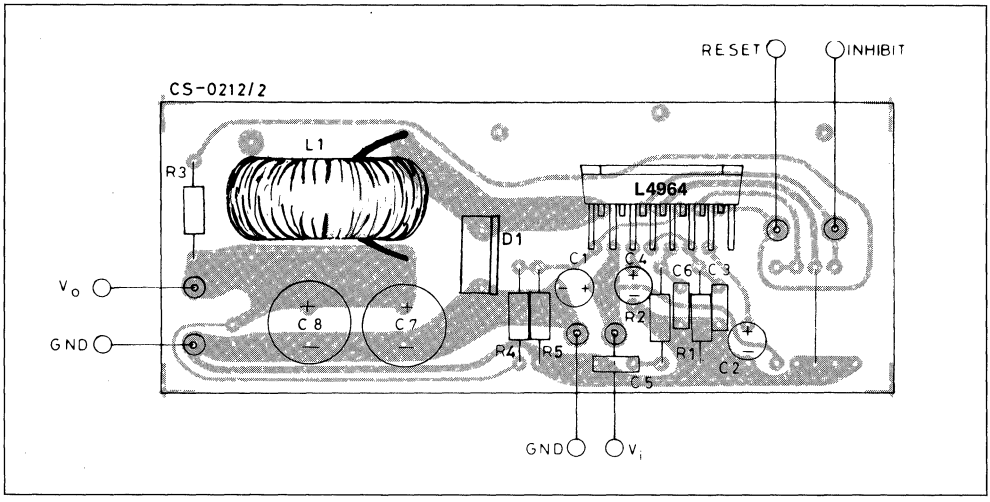


Figure 6 : DC Test Circuits.

Figure 6a.

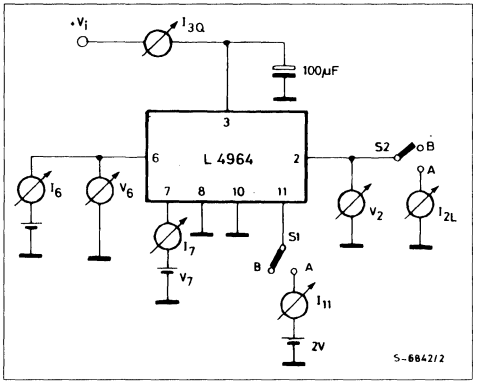


Figure 6b.

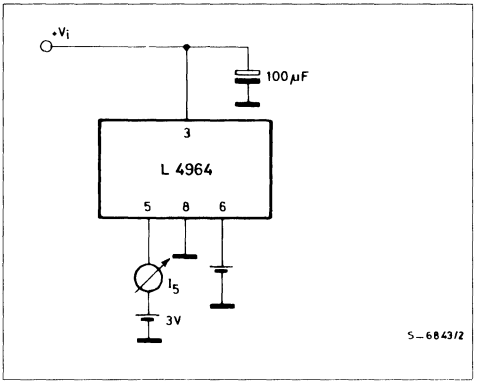


Figure 6c.

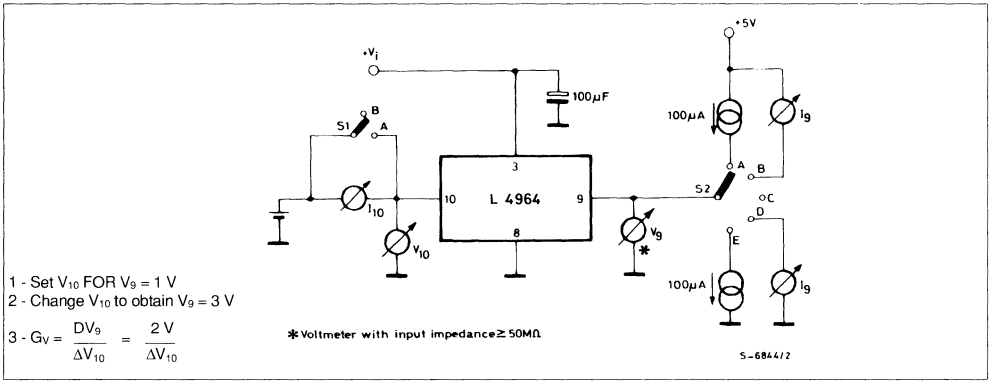


Figure 6d.

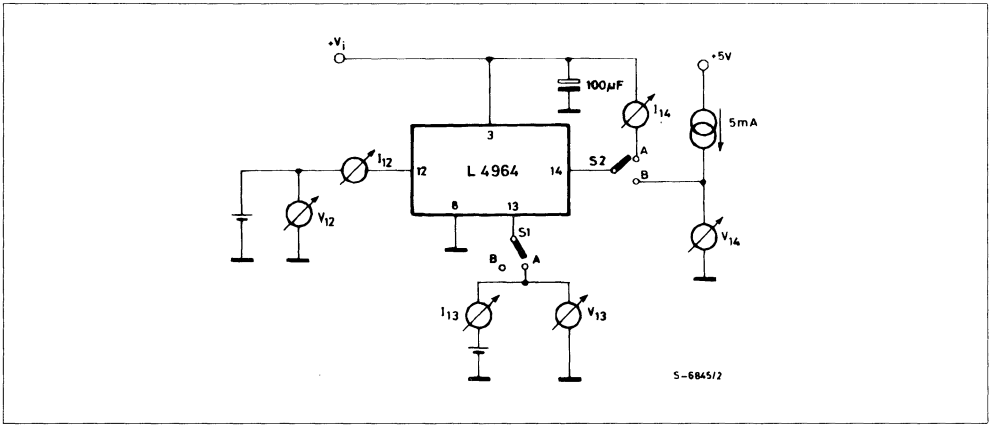


Figure 7 : Switching Frequency vs. R1 (see fig. 4).

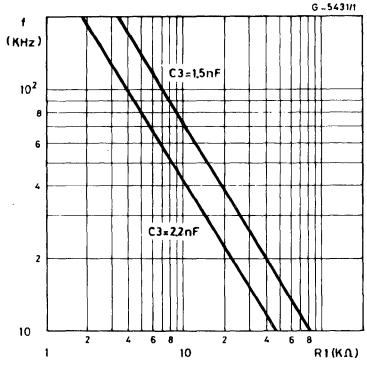


Figure 8 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

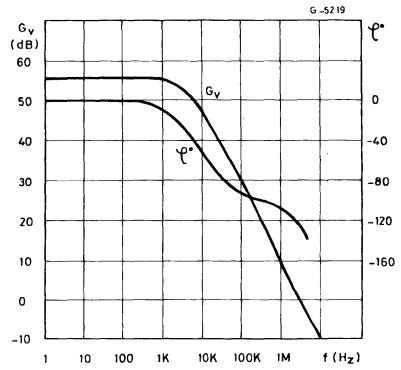


Figure 9 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

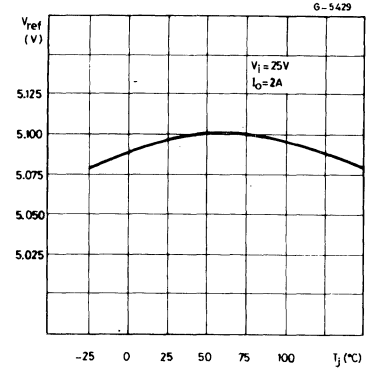


Figure 10 : Power Dissipation (L4964 only) vs. Input Voltage.

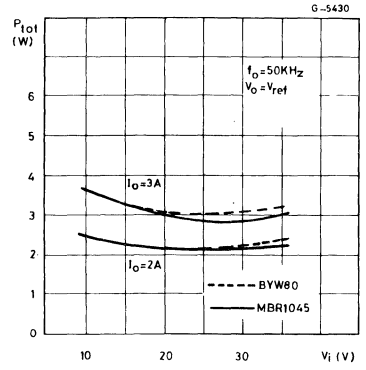


Figure 11 : Efficiency vs. Output Voltage.

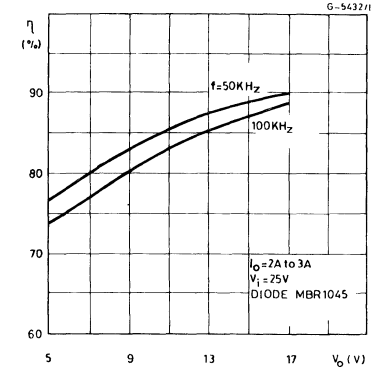
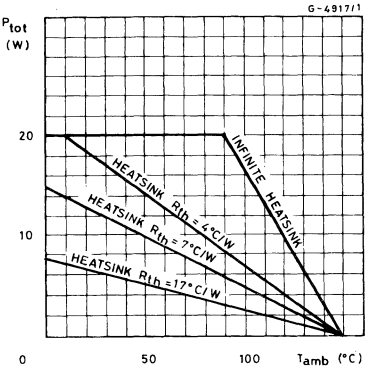


Figure 12 : Power Dissipation Derrating Curve.



APPLICATION INFORMATION

CHOOSING THE INDUCTOR AND CAPACITOR

The input and output capacitors of the L4964 must have a low ESR and low inductance at high current ripple.

Preferably, the inductor should be a toroidal type or wound on a Moly-Permalloy nucleus.Saturation must not occur at current levels below 1.5 times the current limiter level. MPP nuclei have very soft saturation characteristics.

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

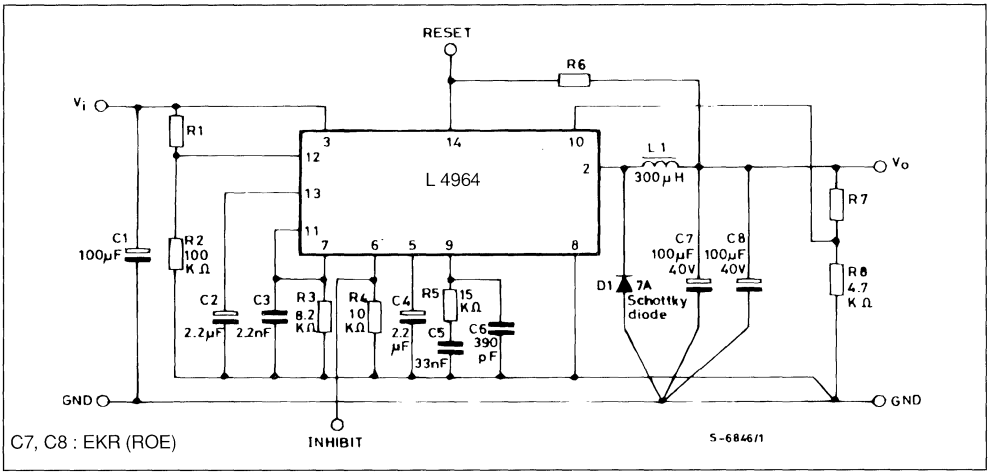
$$C = \frac{(V_i - V_o)\, V_o}{8L\, f^2\, \Delta V_o}$$

F = frequency

ΔI_L = Inductance current ripple

ΔV_o = Output ripple voltage

Figure 13 : Typical Application Circuit.



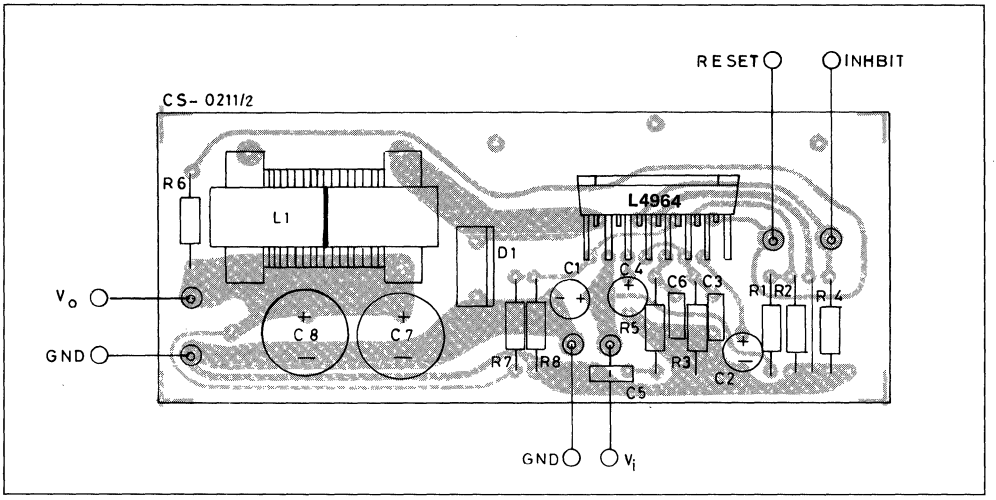
C7, C8 : EKR (ROE)

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	50	0.8 mm	0.7 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages		
V_O	R8	R7
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ

Figure 14 : P.C. Board and Component Layout of the Circuit of Fig. 13 (1:1 scale).



10 A SWITCHING REGULATOR

ADVANCE DATA

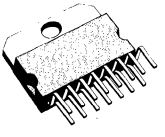
- 10 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 90 % DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1 V +/- 2 % ON CHIP REFERENCE
- RESET AND P. FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500 KHz
- THERMAL SHUTDOWN

DESCRIPTION

The L4970 is a stepdown monolithic power switching regulator delivering 10 A at a voltage variable from 5.1 to 40 V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500 KHz allows reduction in the size and cost of external filter components.

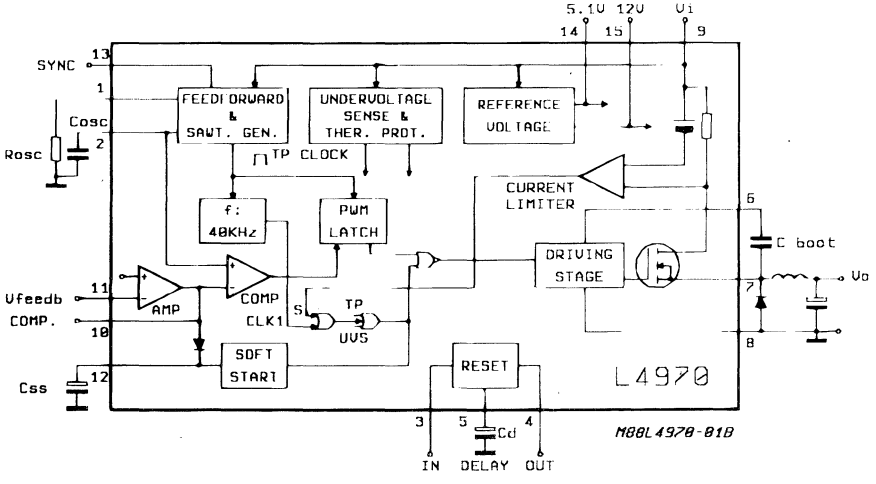
MultiPower BCD Technology



Multiwatt 15

ORDER CODE : L4970

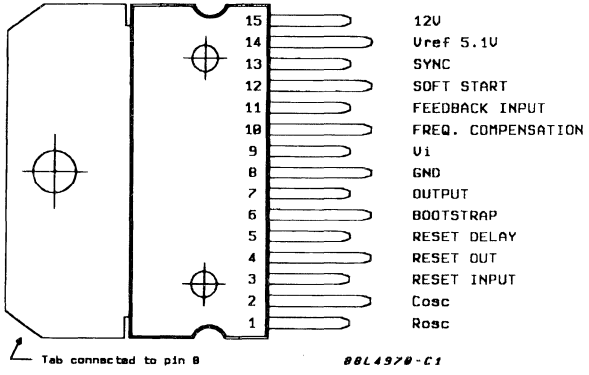
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1 µs f = 200 KHz	– 1 – 7	V V
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{11}, V_{12}	Input Voltage at Pins 3, 11, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{13}	Input Voltage at Pin 5, 10, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	10	mA
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120 °C	30	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top views)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1 V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external resistor when not used.
4	RESET OUT	Open Collector Reset/Power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output.
8	GROUND	Common Ground Terminal.
9	SUPPLY VOLTAGE	Unregulated Voltage Input.
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1 V operation ; it is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4970's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1 V_{ref} Device Reference Voltage.
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage.

Figure 1 : Feedforward Waveform.

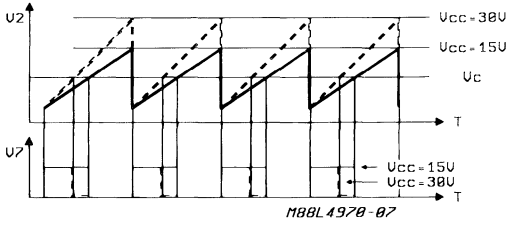


Figure 2 : Soft Start Function.

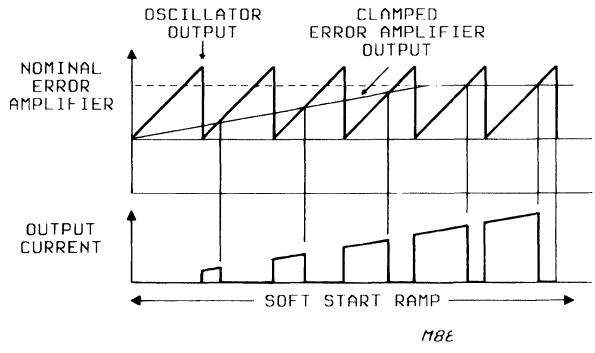


Figure 3 : Limiting Current Function.

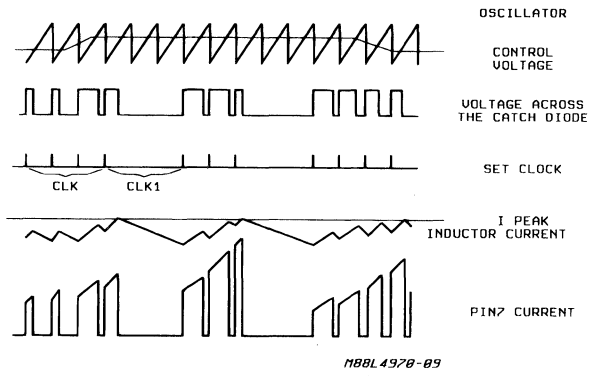
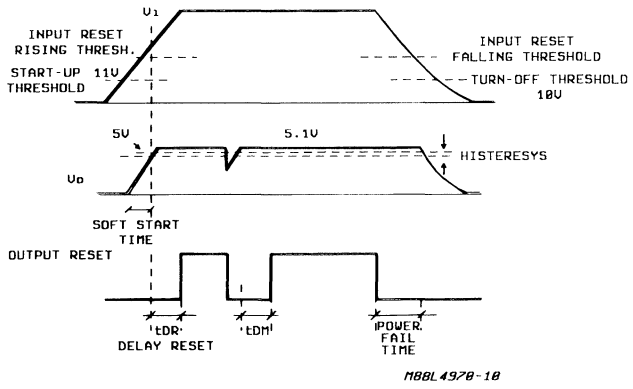
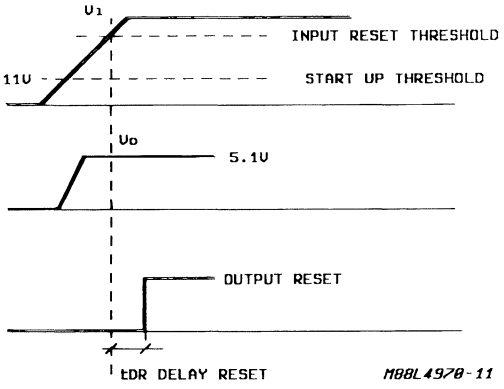


Figure 4 : Reset and Power Fall Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_j = 25 °C, V_i = 35 V, f = 200 kHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS							
V_i	Input Volt. Range (pin 9)	$V_o = V_{ref}$ to 40 V I_o = 10 A	15		50	V	5
V_o	Output Voltage	V_i = 15 V to 50 V I_o = 5 A ; $V_o = V_{ref}$	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15 V to 50 V I_o = 2 A ; $V_o = V_{ref}$		12	30	mV	5
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 3 A to 6 A I_o = 2 A to 10 A		10 20	30 50	mV mV	5
V_{REF} SECTION (pin 14)							
V_{REF}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{REF}	Line Regulation	V_i = 15 V to 50 V V_{12} = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3 mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff. Ref. Voltage	T_j = 0 °C to 125 °c		0.4		mV/C	7
I_{REF}	Short Circuit Curr. Limit	V_{REF} = 0		70		mA	7
V_{START} SECTION (pin 15)							
V_{ref}	Reference Voltage	P_{12} = 0 V	11.4	12	12.6	V	7
ΔV_{ref}	Line Regulation	P_{12} = 0 V ; V_i = 15 to 50 V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1 mA P_{12} = 0 V		50	200	mV	7
I_{ref}	Short Circuit Current Limit	P_{12} = 0 V ; P_{15} = 0 V		80		mA	7
V_d	Dropout Voltage between Pin 9 and 7	I_o = 5 A I_o = 10 A		0.55 1.1	0.8 1.6	V V	5
I_{7L}	Max Limiting Current	V_i = 15 V to 50 V $V_o = V_{ref}$ to 40 V	11	12.5	14	A	5
Efficiency		I_o = 5 A $V_o = V_{ref}$ V_o = 12 V	80	85 92		% %	5
		I_o = 10 A $V_o = V_{ref}$ V_o = 12 V	75	80 87		%	5

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SVR	Supply Voltage Ripple Reject.	V_i = 2 VRMS ; I_o = 5 A f = 100 Hz ; V_o = Vref	56	60		dB	5
f	Switching Freq.	R = 15 KΩ ; C = 2.2 nF	180	200	220	KHz	5
$\Delta f/_{\Delta Vi}$	Volt. Stability of Switching Freq.	V_i = 15 V to 45 V		2	6	%	5
$\Delta f/_{Tj}$	Temp. Stability of Switch. Freq.	T_j = 0 to 125 °C		1		%	5
f_{max}	Max. Operating Switch. Freq.	$V_o = V_{ref}$ I_o = 10 A	500			KHz	5

DC CHARACTERISTICS

V_{9on}	Turn–on Thresh.		10	11	12	V	7A
V_{9Hyst}	Turn–off Hyster.			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0 ; S1 = D ; S2 = C ; S4 = A		10	16	mA	7A
I_{9OQ}	Operating Quiescent Curr.	V_{12} = 0 f = 200 KHz		16	20	mA	7A
I_{7L}	Out Leak Current	V_i = 55 V ; S3 = A ; V_{12} = 0 V ; f = 200 KHz			2	mA	7A

SOFT START (pin 12)

I_{12}	Soft Start Source Current	V_{12} = 3 V ; V_{11} = 0 V	70	100	130	µA	7B
V_{12s}	Output Saturation Voltage	I_{12s} = 20 mA ; V_9 = 10 V			0.7	V	7B

ERROR AMPLIFIER

V_{10H}	High Level out Voltage	I_{10} = – 50µA ; S2 = A P_{11} = 0 V ; S1 = C	6			V	7C
V_{10L}	Low Level out Voltage	I_{10} = 50µA ; S2 = A P_{11} = 6 V ; S1 = C			0.7	V	7C
I_{11}	Input Bias Current	V_{11} = 5 ; S1 = B ; R_S = 10 K		2	10	uA	7C
VOS	Input off Voltage	P_{11} = Vos ; R_s = 50 Ω ; S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	P_{VCM} = 4 V ; R_S = 50 Ω ; S1 = A	60			dB	7C
SVR	Supply Volt. Rej.	15 < Vi < 50 V	60	80		dB	7C

RAMP GENERATOR (pin 2)

	Ramp Valley			1.5		V	7A
	Ramp Peak	V_i = 15 V V_i = 45 V		2.5 5.5		V V	7A
	MIn Ramp Current	S1 = A ; I1 = 100 µA		270	300	µA	7A
	Max Ramp Current	S1 = A ; I1 = 1 mA	2.4	2.7		mA	7A

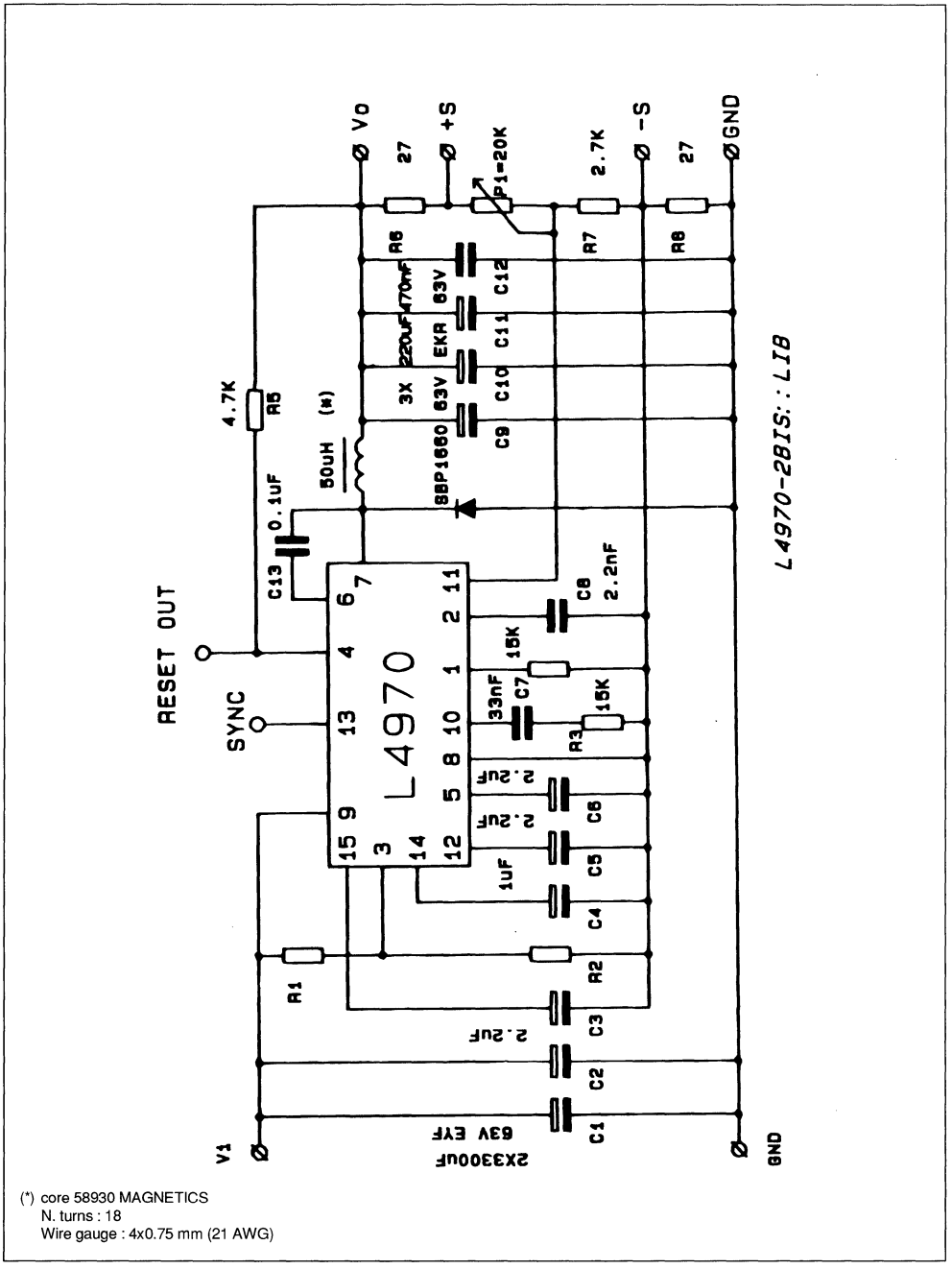
SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_i = 15 V to 50 V	− 0.3		0.9	V	
SYNC	High Input Voltage	V_{12} = 0	3.5		5.5	V	
$-I_{13L}$	Sync Input Current with Low Input Voltage	V_{13} = 0.9 V			0.4	mA	
$-I_{13H}$	Input Current with High Input Voltage	V_{13} = 3.5 V			1.5	mA	
SYNC	Delay			50		ns	
	Output Amplitude			5		V	
	Output Pulse Width			0.5		µsec.	

RESET AND P. FAIL FUNCTIONS

V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50 V S1 = B	Vref − 150	Vref − 100	Vref − 50	V mV	7D
	Hysteresis	S1 = B	80	100	120	mV	7D
V_{5H}	Delay High Threshold Voltage	S1 = B	5	5.1	5.2	V	7D
V_{5L}	Delay Low Threshold Voltage	S1 = B	1	1.1	1.2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3 V ; V_5 = 3 V S1 = A	40	55	70	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7 V ; V_5 = 3 V S1 = A	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15 mA ; S2 = B			0.4	V	7D
I_4	Output Leak Current	V_4 = 50 V ; S2 = A			100	µA	7D
V_{3R}	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit.



(*) core 58930 MAGNETICS
N. turns : 18
Wire gauge : 4x0.75 mm (21 AWG)

Figure 6 : Mockup of the Circuit of Fig. 5 (1.1 scale).

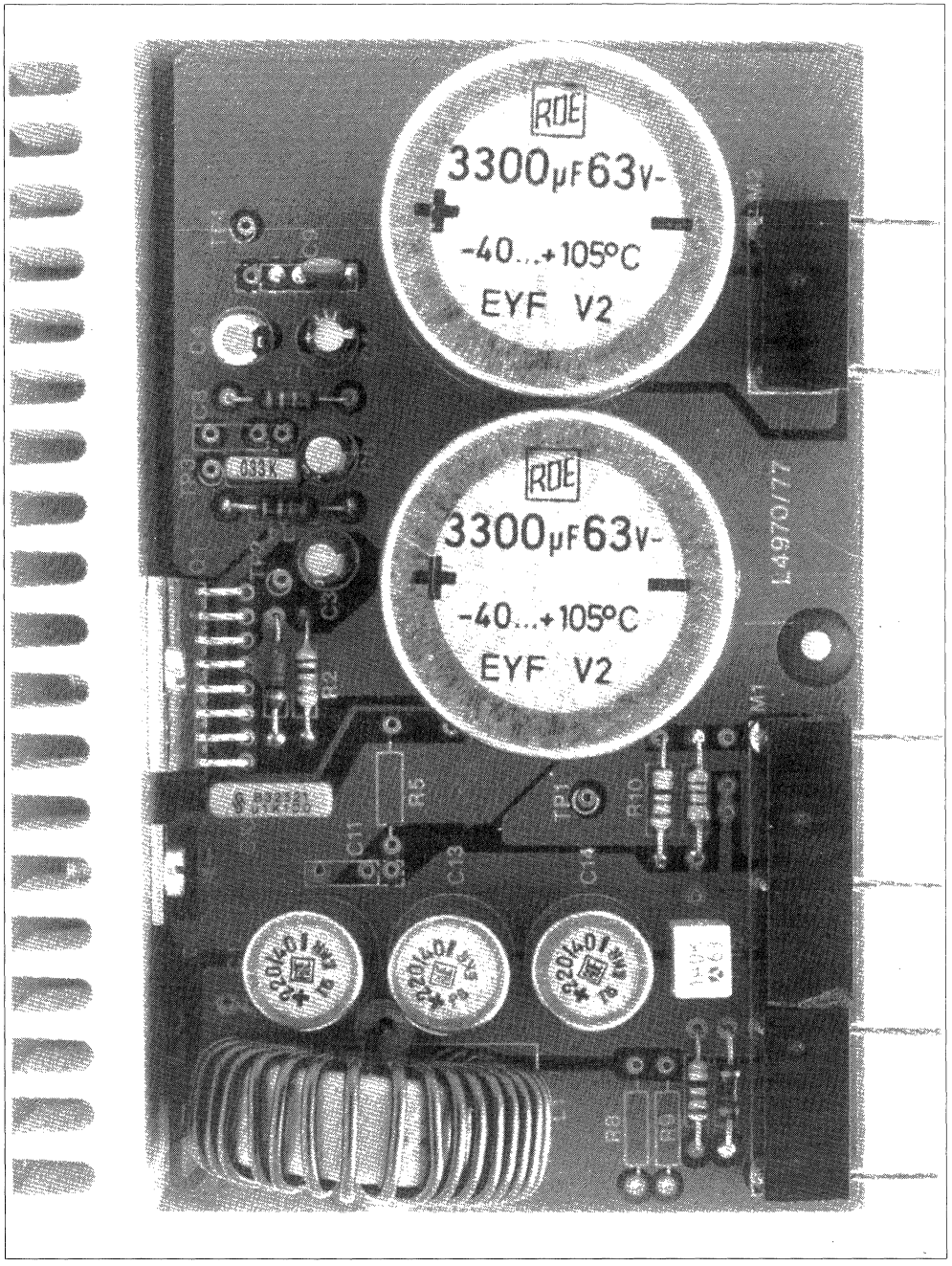


Figure 7 : DC Test Circuits.

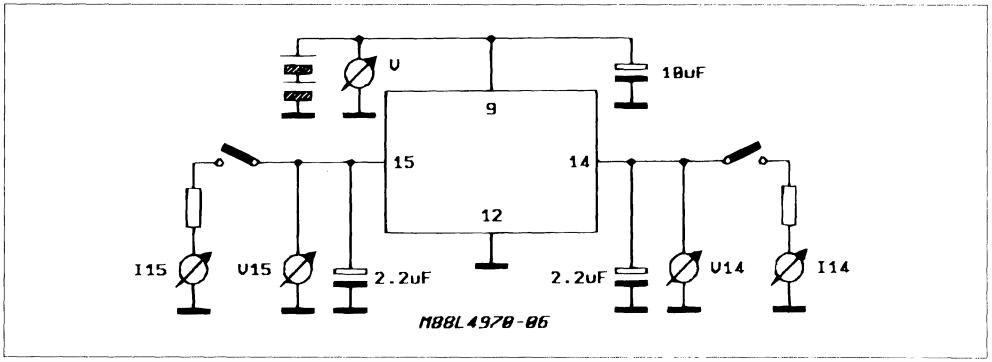


Figure 7A.

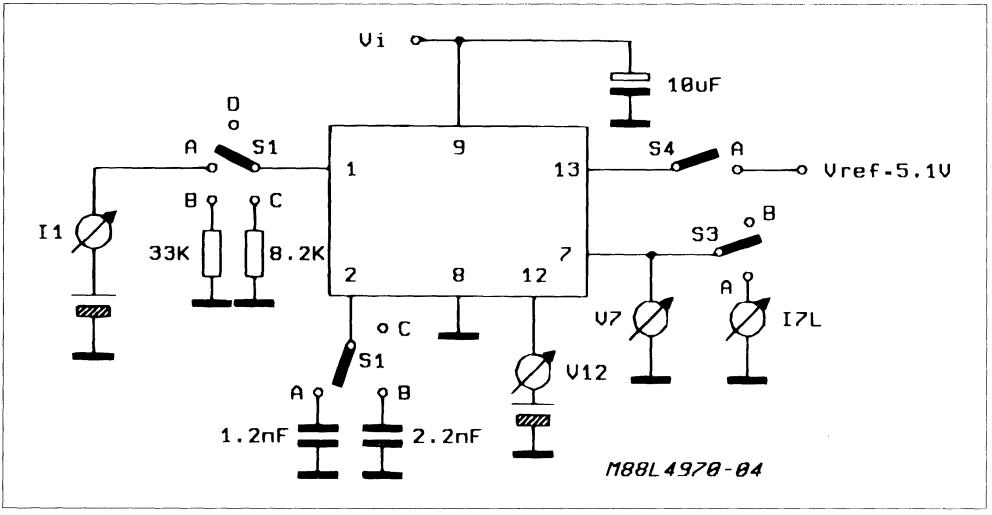


Figure 7B.

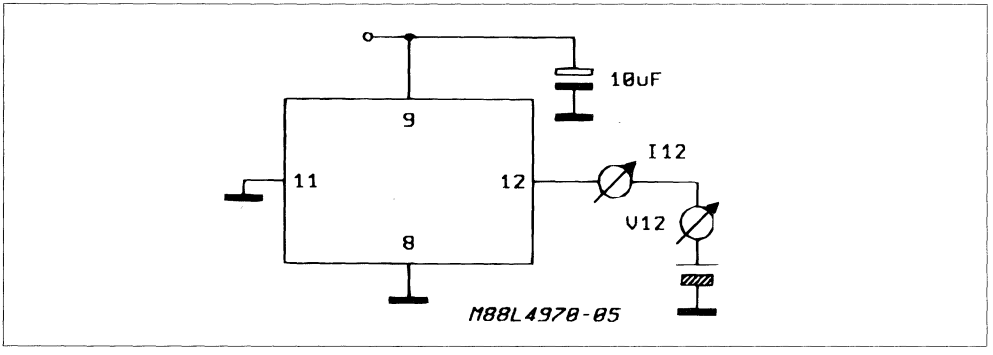


Figure 7C.

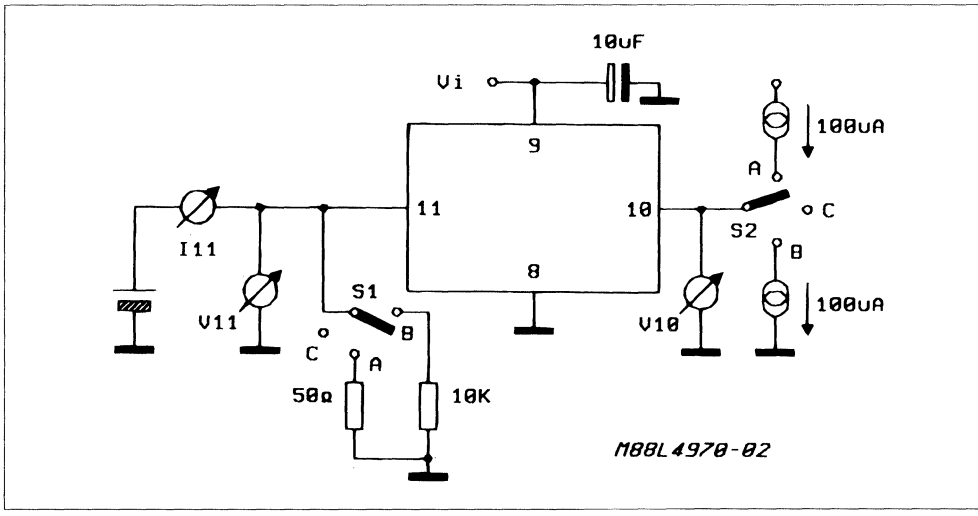


Figure 7D.

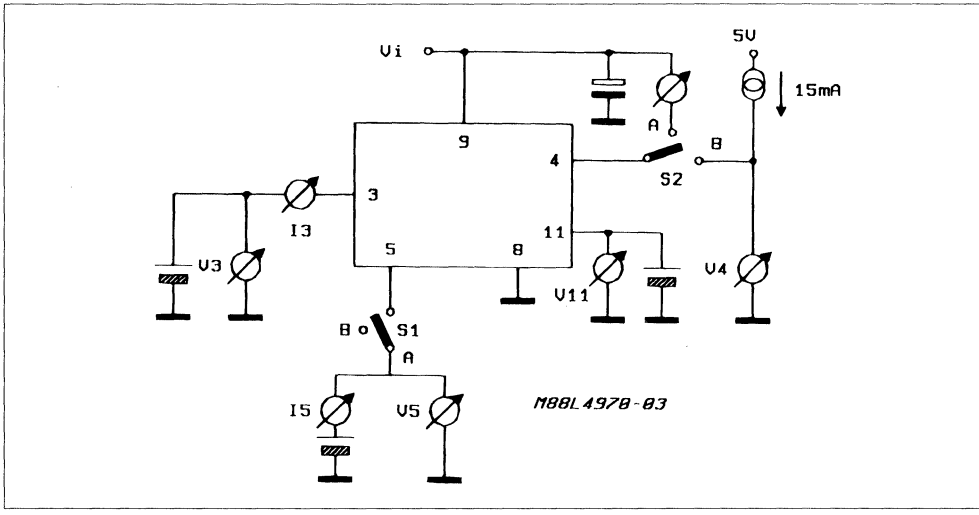


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0 % duty cycle - see fig. 7A).

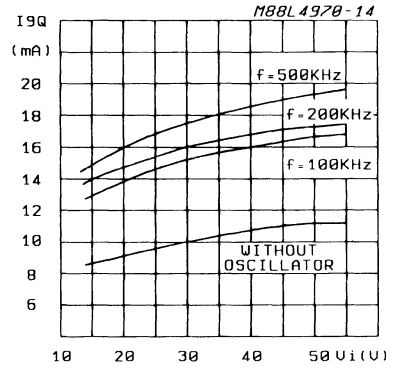


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % duty cycle).

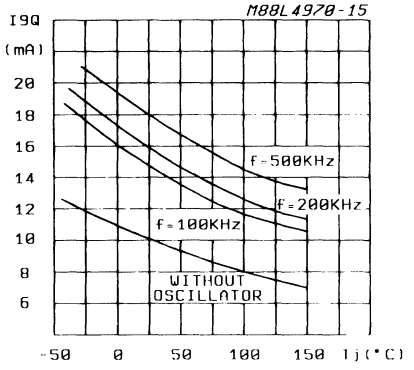


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

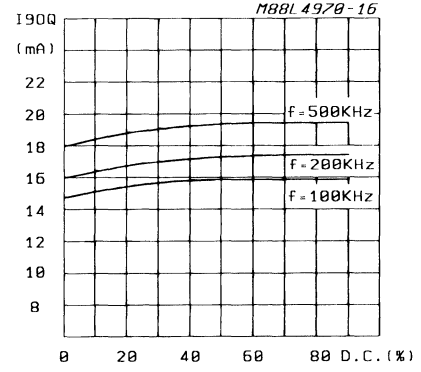


Figure 11 : Reference Voltage (pin 14) vs. V_i (see fig. 7).

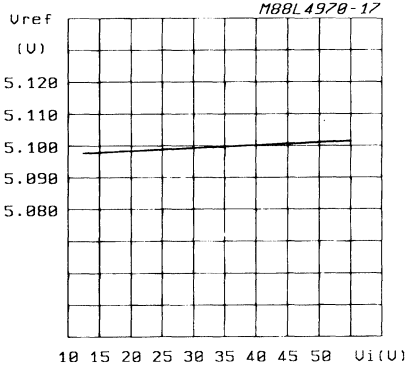


Figure 12 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

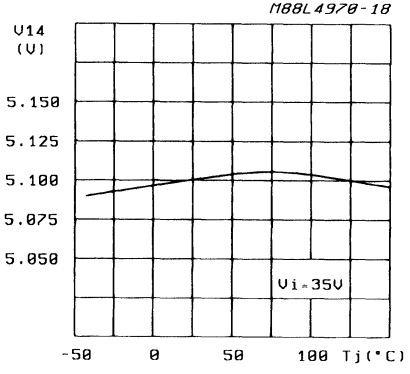


Figure 13 : Reference Voltage (pin 15) vs. V_i (see fig. 7).

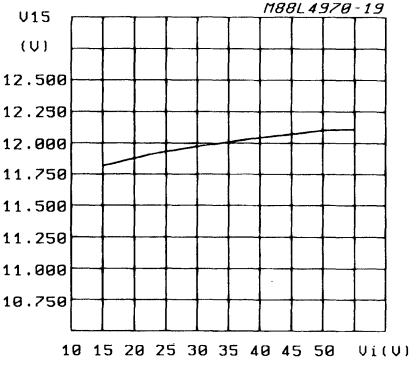


Figure 14 : Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7).

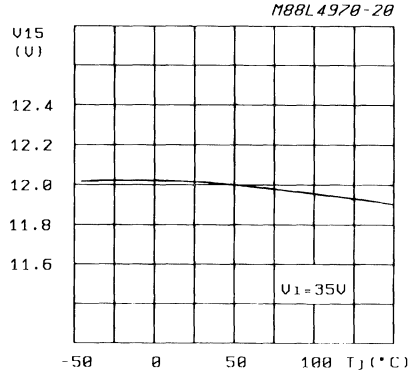


Figure 15 : Switching Frequency vs. Input Voltage (see fig. 5).

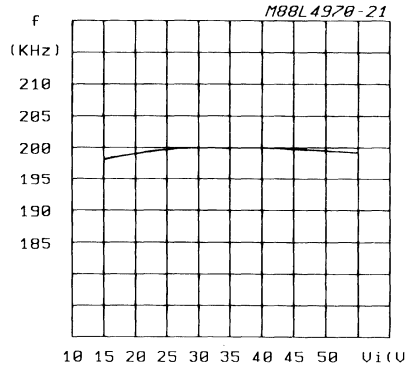


Figure 16 : Switching Frequency vs. Junction Temperature (see fig. 5).

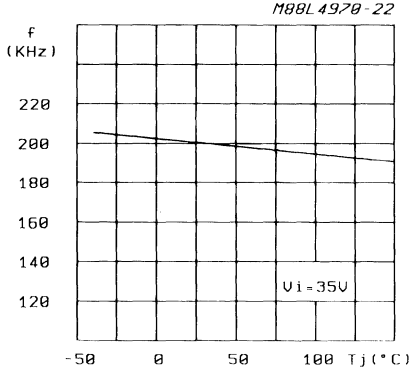


Figure 17 : Switching Frequency vs. R4 (see fig. 5).

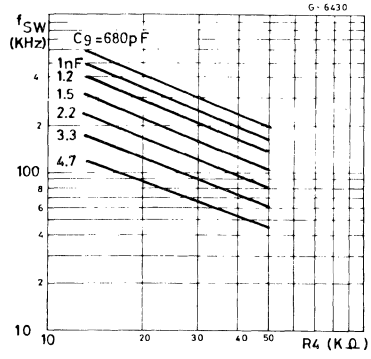


Figure 18 : Line Transient Response (see fig. 5).

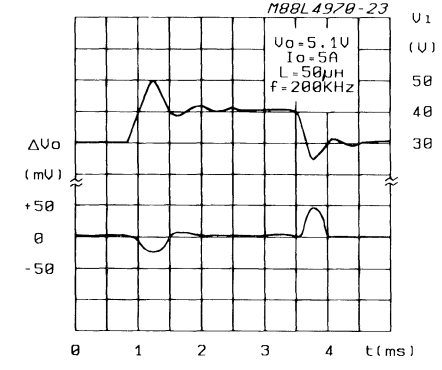


Figure 19 : Load Transient Response (see fig. 5).

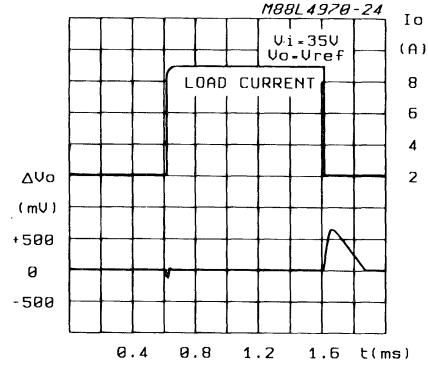


Figure 20 : Dropout Voltage between Pin 9 and Pin 7 vs. Current at Pin 7.

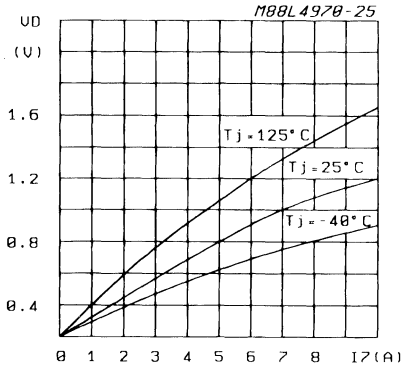


Figure 21 : Dropout Voltage between Pin 9 and Pin 7 vs. Junction Temperature.

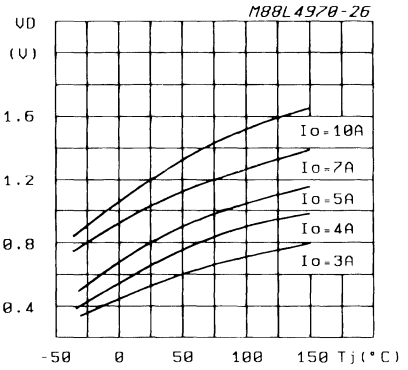


Figure 22 : Power Dissipation (device only) vs. Input Voltage.

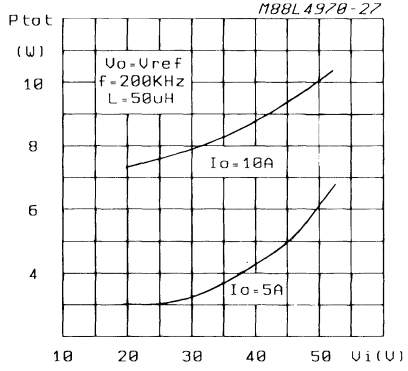


Figure 23 : Power Dissipation (device only) vs. Output Voltage.

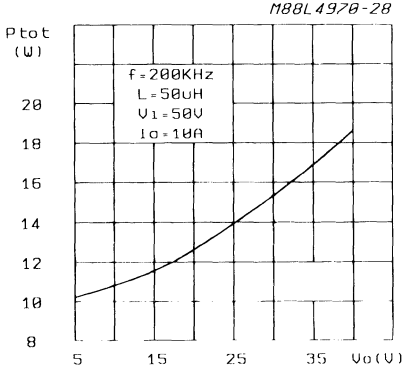


Figure 24 : Efficiency vs. Output Current.

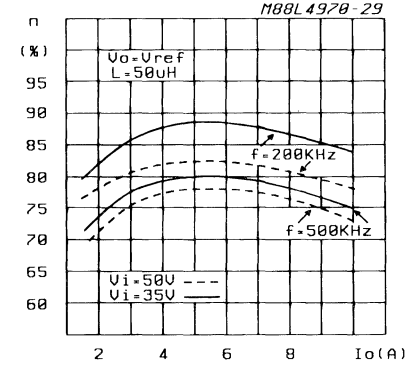


Figure 25 : Efficiency vs. Output Voltage.

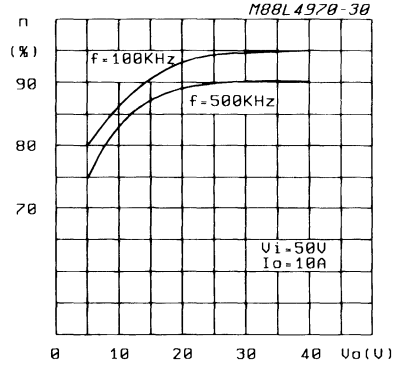


Figure 26 : Power Dissipation Derating Curve.

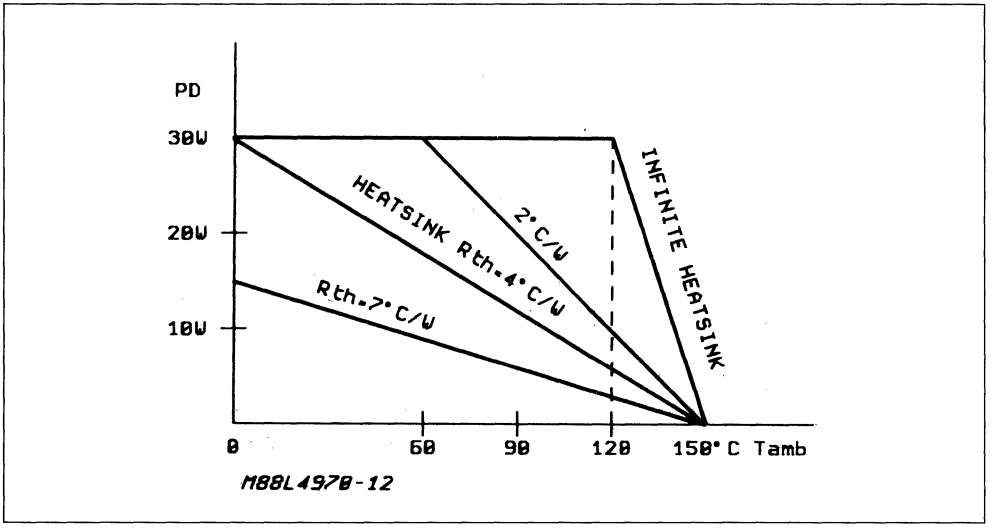
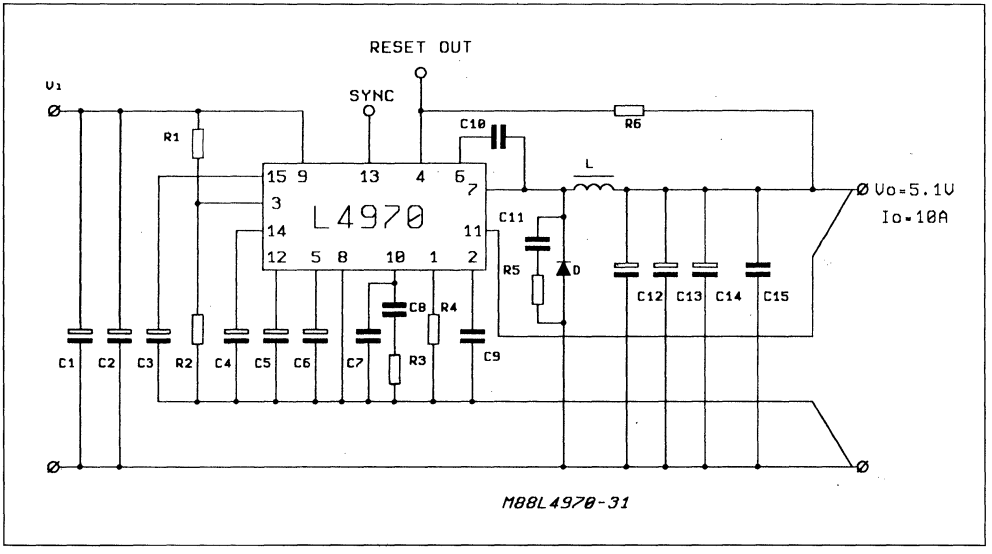


Figure 27 : 10 A - 5.1 V Application Circuit.



TYPICAL PERFORMANCES :

n = 83 % (V_i = 35 V ; V_o = V_{REF} ; I_o = 10 A ; f_{SW} = 200 KHz)

$V_{o\ RIPPLE}$ = 30 mV (at 10 A)

Line regulator = 5 mV (V_i = 15 to 50 V)

Load regulator = 15 mV (I_o = 2 to 10 A)

SOLENOID CONTROLLER

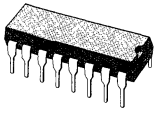
- DRIVES ONE OR TWO EXTERNAL DARLINGTONS
- DUAL AND SINGLE LEVEL CURRENT CONTROL
- SWITCHMODE CURRENT REGULATION
- ADJUSTABLE PEAK DURATION
- WIDE SUPPLY RANGE (4.75-46 V)
- TTL-COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION

DESCRIPTION

The L5832 Solenoid Controller is designed for use with one or two external darlington transistors in solenoid and relay driving applications.The device is controlled by two logic inputs and features switchmode regulation of the load current. A key feature of the L5832 is flexibility.

It can be used with a variety of darlingtons to match the requirements of the load and it allows both simple and two level current control Moreover, the drive waveshape can be adjusted by external components. Other features of the device include thermal shutdown, a supply voltage range of 4.75-46 V and TLL-compatible inputs.

The L5832 is supplied in a 12 + 2 + 2 – lead Powerdip package which use the four center pins to conduct heat to the PC board copper.



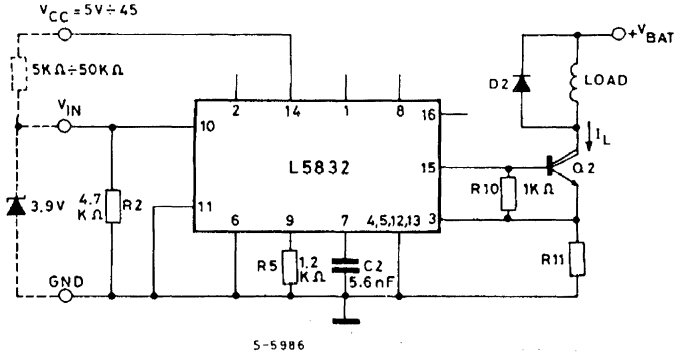
Powerdip
12 + 2 + 2

ORDER CODE : L5832

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	°C/W

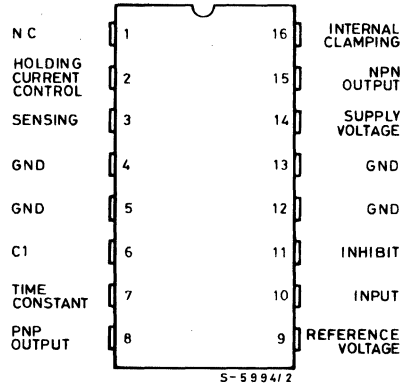
APPLICATION CIRCUIT USING ONE DARLINGTON



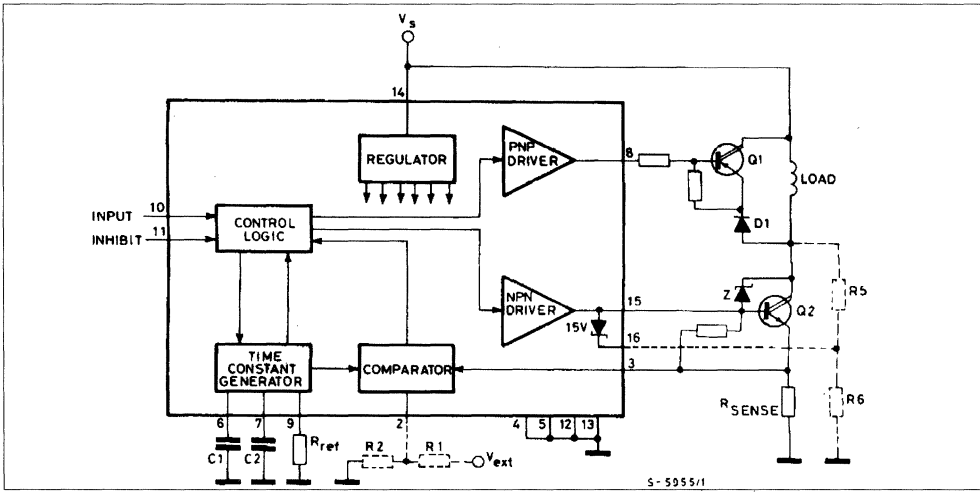
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	46	V
V_8	Positive Transient Voltage at Pin 8	60	V
V_{en}	Enable Input Voltage (pin 11)	7	V
V_I	Input Voltage (pin 10)	7	V
V_R	External Reference Voltage (pin 2)	2	V
P_d	Power Dissipation (T_{case} = 80 °C)	5	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

CONNECTION DIAGRAM



BLOCK DIAGRAM



PIN FUNCTIONS

N°	Name	Function
1	NC	Not Connected. Must be left open circuit.
2	HOLDING CURRENT CONTROL	A voltage applied to this pin sets the holding current level. If left open circuit an internal 75 mV reference is used and $I_h = I_p/6$.
3	SENSING	Connection for Load Current Sense Resistor. Value sets the maximum load current. $I_p = 0.45/R_s$.
4	GROUND	Ground Connection. With pins 5, 12 and 13 conducts heat to printed circuit board copper.
5	GROUND	See Pin 4
6	C1	A capacitor connected between this pin and ground sets the duration of the current peak (t2 in fig.3). If left open, the switchmode control of the peak is suppressed. If grounded, the current does not fall to the holding level.
7	DISCHARGE TIME CONSTANT	A capacitor connected between this pin and ground sets the duration of t_{off} (fig.3). If grounded, switchmode control is suppressed.
8	PNP DRIVING OUTPUT	Current Drive Output for External PNP Darlington (for recirculation). $I = 35\ I_{ref}$.
9	REFERENCE VOLTAGE	A resistor connected between this pin and ground sets the internal current reference, I_{ref}. The recommended value is 1.2kΩ, giving $I_{Ref} = 1$ mA.
10	INPUT	TTL - Compatible Input. A high level on this pin activates the output, driving the load.
11	INHIBIT	TTL - Compatible Inhibit Input. A high level on this input disables the output stages and logic circuitry, irrespective of the state of pin 10.
12	GROUND	See Pin 4
13	GROUND	See Pin 4
14	SUPPLY VOLTAGE	Supply Voltage Input
15	NPN DRIVING OUTPUT	Current Drive for External NPN Darlington (in series with the load). $I = 100\ I_{ref}$.
16	INTERNAL CLAMPING	Internal Zener Clamp Avaible for Fast Turnoff.

ELECTRICAL CHARACTERISTICS ($V_{S\,(pin\,14)}$ = 14 V , T_{amb} = 25 °C, R_{ref} = 1.2 KΩ, unless otherwise specified. Refer to Fig.2)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage (pin 14)			4.75		46	V
I_S	Quiescent Current (pin 14)	$V_{pin\,10} = V_{pin\,11}$ = Low State			21	40	mA
V_{in}	Input Voltage (pin 10)	Low State				0.8	V
V_{en}	Enable Input Voltage (pin 11)	High State		2.4			V
I_{in}	Input Current (pin 10)	Low State				100	µA
I_{en}	Enable Input Current (pin 11)	High State				10	µA
V_{ref}	Internal Reference Voltage (pin 9)			1.2	1.25	1.3	V
I_{ref}	Reference Current (pin 9)	$I_{ref} = V_{ref}/R_{ref}$ R_{ref} = 1.2 KΩ				1 300	µA
I_{pd}	Peak Duration Control Current (pin 6)	$I_{pd} = I_{ref}/8$		110	130	180	µA
t_{pd}	Peak Duration Time (pin 6)	$t_{pd} = C1\ V_{Th}/I_{pd}$ V_{th} = 1.4V C_1 = 4.7 nF			500		µs
I_{od}	Off Duration Control Current (pin 7)	$I_{od} = I_{ref}$ / 8		110	130	180	µA
t_{off}	Off Duration Time (pin 7)	$t_{od} = C2\ V_{th}/I_{od}$ V_{th} = 1.4V C2 = 4.7 nF			50		µs
I_{d1}	NPN Driving Current (pin 15)	$I_{d1} = 100\ I_{ref}$ (only present during charging phase)		80	100	130	mA
I_{d2}	PNP Driving Current (pin 8)	$I_{d2} = 35\ I_{ref}$		28	35	48	mA
I_p	Peak Current (emitter of NPN Darlington)	I_p = 450 mV/R_{sens} R_{sens} = 0.1 Ω		4.2	4.5	4.8	A
V_h	Holding Current Control Voltage	$V_h = R_{sens}\ I_h$ I_h = Emitter Current of NPN Darlington	Pin 2 Floating	70	75	85	mV
			Pin 2 Externally Biased			2	V
R_{in}	Holding Current Control Input Impedance (Pin 2)			100	150	200	Ω
r	Peak to Hold Current Ratio	Pin 2 Floating		5.8	6	6.2	
			Pin 6 Shorted	0.97	1	1.03	
I_B	Sense Input Bias Current (Pin 3)					100	µA
V_{clamp}	Internal Clamping (Pin 16 to 15)	I = 200 µA		14	16	18	V
V_{dt}	Dump Protection Threshold Voltage (Pin 1)			28	32	34	V
R_{dt}	Dump Protection Threshold Input Impedance (Pin 1)			22	32	42	KΩ
	Thermal Drift of Reference Voltage				0.5		mV/°C

APPLICATION INFORMATION

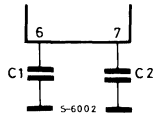
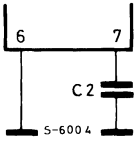
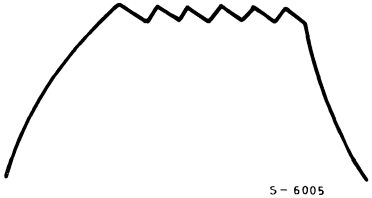
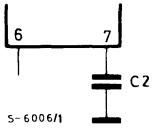
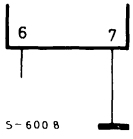
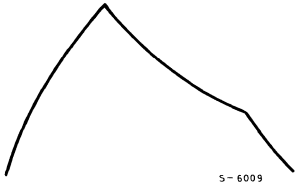
The L5832 solenoid controller is intended for use with one or two external darlington transistors to drive inductive loads such as solenoids, relays, electric valves and DC motors.

Controlled by a logic input and an inhibit input (both TTL compatible), the device drives the external darlington (s) to produce a load current waveform as shown in figure 3. This basic waveform shows that the device produces an initial current peak followed by a lower holding current. Both the peak and holding current levels are regulated by the L5832's switchmode circuitry .

The duration of the peak, the peak current level and holding current level can all be adjusted by external components.

Moreover, by omitting C1, C2 or both it is possible to realize single-level current control, a transitory peak followed by a regulated holding current or a simple peak (figure 1).

Figure 1 : Components Connected to Pins 6 and 7 Determine the Load Current Waveshape.

COMPONENTS ON PINS 6 AND 7	LOAD CURRENT WAVEFORM
	
	
	
	

The peak current level I_p, is set by the sensing resistor, R_{sens}, and is found from :

$$I_p = \frac{0.45}{R_{sens}}$$

The holding current level, I_h, is set by a voltage applied to pin 2. If this pin is left open circuit an internal reference of 75 mV supervenes and the holding current is given by :

$$I_h = \frac{I_p}{6}$$

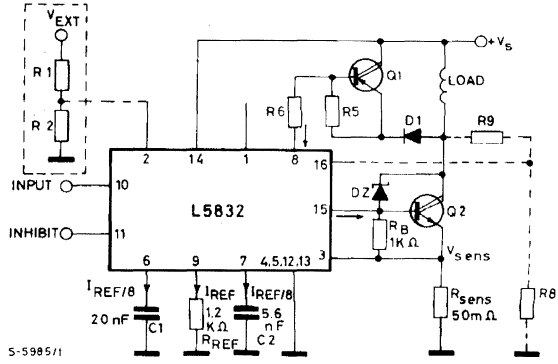
Alternatively, this level may be varied by adding a divider to pin 2 (R1, R2) and suitable values are found from :

$$\frac{I_{h\,max}}{I_p} = \frac{1}{0.45\ V}\left(\frac{R2\ //\ R_{in}}{R1 + R2\ //\ R_{in}}\ Vext + \frac{R2\ //\ R_{in}}{Rx = R2\ //\ R_{in}}\ Vx\right)$$

where Vx = 3V, Rx = 5850Ω. R_{in} = 150Ω (R_{in} of pin 2) and V_{ext} is the external voltage applied to the divider.

Figure 2 : Application Circuit Showing all the Optional Components. In Particular it Illustrates how the Holding Current Level is Adjusted Independently of the Peak Current (with R1, R2, V_{ext}) and how the Internal Zener Clamp is Connected. This Circuit Produces the Waveforms Shown in Fig.3.

I_o (A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
12	BDV64	BDV65



The drive currents for the two darlingtons and the waveform time constants are all defined by a reference current, I_{ref}, which is defined in turn by a resistor between pin 9 and ground.

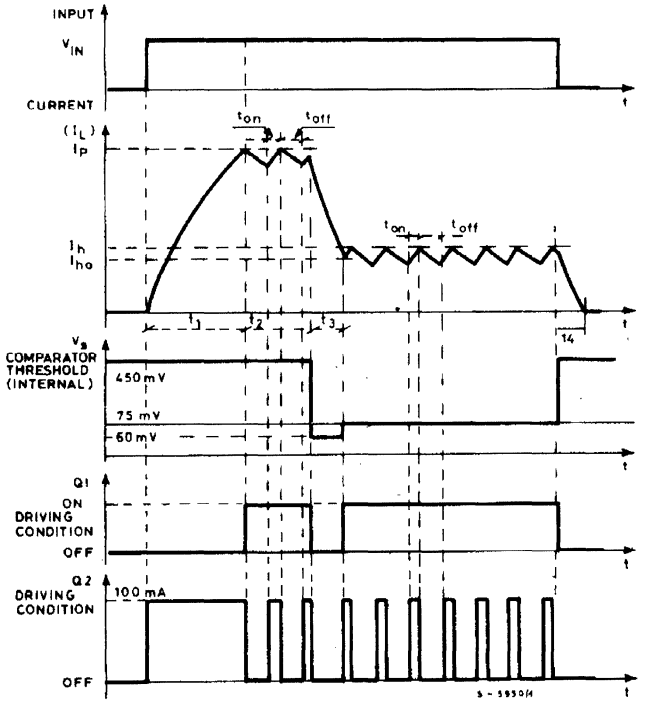
The recommended value for I_{ref} is 1 mA which is obtained with a 1.2 kΩ resistor. From I_{ref} the darlington drive currents are given by :

PNP : I = 35 I_{ref}
NPN : I = 100 I_{ref}

The duration of the high current level (t2 in figure 3) is set by a capacitor connected between pin 6 and ground. This capacitor, C1, is related to the duration, T, by :

$$C1 = \frac{I_{ref}\,T}{12}$$

Figure 3 : Waveforms of the Typical Application Circuit of Fig. 2.



The discharge time constant (t_{off} in figure 3) is set by a capacitor between pin 7 and ground and is found from :

$$t_{off} = \frac{12C2}{I_{ref}}$$

The t_{off} and t_{on} times are also related to the current ripple , ΔI :

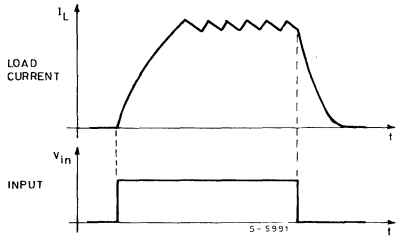
$$t_{off} = \frac{L\Delta I}{V_{off}} \quad \text{and } t_{on} = \frac{L\Delta I}{V_{on}}$$

where $V_{off} = V_{diode} + V_{CEQ1} + R_L I_L$
$V_{on} = V_S - V_{CEQ2} - V_{RS} - R_L I_L$
L = load inductance
R_L = load resistance
ΔI = load current ripple.

Note that t_{off} is the same for both the peak and holding currents.

Figure 4 : When Pin 6 in Grounded, as Shown here, the Load Current is Regulated at a Single Level.

I_o(A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65



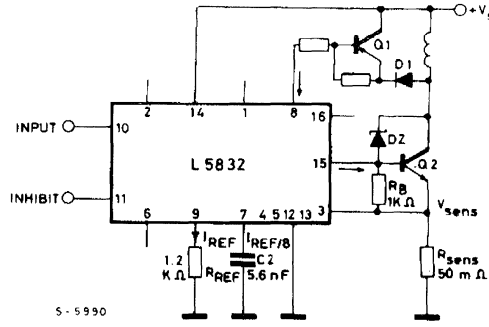
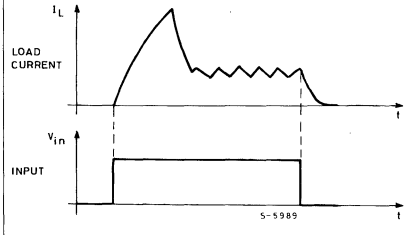


Figure 5 : In this Application Circuit, Pin 6 is Left Open to Give a Single Peak Followed by a Regulated Holding Current.

I_o(A)	Q1	Q2
4	BDX54	BDX53
8	BDX54	BDX53
16	BDW94	BDV65



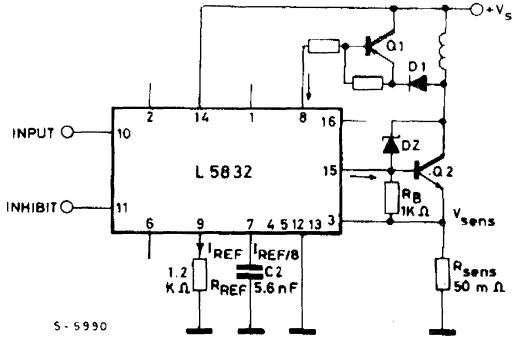
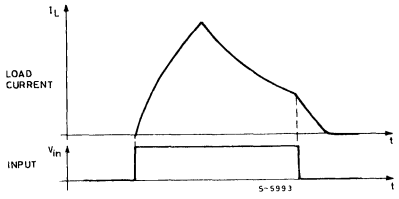
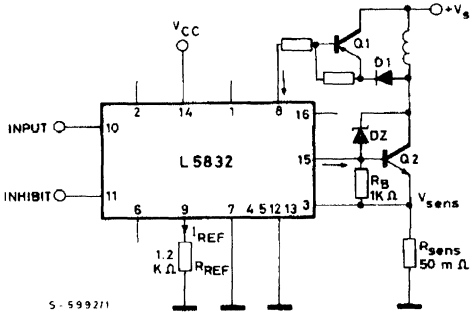


Figure 6 : Switchmode Control of the Current can be Suppressed Entirely by Leaving Pin 6 Open and Grounding Pin 7. The Peak Current is still Controlled.

I_o(A)	Q1	Q2
4	BDX54	BDX53
8	BDW94	BDW93
10	BDV64	BDV65





For fast turnoff an internal zener clamp is available on pin 16.
This is used with an external divider, R8 R9, as shown in figure 2. Suitable values can be found from :

$$V_{pin\,16} \cong 15V + V_{BEQ2} + VRsense$$

$$V_{CQ2} \cong V_{pin16} \cdot \frac{R9 + R8}{R8}$$

(V_{CQ2} is the voltage at the collector of Q2).

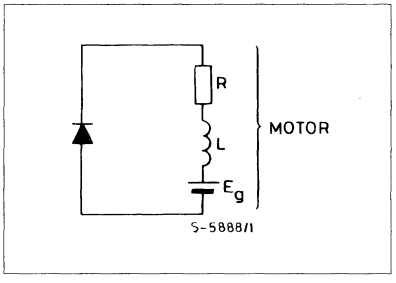
To ensure stability, a small capacitor (about 200 pF) must be connected between the base and collector of Q2 when pin 16 is used.

For the application circuit of figure 7 $t_{off} = 12C2/I_{ref}$, as before, and the current ripple is given by :

$$t_{off} = -\frac{L}{R} \cdot \frac{\ln(I_{LP} - \Delta I) \cdot R_L + V_L}{I_{LP} \cdot R_L + V_L}$$

where V_L is the voltage across the inductor during recirculation.

Note that if the load is a motor $V_L = Eg + V_D$.



Normally Δ I is a design parameter therefore C2 can be calculated directly from :

$$C2 = \frac{-I_{ref} \cdot L}{12\,R_L} \cdot \frac{\ln(I_{LP} - \Delta I)\,R_L + V_L}{I_{LP} \cdot R_L + V_L}$$

This application is particularly important because it allows the use of inductive loads with the lowest possible series resistance (compatible with constructional requirements) and therefore reduces notably the power dissipation.

For example, an electric valve driven from 24V which draws 2A has a series resistance of 12Ω and dissipates 48W . Using this circuit a valve with a 2Ω series resistance can be used and the power dissipation is :

$$Pd = R_L I_L^2 + V_D I_L(1-\delta) + V_{sat} \cdot I_L\,\delta + R_S I_L 2\delta$$

where R_L = resistance of valve = 2Ω
V_D = drop across diode, $V_D \cong 1V$
V_{sat} = saturation voltage of Q2, ≅ 1V
R_S = R11 = 220 mΩ
δ = duty cycle = 20 %

therefore :

$$Pd = 8 + 1.6 + 0.4 + 0.16 = 10.16W$$

This given two advantages : the size (and cost) of the valve is reduced and the drive current is reduced from 2A to about 0.4A.

The same consideration is also true for DC motors.

Figure 7 : Application Circuit Using Only one Darlington. The Resistor and Zener Shown Dotted Activate the Load when Power is Applied.

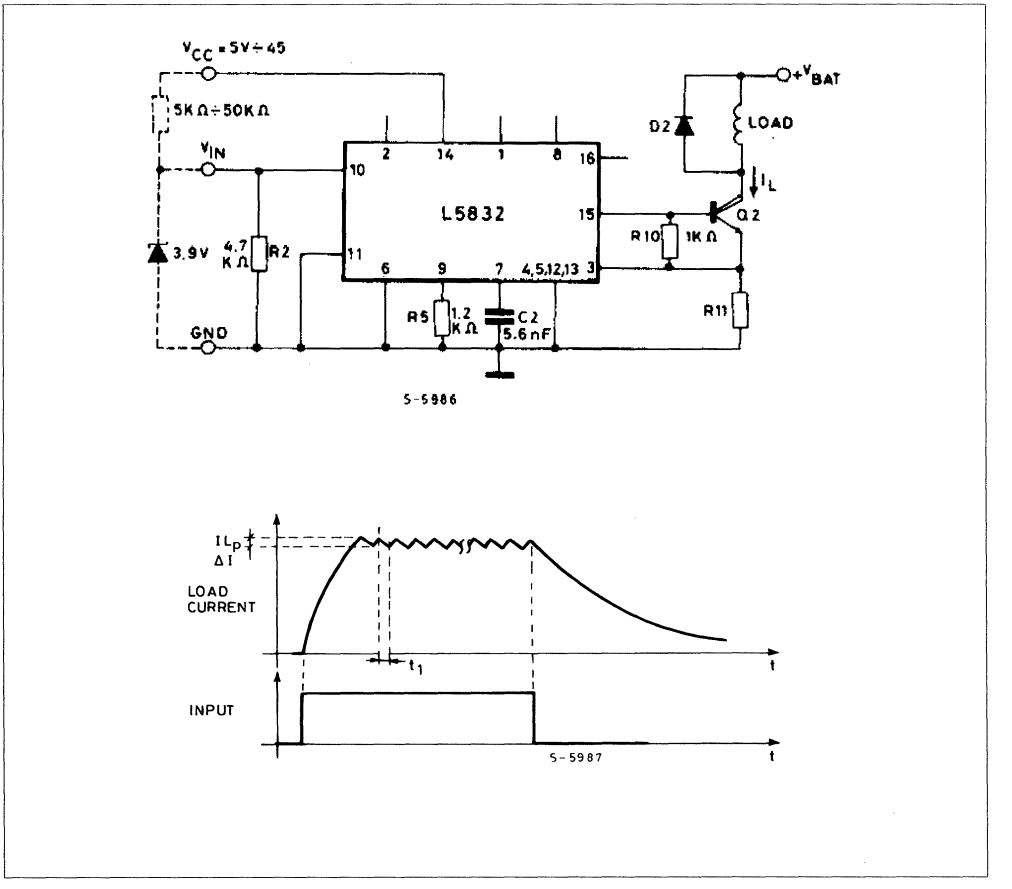


Figure 8: P.C. Board and Component Layout of the Circuit of Fig. 7 (1 : 1 Scale)

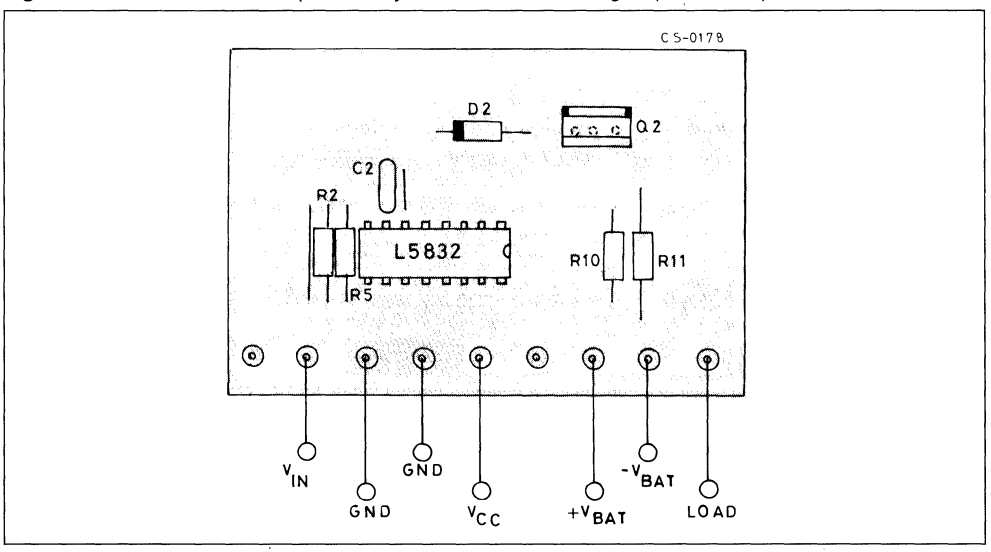
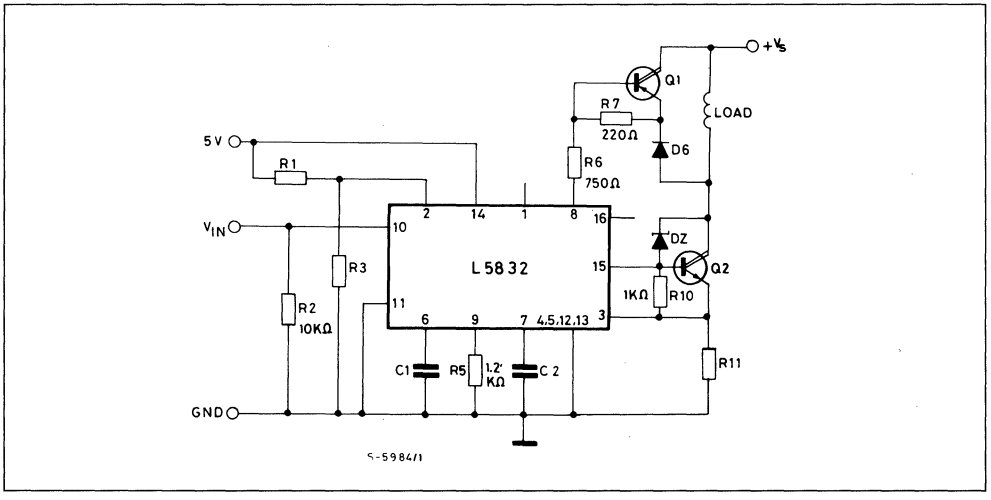


Figure 9: Application Circuit Showing how two Separate Supplies can be Used.



The application circuit of figure 9 is very similar to figure 2 except that it shows the use of two supplies-one for the control circuit, one for the power stage.

Chose R6 so that the voltage on pin 8 does not exceed 46V DC. This can be done simply bearing in mind that the pin 8 current is 35 I_{ref}.

R6 must not be too high if a very low supply voltage is used because:

$$V_{smin} = R6 \cdot 16 + 4.75$$

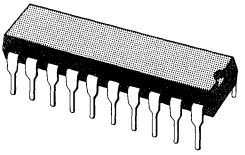
$$V_{smin} = 750 \cdot 35 \cdot 10^{-3} + 4.75 = 31V$$

The zener diode DZ can not exceed 62V because when Q1 is off and DZ triggered – the fast recirculation – the voltage on pin 8 may not exceed 60 V.

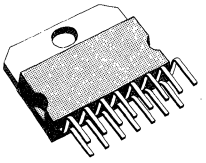
QUAD 100 V, DMOS SWITCH

- OUTPUT VOLTAGE TO 100 V
- 0.7 Ω $R_{DS(ON)}$
- SUPPLY VOLTAGE UP TO 60 V
- LOW INPUT CURRENT
- TTL/CMOS COMPATIBLE INPUTS
- HIGH SWITCHING FREQUENCY (200 KHz)

MultiPower BCD Technology



Powerdip 14 + 3 + 3



Multiwatt-15

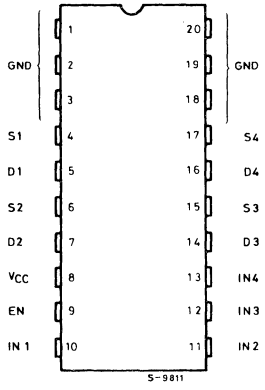
ORDER CODES : L6114 (Powerdip)
L6115 (Multiwatt-15)

DESCRIPTION

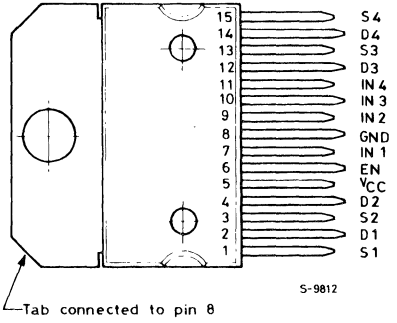
Realized with the Multipower-BCD mixed bipolar/CMOS/DMOS process, the L6114/15 monolithic quad DMOS switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL/CMOS compatible for direct connection to logic circuits. Each source is available for the insertion of the sense resistors in current control applications.

Two versions are available : the L6114 mounted in a Powerdip 14+3+3 package and the L6115 in a 15-lead Multiwatt package.

CONNECTION DIAGRAMS (top view)



L6114 (Powerdip)



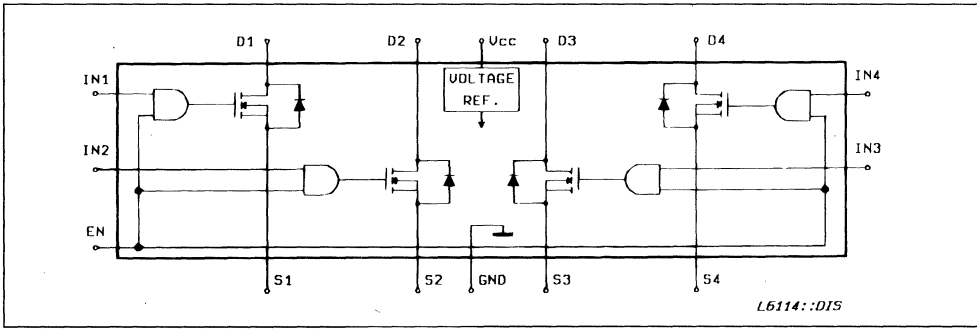
L6115 (Multiwatt-15)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit
V_{DS}	Drain-source Voltage			100	V
V_{CC}	Supply Voltage			60	V
I_D	Continuous Drain Current	@ T_{pins} = 90 °C	Powerdip	1.5	A
		@ T_{case} = 90 °C	Multiwatt –15	3	A
I_{DM} (*)	Pulsed Drain Current		Powerdip	5	A
			Multiwatt –15	8	A
I_{SD}	Continuous Source-drain Diode Current	@ T_{pins} = 90 °C	Powerdip	1.5	A
		@ T_{case} = 90 °C	Multiwatt –15	3	A
I_{SDM}	Pulsed Source Drain Diode Current		Powerdip	5	A
			Multiwatt –15	8	A
V_{IN}	Input Voltage			7	V
V_{EN}	Enable Voltage			7	V
V_S	Source Voltage			– 1 to + 4	V
P_{tot}	Total Power Dissipation	@ T_{pins} = 90 °C	Powerdip	4.3	W
		@ T_{case} = 90 °C	Multiwatt –15	20	W
		@ T_{amb} = 70 °C	Powerdip	1.3	W
		@ T_{amb} = 70 °C	Multiwatt –15	2.3	W
T_{stg}, T_j	Storage and Junction Temperature Range			– 40 to + 150	°C

(*) Pulse width ≤ 300 µs, duty cycle ≤ 10 %.
Note : I_D, I_{DM}, I_{SD}, I_{SDM} are given per channel.

BLOCK DIAGRAM



THERMAL DATA

			Powerdip	Multiwatt–15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	65 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_{CC} = 40 V, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			14		48	V
I_{CC}	Supply Current	All V_{IN} = H V_{EN} = Square Wave (200 KHz, 50 % DC)			9		mA
I_Q	Quiescent Current	V_{EN} = L			2	3	mA
BV_{DSS}	Drain Source Breakdown Voltage	I_D = 1 mA V_{EN} = L		100			V
I_{DSS}	Output Leakage Current	V_{EN} = L	V_{DS} = 100 V			1	mA
			V_{DS} = 80 V T_j = 125 °C		1		mA
$R_{DS\ (on)}$ (*)	Static Drain-source on Resistance	$V_{CC} \geq$ 14 V V_{EN}, V_{IN} = H	I_D = 1.5 A		0.7		Ω
$V_{IN\,L}$, $V_{EN\,L}$	Input Low Voltage			– 0.3		0.8	V
$V_{IN\,H}$, $V_{EN\,H}$	Input High Voltage			2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low Current	V_{IN}, V_{EN} = L				– 100	µA
$I_{IN\,H}$, $I_{EN\,H}$	Input High Current	V_{IN}, V_{EN} = H				10	µA
$t_{d\ (on)}$	Turn on Delay Time	I_D = 1.5 A See Test Circuit and Waveforms			300		ns
t_r	Rise Time				100		ns
$t_{d\ (off)}$	Turn off Delay Time				400		ns
t_f	Fall Time				100		ns
V_{SD} (*)	Source Drain Diode Forward Voltage	I_{SD} = 1.5 A	V_{EN} = L			1.5	V
$V_{SD\ (on)}$ (*)	Source Drain Forward Voltage	I_{SD} = 1.5 A V_{IN}, V_{EN} = H				1.2	V

(*) Pulse test : pulse width = 300 µs, duty cycle = 2 %.

SWITCHING TIMES RESISTIVE LOAD

Figure 1 : Test Circuit
(Pins x = Powerdip ; Pins (x) = Multiwatt).

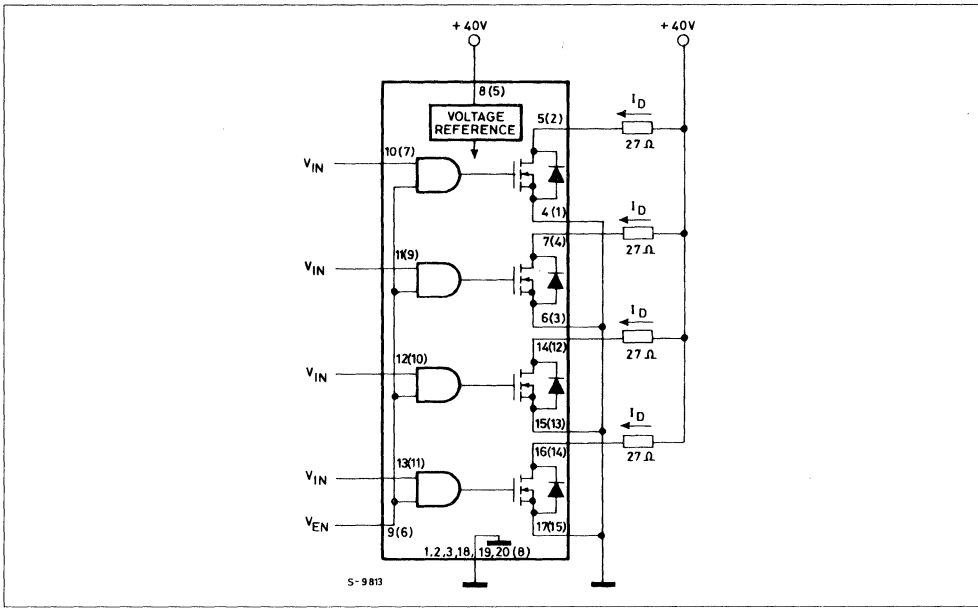
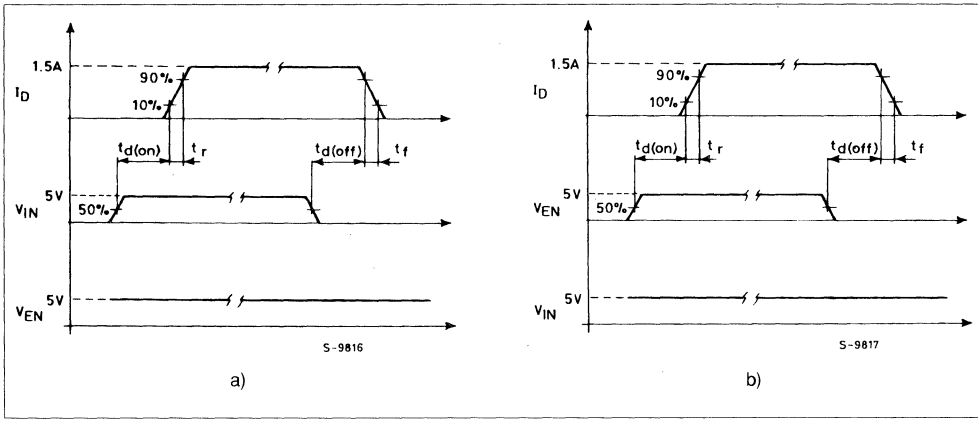
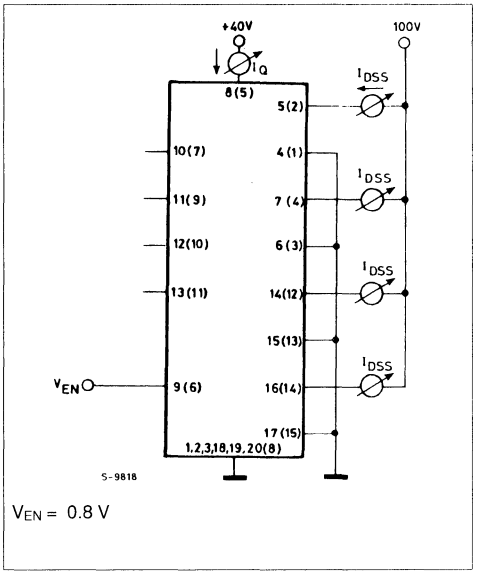


Figure 2 : Waveforms.



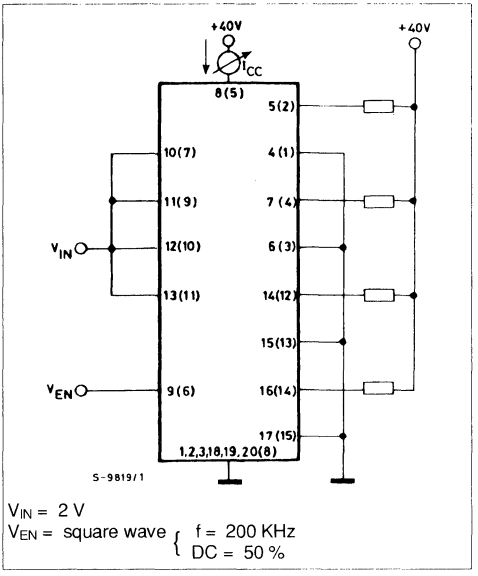
TEST CIRCUIT (Pins x = Powerdip ; Pins (x) = Multiwatt)

Figure 3 : Quiescent Current and Output Leakage Current..



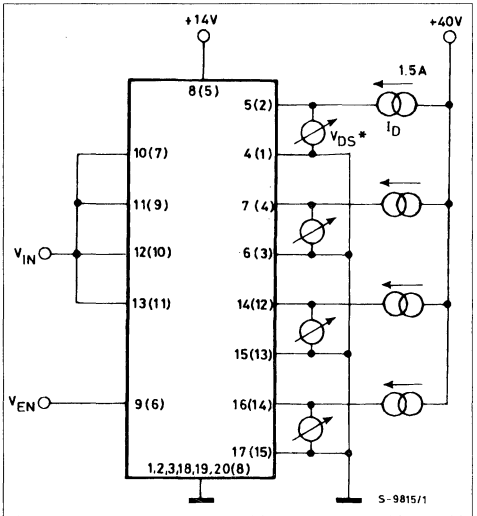
V_{EN} = 0.8 V

Figure 4 : Supply Current.



V_{IN} = 2 V
V_{EN} = square wave { f = 200 KHz, DC = 50 %

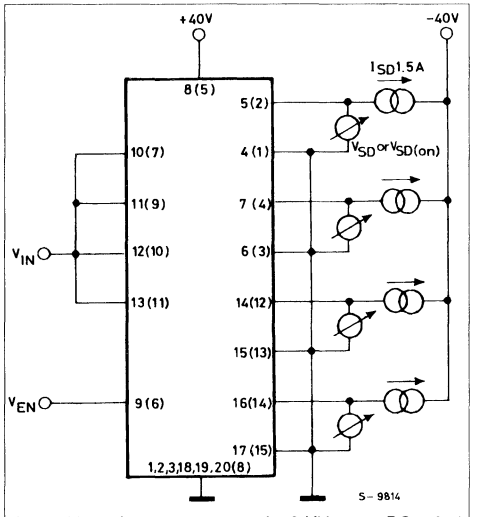
Figure 5 : $R_{DS\,(on)}$.



V_{CC} = 14 V, V_{IN} = 2 V, V_{EN} = 2V
I_D = square wave, f = 3 KHz DC = 2 %
(*) V_{DS} is taken during the time in which the I_D = 1.5 A

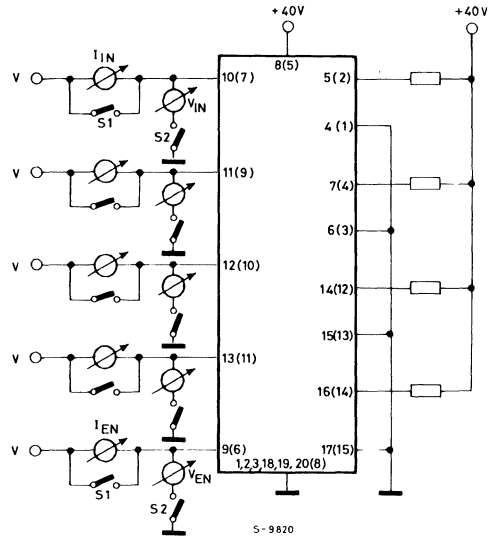
$$R_{DS} = \frac{V_{DS}}{1.5}$$

Figure 6 : Source-drain Diode Forward Voltage.



V_{IN} = 2 V, I_{SD} square wave, f = 3 KHz DC = 2 %
- Set V_{EN} = 0.8 V for V_{SD} (taken during the time in which I_{SD} = 1.5 A)
- Set V_{EN} = 2 V for $V_{SD\,(on)}$ (taken during the time in which I_{SD} = 1.5 A)

Figure 7 : Input Logic Levels



Set	V = 0.8 V	S1,S2 open	for	$I_{IN\,L}$ and $I_{EN\,L}$
Set	V = 0.8 V	S1,S2 close	for	$V_{IN\,L}$ and $V_{EN\,H}$
Set	V = 2 V	S1,S2 open	for	$I_{IN\,H}$ and $I_{EN\,H}$
Set	V = 2 V	S1,S2 close	for	$V_{IN\,H}$ and $V_{EN\,H}$

Figure 8 : Static Drain-source on Resistance.

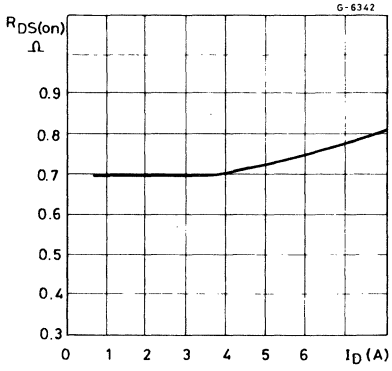


Figure 9 : Normalized Break-down Voltage vs. Temperature.

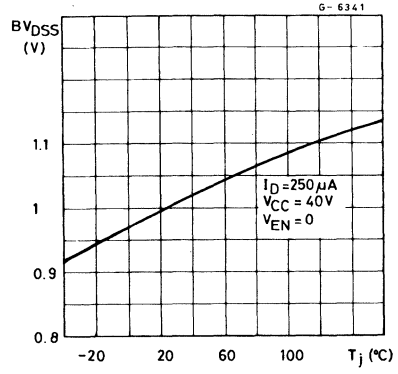


Figure 10 : Normalized on Resistance vs. Temperature.

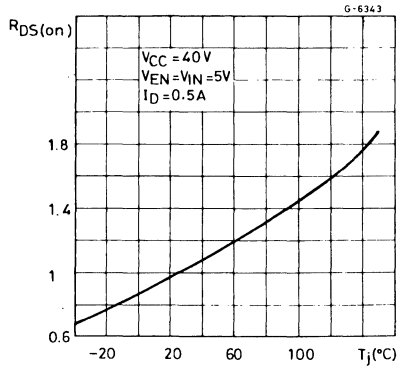


Figure 11 : Typical Source-drain Diode Forward Voltage.

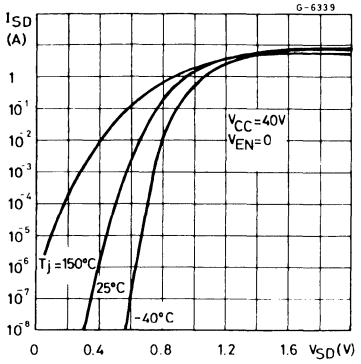
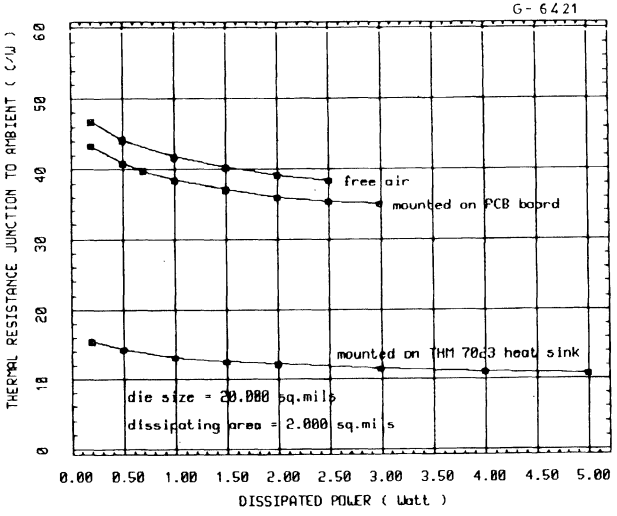


Figure 12 : $R_{th\ j\text{-}amb}$ vs. Dissipated Power(Multiwatt).



(*) $R_{th} \approx 9$ °C/W.

Figure 13 : Transient Thermal Resistance for Single Pulses (Multiwatt).

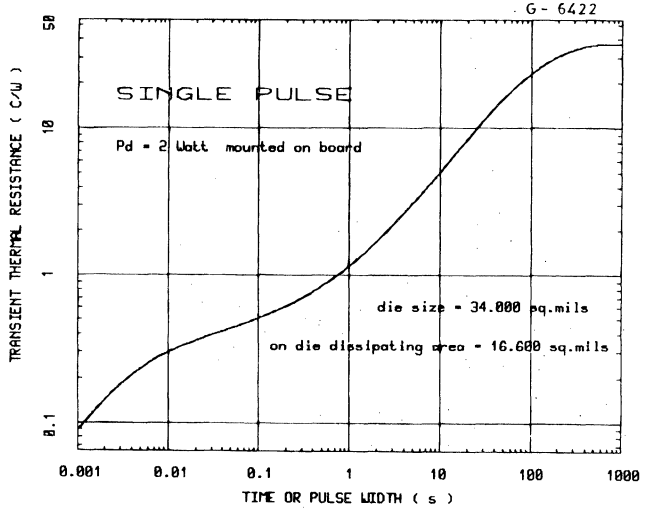
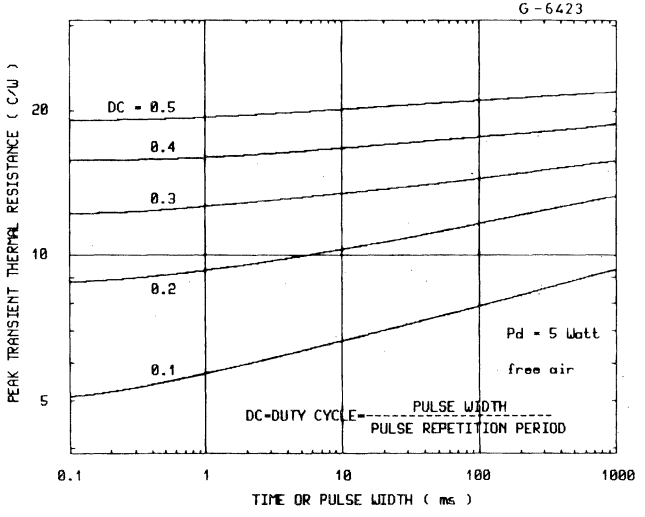


Figure 14 : Peak Transient Thermal Resistance vs.Pulse width and duty cycle (Multiwatt).



SGS-THOMSON MICROELECTRONICS

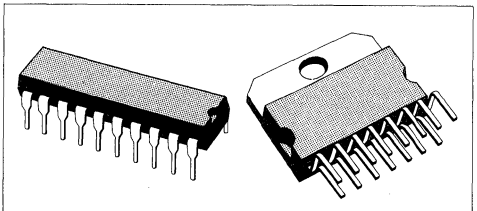
L6122
L6123

100 V DMOS SWITCHES

ADVANCE DATA

- OUTPUT VOLTAGE TO 100 V
- 0,5 Ω $R_{DS\ (on)}$
- SUPPLY VOLTAGE UP TO 60 V
- LOW INPUT CURRENT
- TTL/CMOS COMPATIBLE INPUTS
- HIGH SWITCHING FREQUENCY (200 KHz)

MultiPower BCD Technology



Powerdip 14+3+3 — **Multiwatt-15**

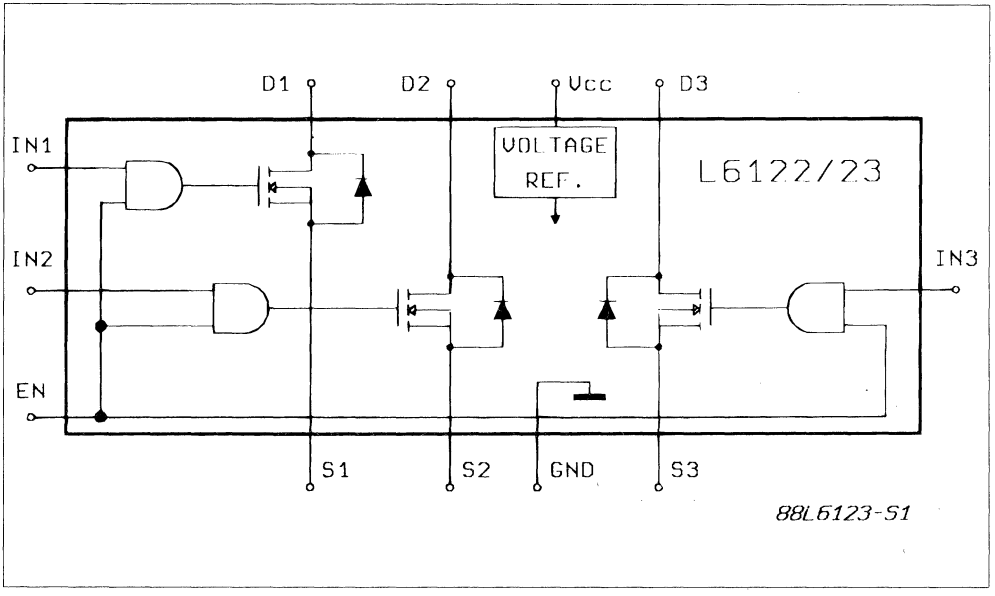
ORDER CODES : L6122, L6123

DESCRIPTION

Realized with the Multipower-BCD mixed bipolar/CMOS/DMOS process, the L6122/23 monolithic three DMOS switch is designed for high current, high voltage switching applications. Each of the three switches is controlled by a logic input and all three are controlled by a common enable input. All inputs are TTL/CMOS compatible for direct connection to logic circuits. Each source is available for the insertion of the sense resistors in current control applications.

Two versions are available : the L6122 mounted in a Powerdip 14 + 3 + 3 package and the L6123 in a 15-lead Multiwatt package.

BLOCK DIAGRAM

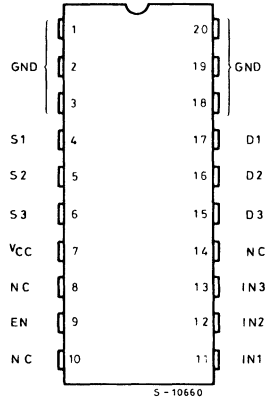


ABSOLUTE MAXIMUM RATINGS

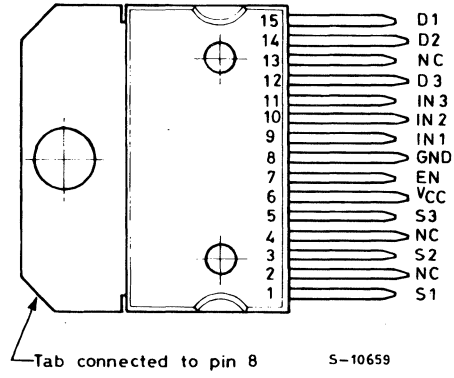
Symbol	Parameter		Value	Unit
V_{DS}	Drain-source Voltage		100	V
V_{CC}	Supply Voltage		60	V
I_D	Continuous Drain Current	@ T_{pins} = 90 °C Powerdip	1.5	A
		@ T_{case} = 90 °C Multiwatt –15	3	A
I_{DM} (*)	Pulsed Drain Current	Powerdip	5	A
		Multiwatt –15	8	A
I_{SD}	Continuous Source-drain Diode Current	@ T_{pins} = 90 °C Powerdip	1.5	A
		@ T_{case} = 90 °C Multiwatt –15	3	A
I_{SDM}	Pulsed Source Drain Diode Current	Powerdip	5	A
		Multiwatt –15	8	A
V_{IN}	Input Voltage		7	V
V_{EN}	Enable Voltage		7	V
V_S	Source Voltage		– 1 to + 4	V
P_{tot}	Total Power Dissipation	@ T_{pins} = 90 °C Powerdip	4.3	W
		@ T_{case} = 90 °C Multiwatt –15	20	W
		@ T_{amb} = 70 °C Powerdip	1.3	W
		@ T_{amb} = 70 °C Multiwatt –15	2.3	W
T_{stg}, T_j	Storage and Junction Temperature Range		– 40 to + 150	°C

(*) Pulse width ≤ 300 µs, duty cycle ≤ 10 %.
NOTE : I_D, I_{DM}, I_{SD}, I_{SDM} are given per channel.

CONNECTION DIAGRAMS (top view)



L6122 (Powerdip)



L6123 (Multiw. 15)

THERMAL DATA

			Powerdip	Multiwatt –15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	-
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	-	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	65 °C/W	35 °C/W

ELECTRICAL CHARACTERISTICS (T_j = 25 °C, V_{CC} = 40 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		14		48	V
I_{CC}	Supply Current	All V_{IN} = H V_{EN} = Square Wave (200 KHz, 50 % DC)		9		mA
I_Q	Quiescent Current	V_{EN} = L		2	3	mA
BV_{DSS}	Drain Source Breakdown Voltage	I_D = 1 mA, V_{EN} = L	100			V
I_{DSS}	Output Leakage Current	V_{EN} = L, V_{DS} = 100 V			1	mA
		V_{EN} = L, V_{DS} = 80 V, T_j = 125 °C		1		mA
$R_{DS\ (on)}$ (*)	Static Drain-source on Resistance	$V_{CC} \geq$ 14 V, I_D = 1.5 A, V_{EN}, V_{IN} = H		0.7		Ω
V_{INL}, V_{ENL}	Input Low Voltage		− 0.3		0.8	V
V_{INH}, V_{ENH}	Input High Voltage		2		7	V
I_{INL}, I_{ENL}	Input Low Current	V_{IN}, V_{EN} = L			− 100	µA
I_{INH}, I_{ENH}	Input High Current	V_{IN}, V_{EN} = H			10	µA
$t_{d\ (on)}$	Turn on Delay Time	I_D = 1.5 A See Test Circuit and Waveforms		300		ns
t_r	Rise Time			100		ns
$t_{d\ (off)}$	Turn off Delay Time			400		ns
t_f	Fall Time			100		ns
V_{SD} (*)	Source Drain Diode Forward Voltage	I_{SD} = 1.5 A, V_{EN} = L			1.5	V
$V_{SD\ (on)}$ (*)	Source Drain Forward Voltage	I_{SD} = 1.5 A, V_{IN}, V_{EN} = H			1.2	V

(*) Pulse test : pulse width = 300 µs, duty cycle = 2 %.

SWITCHING TIMES RESISTIVE LOAD

Figure 1 : Test Circuit.

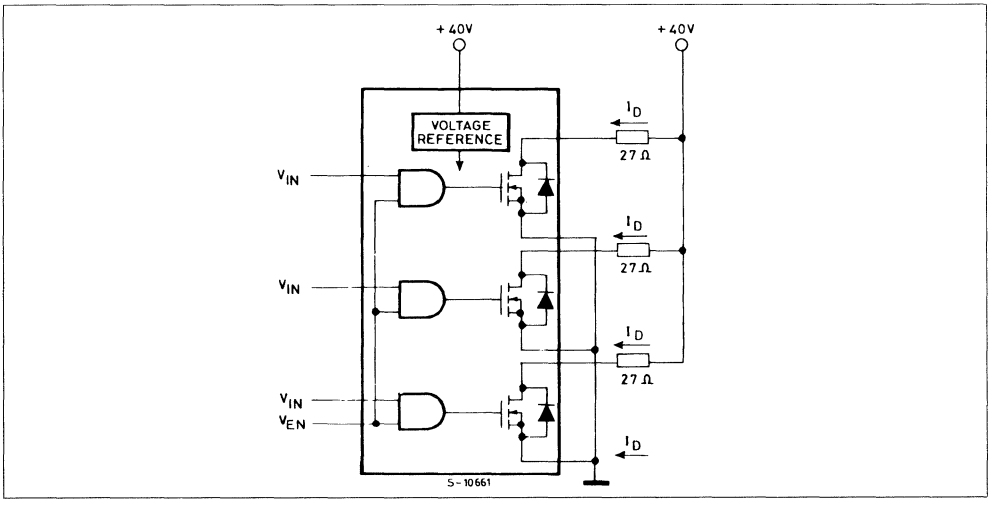


Figure 2 : Waveforms.

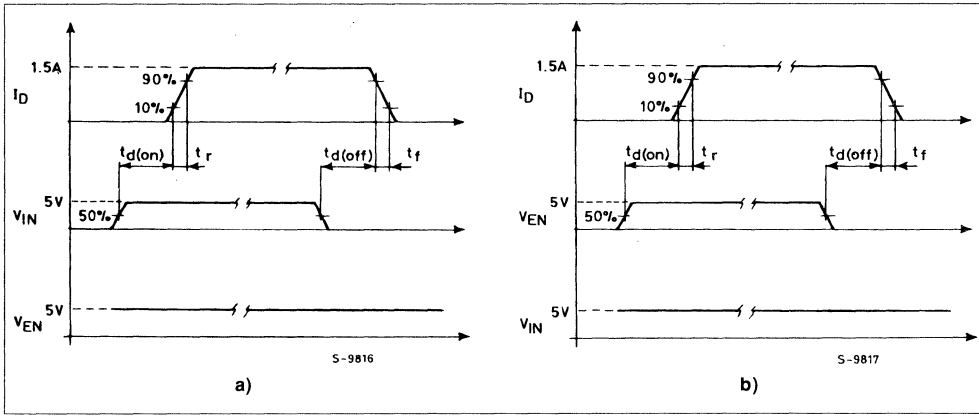


Figure 3 : Static Drain-source on Resistance.

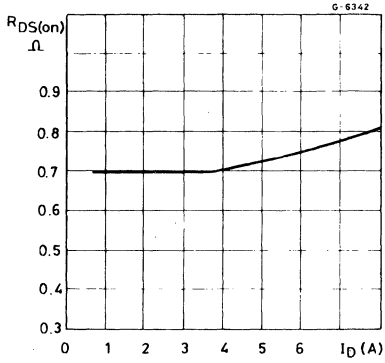


Figure 4 : Normalized Breakdown Voltage vs. Temperature.

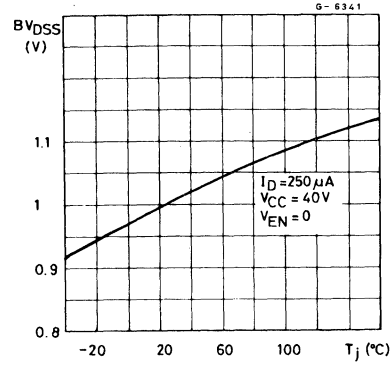


Figure 5 : Normalized on Resistance vs. Temperature.

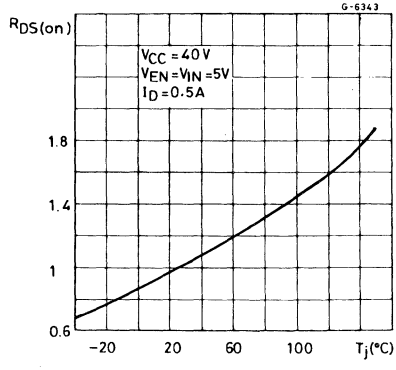


Figure 6 : Typical Source-drain Diode Forward Voltage.

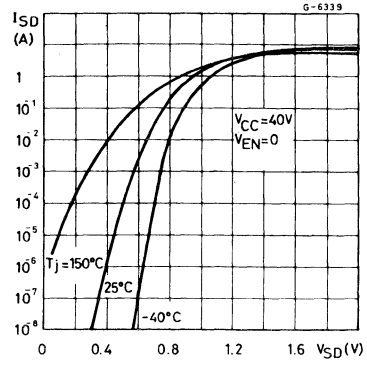
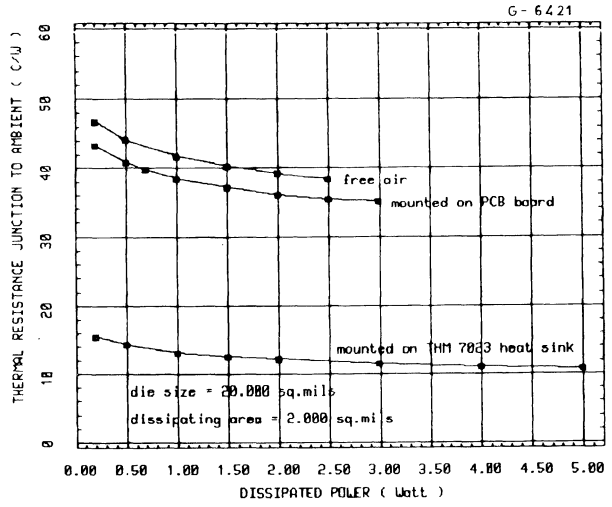


Figure 7 : $R_{th\ j\text{-}amb}$ vs. Dissipated Power (Multiwatt).



(*) Rth ≈ 9°C/W

Figure 8 : Transient Thermal Resistance for Single Pulses (Multiwatt).

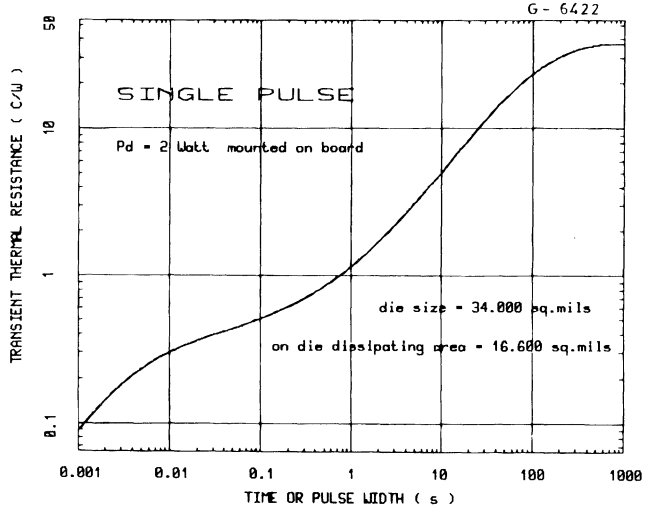
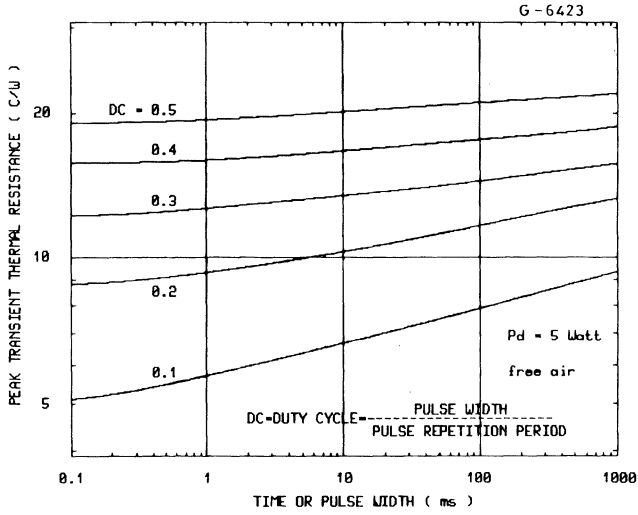


Figure 9 : Peak Transient Thermal Resistance vs. Pulse Width and Duty Cycle (Multiwatt).



0.3Ω DMOS FULL BRIDGE DRIVER

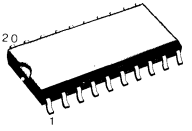
ADVANCE DATA

- SUPPLY VOLTAGE UP TO 48V
- 2A MAX PEAK CURRENT
- TOTAL RMS CURRENT UP TO 1.0A (limited by power dissipation)
- $RD_{DS(ON)}$ 0.3Ω (TYPICAL VALUE AT 25°C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY (TYPICAL 90%)

DESCRIPTION

The L6201 is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can deliver 1.0A RMS at motor supply voltages up to 48V and efficiently at high switching speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The L6201 is mounted in an SO.20 package. Even at the full rated current and voltage no external heatsink is required at normal operating temperatures.

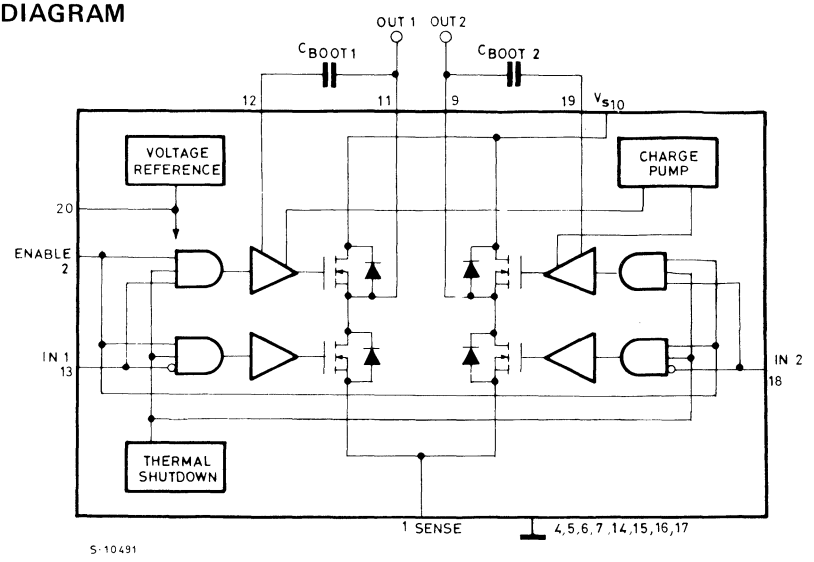
MultiPower BCD Technology



SO-20
(12 + 4 + 4)

ORDERING NUMBER: L6201

BLOCK DIAGRAM

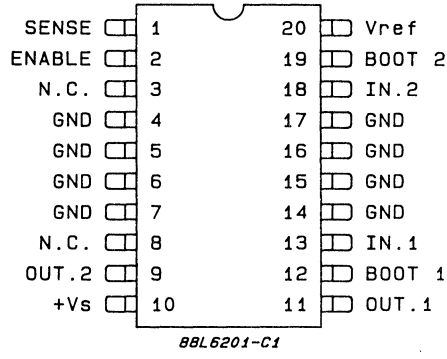


ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	52	V
V_{IN}, V_{EN}	Input or Enable voltage	-0.3 to 7	V
I_o	DC output current (note 1)	1	A
	- non repetitive (< 1ms)	5	A
V_{sense}	Sensing voltage	-1 to 4	V
V_b	Boostrap peak voltage	60	V
P_{tot}	Total power dissipation (T_{pins} = 90°C)	4	W
	(T_{amb} = 70°C no copper area on PCB)	0.9	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Note 1 : Pulse width limited only by junction temperature and the transient thermal impedance.

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	15	°C/W

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	SENSE	A resistance R_{sense} connected to this pin provides feedback for motor current control
2	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.
3	NO CONNECTION	
4, 5, 6, 7	GND	Common ground terminal.
8	NO CONNECTION	
9	OUT2	Output of the half bridge.
10	V_s	Supply voltage.
11	OUT1	Output of the half bridge.
12	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
13	IN1	Digital input from the motor controller.
14,15,16,17	GND	Common ground terminal.
18	IN2	Digital input from the motor controller.
19	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
20	V_{ref}	Internal voltage reference, a capacitor from this pin to GND increases stability of the POWER DMOS logic drive circuit.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_j = 25°C, V_s = 36V, unless otherwise stated)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		12	36	48	V
V_{ref}	Reference voltage			13.5		V
I_s	Quiescent supply current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L Fig. 10		10 10 8		mA mA mA
f_c	Commutation frequency (*)			30	100	KHz
T_j	Thermal shutdown			150		°C
T_d	Dead time protection			100		ns
TRANSISTORS						
OFF						
I_{DSS}	Leakage current	Fig. 11		100		µA
ON						
R_{DS}	On resistance			0.3		Ω
$V_{DS(ON)}$	Drain source voltage	I_{DS} = 1.0A Fig. 9		0.3		V
V_{sens}	Sensing voltage		-1		4	V
SOURCE DRAIN DIODE						
V_{sd}	Forward ON voltage	I_{SD} = 1.0A EN = L		0.9(**)		V
t_{rr}	Reverse recovery time	I_F = 1.0A $\frac{dif}{dt}$ = 25A/µs		300		ns
t_{fr}	Forward recovery time			200		ns
LOGIC LEVELS						
$V_{IN\,L}$, $V_{EN\,L}$	Input Low voltage		-0.3		0.8	V
$V_{IN\,L}$, $V_{EN\,H}$	Input High voltage		2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low current	V_{IN}, V_{EN} = L			-10	µA
$I_{IN\,H}$, $I_{EN\,H}$	Input High current	V_{IN}, V_{EN} = H		30		µA
LOGIC CONTROL TO POWER DRIVE TIMING						
t_1 (V_i)	Source current turn-off delay	Fig. 12		300		ns
t_2 (V_i)	Source current fall time	Fig. 12		200		ns
t_3 (V_i)	Source current turn-on delay	Fig. 12		400		ns
t_4 (V_i)	Source current rise time	Fig. 12		200		ns
t_5 (V_i)	Sink current turn-off delay	Fig. 13		300		ns
t_6 (V_i)	Sink current fall time	Fig. 13		200		ns
t_7 (V_i)	Sink current turn-on delay	Fig. 13		400		ns
t_8 (V_i)	Sink current rise time	Fig. 13		200		ns

(*) Limited by power dissipation
(**) In synchronous rectification the drain - source voltage is of 0.3V typ.

Fig. 1 - Typical I_s normalized vs. T_j

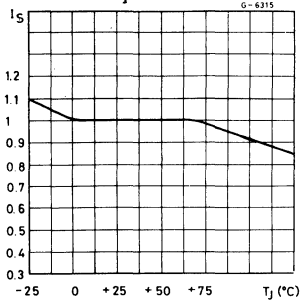


Fig. 2 - Quiescent current vs. frequency

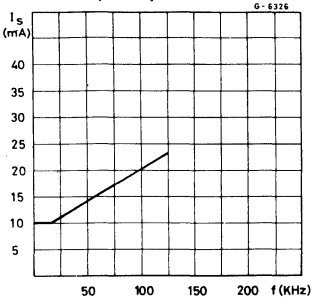


Fig. 3 - Typical I_s normalized vs. V_s

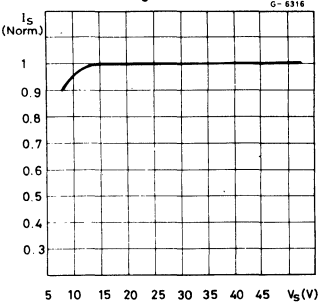


Fig. 4 - Typical diode behaviour in synchronous rectification

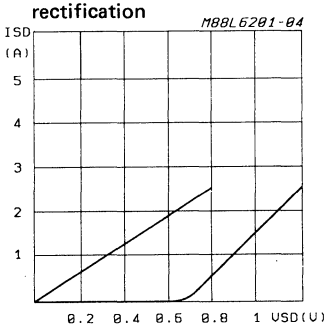


Fig. 5 - Typical $R_{DS\ (ON)}$ vs. $V_s \cong V_{ref}$

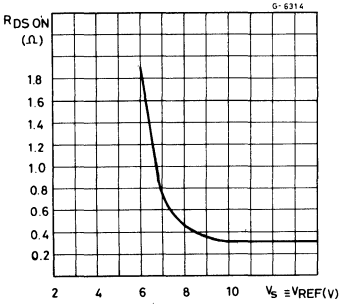


Fig. 6 - $R_{DS\ (ON)}$ normalized at 25°C vs. temperature typical values

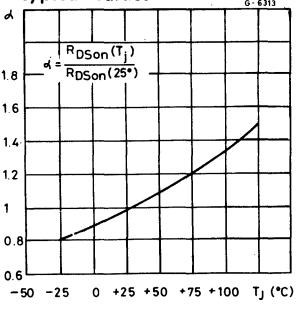


Fig. 7 - $R_{DS\ (ON)}$ vs. DMOS transistor current

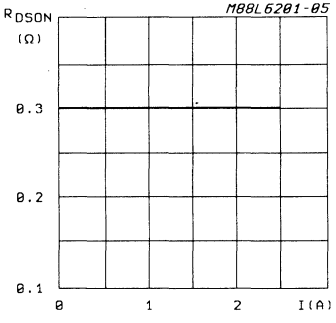


Fig. 8 - Typical power dissipation vs. I_L

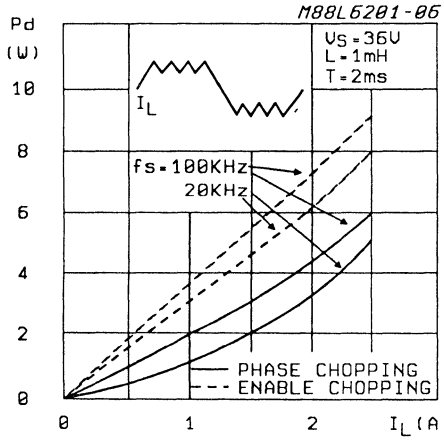


Fig. 8a - Two phase chopping

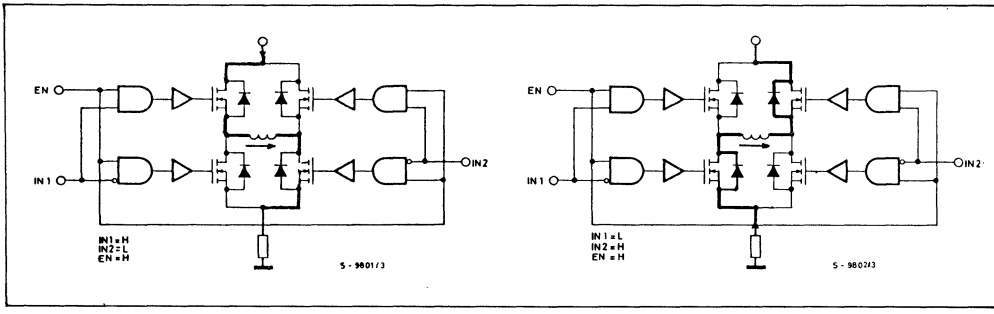


Fig. 8b - One phase chopping

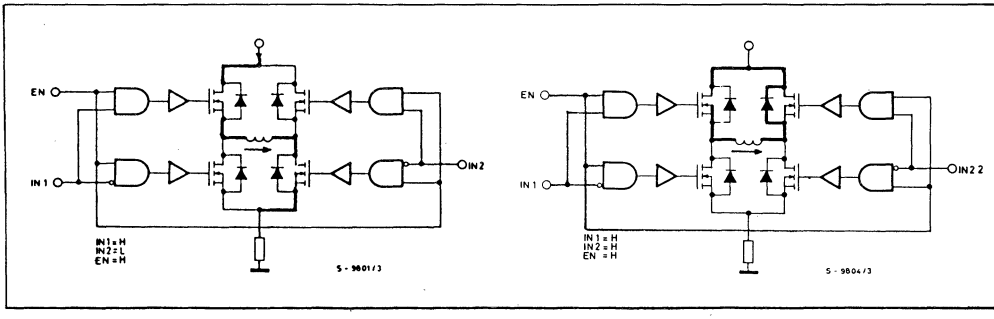
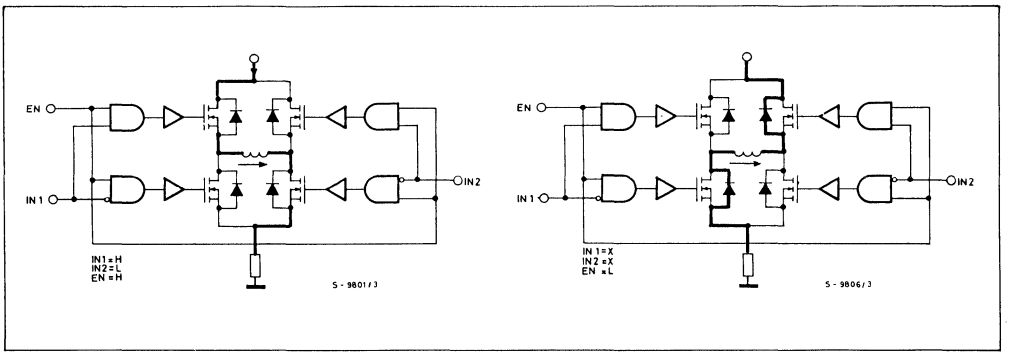


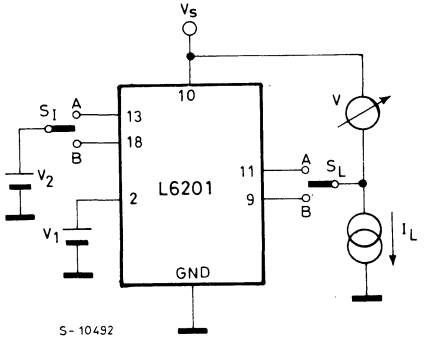
Fig. 8c - Enable chopping



TEST CIRCUITS

Fig. 9 - Saturation voltage

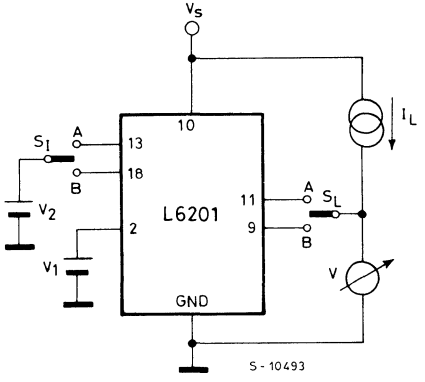
a) Source outputs



For IN1 source output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "H"

For IN2 source output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "H"

b) Sink outputs



For IN1 sink output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "L"

For IN2 sink output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "L"

TEST CIRCUITS (continued)

Fig. 10 - Quiescent current

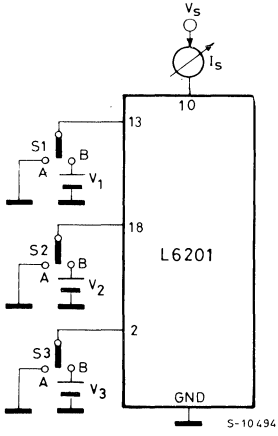
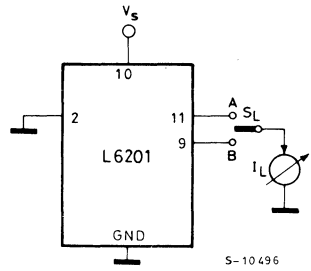
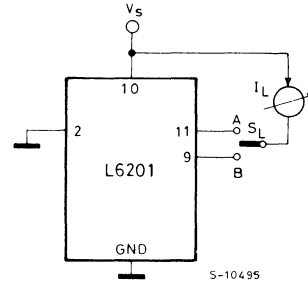


Fig. 11 - Leakage current

a) Source outputs

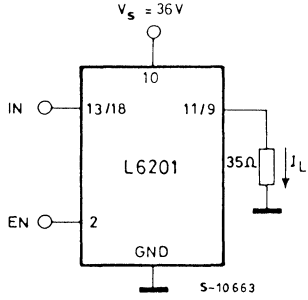


b) Sink outputs



SWITCHING TIMES

Fig. 12 - Source current delay times vs. input



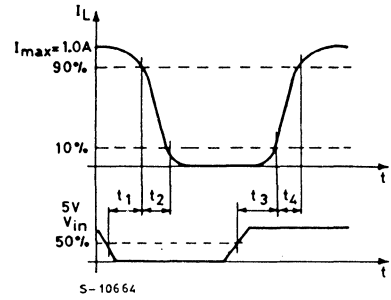
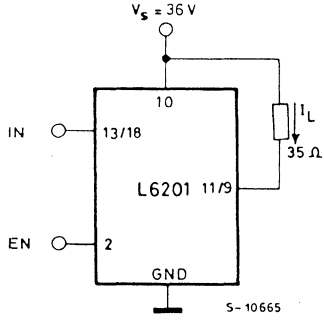
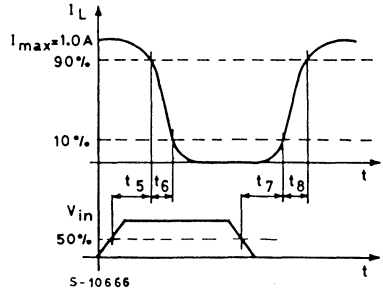


Fig. 13 - Sink current delay times vs. input





CIRCUIT DESCRIPTION

The L6201 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components.

LOGIC DRIVE

INPUTS			OUTPUT MOSFETS (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned OFF

L = Low H = High X = Don't care

(*) Numbers referred to INPUT 1 or INPUT2 controlled outputs stages

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 15)

Fig. 14 - Intrinsic structures in the POWER DMOS transistors

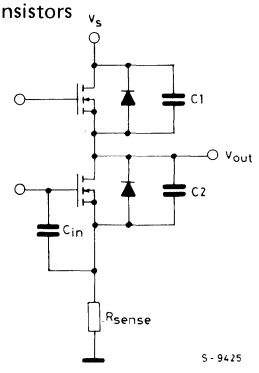
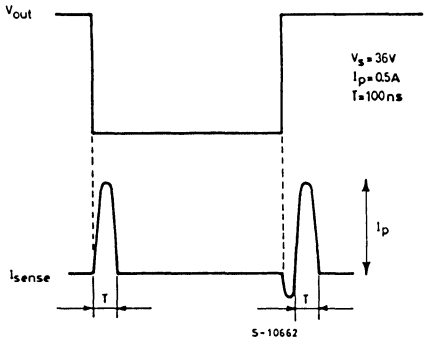


Fig. 15 - Current typical spikes on the sensing pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS(ON)}$ (= 0.3Ω) throughout the recommended operating range. In this condition the dissipated power is given by:

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by:

$$P_{OFF} = V_s \cdot I_{DSS}$$

The power dissipation is in the order of pW and is negligible in comparison to that dissipated in the ON STATE.

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode

applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOSTRAP CAPACITORS

To ensure that the POWER DMOS transistors are driven correctly gate source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. This is no problem for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. In the L6201 this achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit charges the external C_B capacitors when the source transistor is OFF and the sink transistor is ON giving lower commutation losses in switched mode operation. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1nF. It is recommended that a capacitance of at least 10nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher $R_{DS\,(ON)}$. On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

REFERENCE

To stabilise the internal drive circuit it is recommended that a capacitor be placed between this pin and ground. A value of 0.22μF should be sufficient for most applications.

This pin is also protected against a short circuit to ground.

DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail to rail short, the logic control circuit provides a dead time greater than 40ns.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature e reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION

In order to achieve the high performance provided by the L6201 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 16 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case:

$$E_{OFF/ON} = [R_{DS\,(ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_s \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;
$T_{COM} = T_{TURN-ON} = T_{TURN-OFF} = 100ns$
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L^2 \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

The Total Power Dissipation P_{DIS} is simply:

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

Fig. 16 - Load current in half step operation

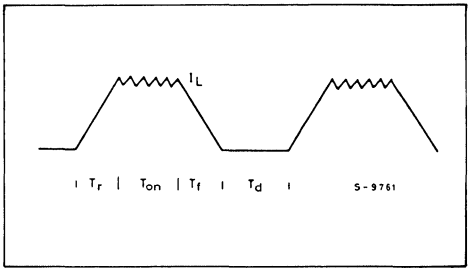


Fig. 17 shows a two phase Bipolar Stepper Motor Control circuit where the current is controlled by the IC L297.
Between the sense resistors and each sense input of the L297 a resistor must be foreseen; if the connections between the outputs of the L297 and the inputs of the L6201 need a long path, a resistor must be connected between each input of the L6201 and ground.
When the Supply Voltage is higher than 26V or if the motor is driven through long wires, a snubber network made by the series of R and C must be foreseen very near to the output pins of the L6201.
The following formulas can be used :

$R \simeq V_s/I_p$
$C = I_p/(dv/dt)$ where
V_s is the max supply voltage foreseen on the application;
I_p is the peak of the lood current;
dv/dt is the needed rise time of the output voltage (200V/μsec is generally used).

Fig. 17 - Two phase Bipolar stepper motor control circuit with chopper current control and translator

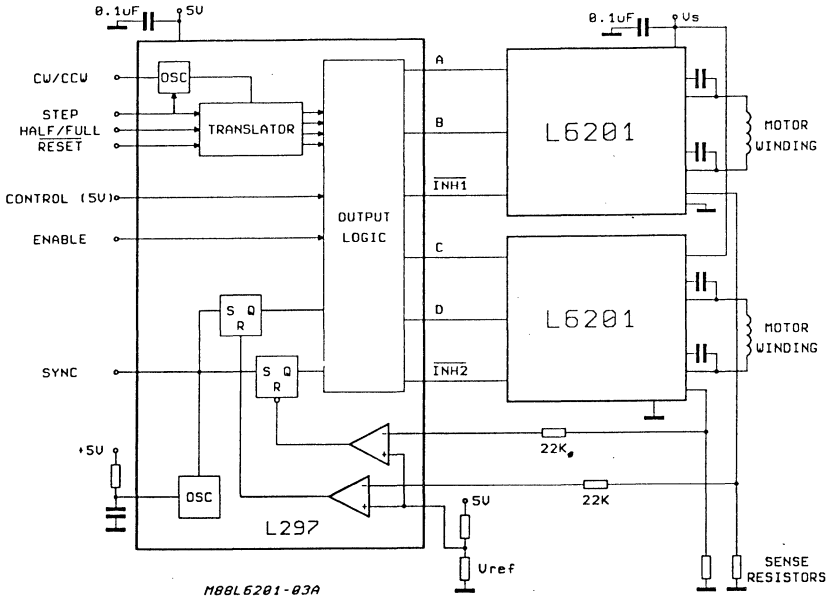
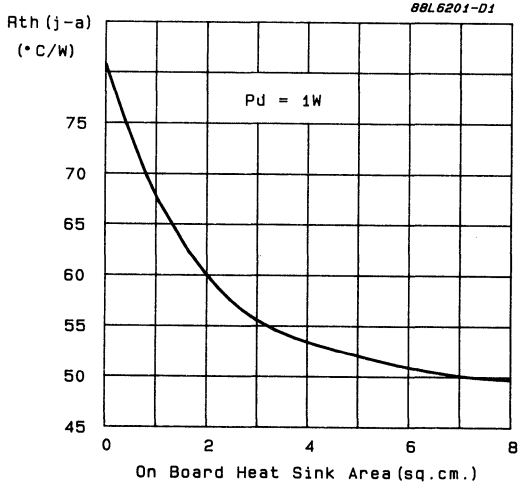


Fig. 18 - Rth junction to ambient vs. "on board" heat sink area



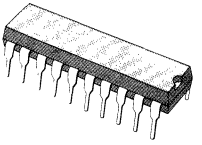
0.3Ω DMOS FULL BRIDGE DRIVER

PRELIMINARY DATA

- SUPPLY VOLTAGE UP TO 48V
- 5A MAX PEAK CURRENT
- TOTAL RMS CURRENT UP TO 1.5A
- $R_{DS\ (ON)}$ 0.3Ω (TYPICAL VALUE AT 25°C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY (TYPICAL 90%)

The L6202 is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can deliver 1.5A RMS at motor supply voltages up to 48V and efficiently at high switching speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The L6202 is mounted in an 18-lead powerdip package and the six center pins are used to conduct heat to the PCB. Even at the full rated current and voltage no external heatsink is required at normal operating temperatures.

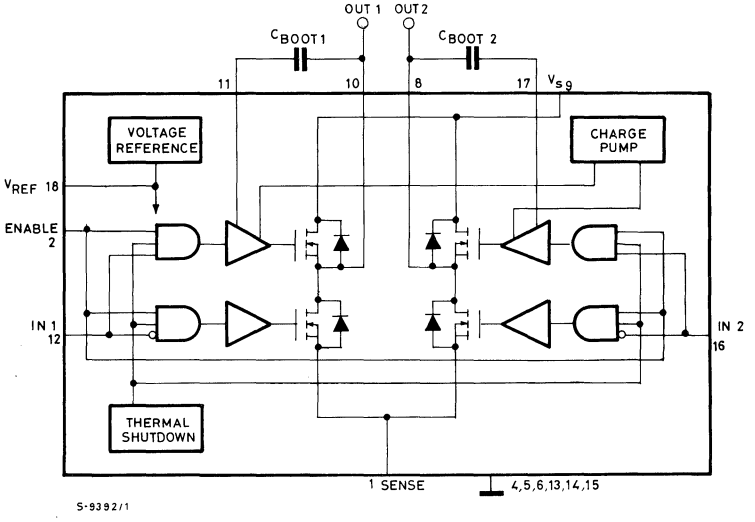
MultiPower BCD Technology



Powerdip 12+3+3

ORDERING NUMBER: L6202

BLOCK DIAGRAM

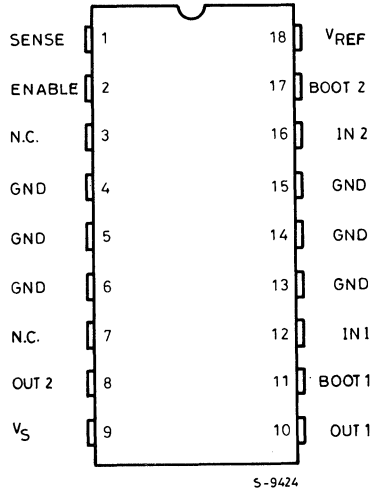


ABSOLUTE MAXIMUM RATINGS

V_s	Power supply	52	V
V_{OD}	Differential output voltage (Between pins 10 and 8)	60	V
V_{IN}, V_{EN}	Input or Enable voltage	-0.3 to 7	V
I_o	Pulsed output current (note 1)	5	A
	- non repetitive ($<$ 1ms)	10	A
V_{sense}	Sensing voltage	-1 to 4	V
V_b	Boostrap peak voltage	60	V
P_{tot}	Total power dissipation (T_{pins} = 90°C)	5	W
	(T_{amb} = 70°C no copper area on PCB)	1.3	W
	(T_{amb} = 70°C 4cm^2 copper area on PCB)	2	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Note 1 : Pulse width limited only by junction temperature and the transient thermal impedance.

CONNECTION DIAGRAM
(Top view)



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (Fig. 21)	max	60	°C/W

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	SENSE	A resistance R_{sense} connected to this pin provides feedback for motor current control.
2	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.
3	NO CONNECTION	
4	GND	Common ground terminal.
5	GND	Common ground terminal.
6	GND	Common ground terminal.
7	NO CONNECTION	
8	OUT2	Output of the half bridge.
9	V_s .	Supply voltage.
10	OUT1	Output of the half bridge.
11	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
12	IN1	Digital input from the motor controller.
13	GND	Common ground terminal.
14	GND	Common ground terminal.
15	GND	Common ground terminal.
16	IN2	Digital input from the motor controller.
17	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
18	V_{ref}	Internal voltage reference, a capacitor from this pin to GND increases stability of the POWER DMOS logic drive circuit.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_j = 25°C, V_s = 42V, unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		12	36	48	V
V_{ref}	Reference voltage			13.5		V
I_{REF}	Output current				2	mA
I_s	Quiescent supply current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L Fig. 10		10 10 8		mA mA mA
f_c	Commutation frequency (*)			30	100	KHz
T_j	Thermal shutdown			150		°C
T_d	Dead time protection			100		ns
TRANSISTORS						
OFF						
I_{DSS}	Leakage current	Fig. 11 V_s = 52V			1	mA
ON						
R_{DS}	On resistance			0.3		Ω
$R_{DS\ (ON)}$	Drain source voltage	I_{DS} = 1.2 A Fig. 9		0.36		V
V_{sens}	Sensing voltage		-1		4	V
SOURCE DRAIN DIODE						
V_{sd}	Forward ON voltage	I_{SD} = 1.2A EN = L		0.9(**)		V
t_{rr}	Reverse recovery time	I_F = 1.2A $\frac{dif}{dt}$ = 25A/μs		300		ns
t_{fr}	Forward recovery time			200		ns
LOGIC LEVELS						
$V_{IN\,L}$, $V_{EN\,L}$	Input Low voltage		-0.3		0.8	V
$V_{IN\,L}$, $V_{EN\,H}$	Input High voltage		2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low current	V_{IN}, V_{EN} = L			-10	μA
$I_{IN\,H}$, $I_{EN\,H}$	Input High current	V_{IN}, V_{EN} = H		30		μA
LOGIC CONTROL TO POWER DRIVE TIMING						
t_1 (V_i)	Source current turn-off delay	Fig. 12		300		ns
t_2 (V_i)	Source current fall time	Fig. 12		200		ns
t_3 (V_i)	Source current turn-on delay	Fig. 12		400		ns
t_4 (V_i)	Source current rise time	Fig. 12		200		ns
t_5 (V_i)	Sink current turn-off delay	Fig. 13		300		ns
t_6 (V_i)	Sink current fall time	Fig. 13		200		ns
t_7 (V_i)	Sink current turn-on delay	Fig. 13		400		ns
t_8 (V_i)	Sink current rise time	Fig. 13		200		ns

(*) Limited by power dissipation
(**) In synchronous rectification the drain-source voltage drop V_{DS} is shown in fig. 4.

Fig. 1 - Typical I_s normalized vs. T_j

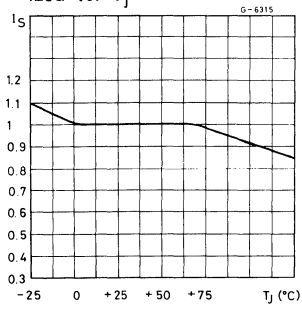


Fig. 2 - Quiescent current vs. frequency

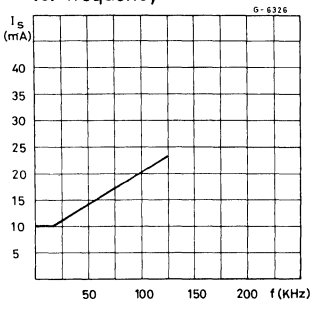


Fig. 3 - Typical I_s normalized vs. V_s

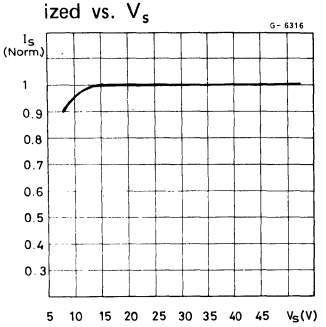


Fig. 4 - Typical diode behaviour in synchronous rectification

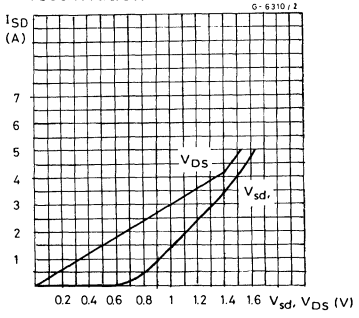


Fig. 5 - Typical $R_{DS\ (ON)}$ vs. $V_s \cong V_{ref}$

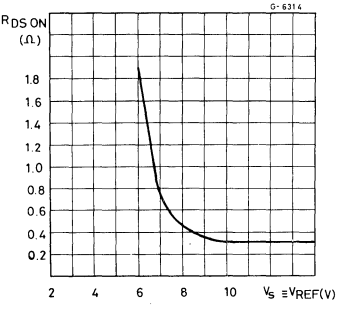


Fig. 6 - $R_{DS\ (ON)}$ normalized at 25°C vs. temperature typical values

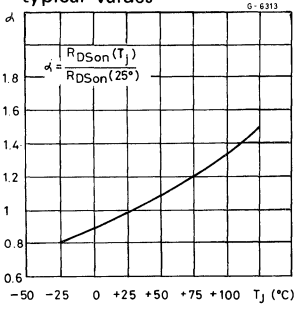


Fig. 7 - $R_{DS\ (ON)}$ vs. DMOS transistor current

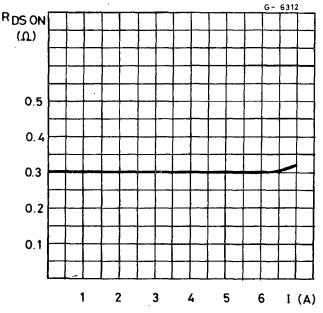


Fig. 8 - Typical power dissipation vs. I_L

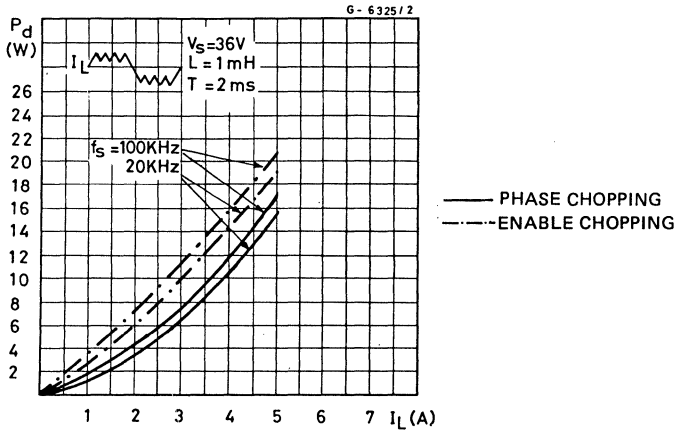


Fig. 8a - Two phase chopping

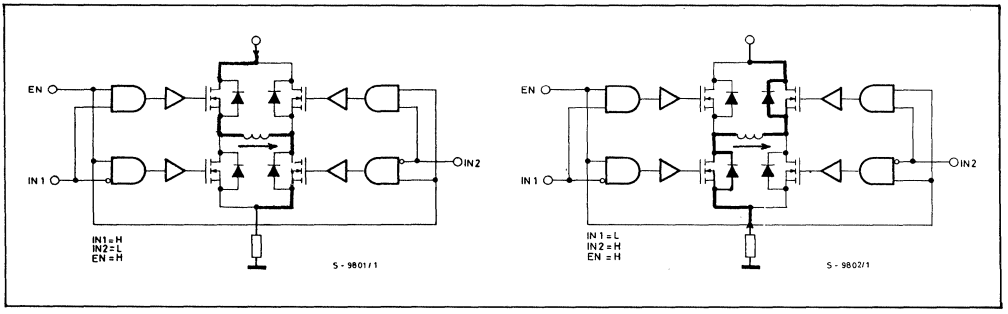


Fig. 8b - One phase chopping

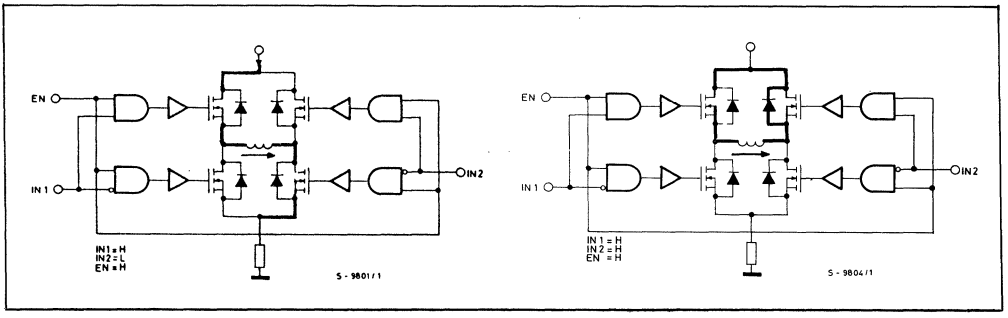
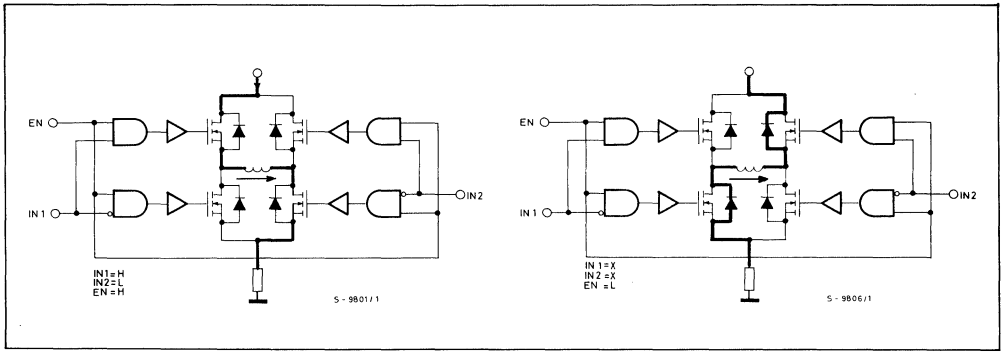


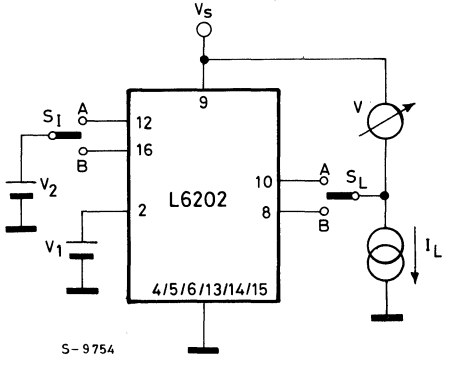
Fig. 8c - Enable chopping



TEST CIRCUITS

Fig. 9 - Saturation voltage

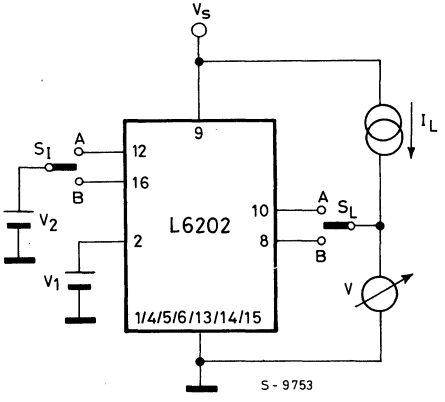
a) Source outputs



For IN1 source output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "H"

For IN2 source output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "H"

b) Sink outputs



For IN1 sink output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "L"

For IN2 sink output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "L"

TEST CIRCUITS (continued)

Fig. 10 - Quiescent current

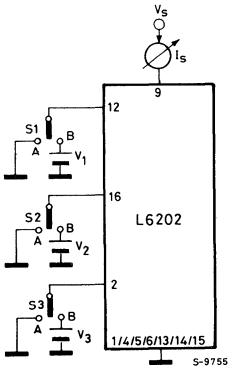
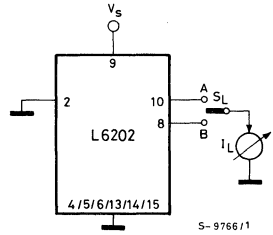
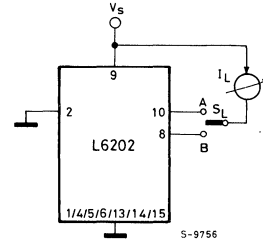


Fig. 11 - Leakage current

a) Source outputs

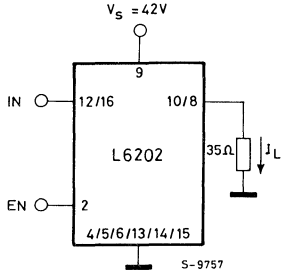


b) Sink outputs



SWITCHING TIMES

Fig. 12 - Source current delay times vs. input chopper



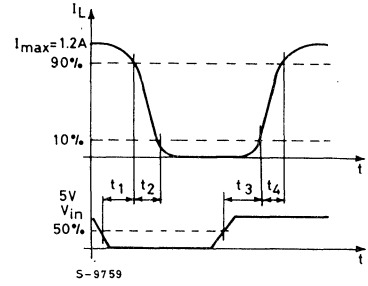
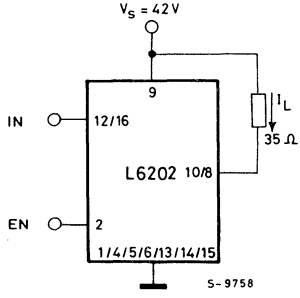
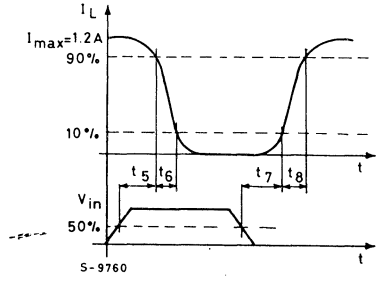


Fig. 13 - Sink current delay times vs. input chopper





CIRCUIT DESCRIPTION

The L6202 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components.

LOGIC DRIVE

INPUTS			OUTPUT MOSFETS (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned OFF

L = Low H = High X = Don't care

(*) Numbers referred to INPUT 1 or INPUT2 controlled outputs stages

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 15)

Fig. 14 - Intrinsic structures in the POWER DMOS transistors

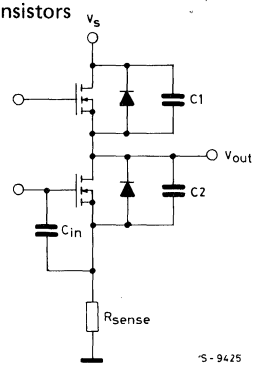
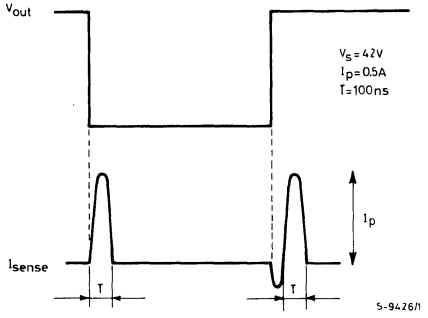


Fig. 15 - Current typical spikes on the sensing pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS\,(ON)}$ (= 0.3Ω) throughout the recommended operating range. In this condition the dissipated power is given by:

$$P_{ON} = R_{DS\,(ON)} \cdot I_{DS}^2$$

The low $R_{DS\,(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by:

$$P_{OFF} = V_s \cdot I_{DSS}$$

The power dissipation is in the order of pW and is negligible in comparison to that dissipated in the ON STATE.

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode

applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOSTRAP CAPACITORS

To ensure that the POWER DMOS transistors are driven correctly gate source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. This is no problem for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. In the L6202 this achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit charges the external C_B capacitors when the source transistor is OFF and the sink transistor is ON giving lower commutation losses in switched mode operation. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1nF. It is recommended that a capacitance of at least 10nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher $R_{DS\,(ON)}$. On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

REFERENCE

To stabilise the internal drive circuit it is recommended that a capacitor be placed between this pin and ground. A value of 0.22μF should be sufficient for most applications.

This pin is also protected against a short circuit to ground.

DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail to rail short, the logic control circuit provides a dead time greater than 40ns.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature e reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\,(ON)} \cdot I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION

In order to achieve the high performance provided by the L6202 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 16 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case:

$$E_{OFF/ON} = [R_{DS\,(ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_s \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;
$T_{COM} = T_{TURN-ON} = T_{TURN-OFF} = 100ns$
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L^2 \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

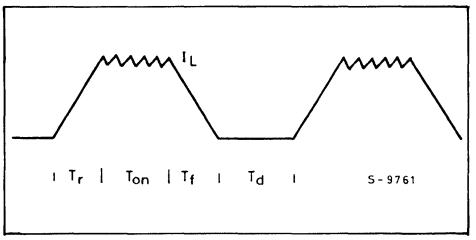
The Total Power Dissipation P_{DIS} is simply:

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

Fig. 16

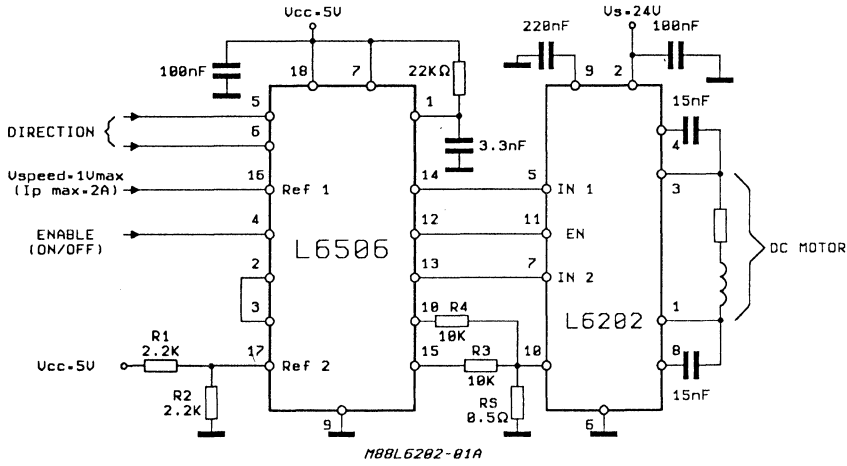


DC MOTOR SPEED CONTROL

Since the L6202 integrates a full H-Bridge in a single package it is idealy suited for controlling small DC motors. When used for DC motor control the L6202 provides the power stage required for both speed and direction control. The L6202 can be combined with a current regulator like the L6506 to implement a transconductance amplifier for speed control, as shown in figure 17.
In this configuration the L6506 sense the voltage across the sense resistor, R_{SENSE}, to monitor the motor current. The L6506 then compares the sensed voltage to control the speed or during the brake of the L6202.
Between the sense resistor and each sense input of the L6506 a resistor must be foreseen; if the connections between the outputs of the L6506 and the inputs of the L6202 need a long path, a resistor must be connected between each input of the L6202 and ground.
When the Supply Voltage is higher than 26V or if the motor is driven through long wires, a snubber network made by the series of R and C must be foreseen very near to the output pins of the L6202.
The following formulas can be used :

$R \simeq Vs/I_p$
$C = I_p/(dv/dt)$ where
V_s is the max Supply Voltage foreseen on the application;
I_p is the peak of the load current;
dv/dt is the needed rise time of the output voltage (200V/μsec is generally used).
Higher voltages than 26V of V_s require that a diode (BYW98) is connected between each power output pin and ground as well.
If the Power Supply Cannot Sink Current, a suitable large capacitance must be used and connected near the supply pin of the L6202.
Sometimes a capacitor at pin 17 of the L6506 let the application better work.

Fig. 17 - Bidirectional DC motor control



BIPOLAR STEPPER MOTORS APPLICATIONS

Bipolar stepper motors can be driven with an L297 or L6506, two L6202 bridge BCD drivers and very few external components. Together these three chips form a complete microprocessor-to-stepper motor interface.

As shown in Fig. 18 and Fig. 19, the controller connect directly to the two bridge BCD drivers. External component requirements are minimal: an RC network to set the chopper frequency and a resistive divider to establish the comparator reference voltage (pin 15 for L297, pin 10 and 15 for L6506). These solutions have a very high efficiency because of low power dissipation.

A snubber network at the output of the L6202 and resistors between the inputs of the some IC and GND cound be foreseen (see DC Motor Speed Control).

HIGH CURRENT MICROSTEP DRIVE FOR STEPPER MOTORS

The L6202 can by used in conjunction with the L6217 to (figure 20) implement a high current microstepping controller for stepper motors. In this application the L6217 is used as a control circuit and its outputs are used only to drive the inputs of the L6202. The application allows easy interface to a microprocessor since the L6217 may be connected directly to the microprocessor bus.

In the circuit shown in Figure 20, the L6217 senses the motor current by monitoring the voltage across the sense resistors, R_{SENSE}, and compares this value to the output of a 6 bit (7 bit if the L6217A is used) D to A Converter. The L6217 controls the current using a frequency modulated, constant off time, switching controller. The off time of each coil may be set using and external resistor and capacitor connected to PTA and PTB.

In this configuration the microprocessor simply loads the appropriate value for the direction of current flow through the coil and the data for the DAC into the L6217. The L6217 and L6202 then forms the complete interface between the micro and the motor.

When the pins 3 and 4 of the L6217 (Test A and B) are low, the bridges must be in tri-state condition.
For this reason two LM339 comparators must be used. The outputs of the comparators act on the enable inputs of the L6202 ICs.
A bilevel operation can be used for decreasing the minimum controllable load current. The mi-

nimum current that can be controlled is given by the following expression :

$$I_L \text{ (avg.)} = \frac{V_s}{R_{sense} + (2R_{DSon} + R_{LOAD})/DC}$$

where R_{LOAD} is the equivalent resistance of the load DC is the duty cycles given by

$$\frac{T_{on}}{T_{on} + T_{off}}$$

If 12V is forced on pin 18 (Reference voltage) and the supply voltage V_s is reduced below 12V the on resistance tends to increase above the normal guaranteed 0.3ohm.

Consequently the minimum current will also be reduced, as given in the above expression. When a minimum current operation is required, a high signal at point (A) can disable the pnp transistors in fig. 20. So it's possible to operate at a V_s of $(7V - V_{BE})$.

Fig. 18 - Two phase Bipolar stepper motor control circuit with chopper current control

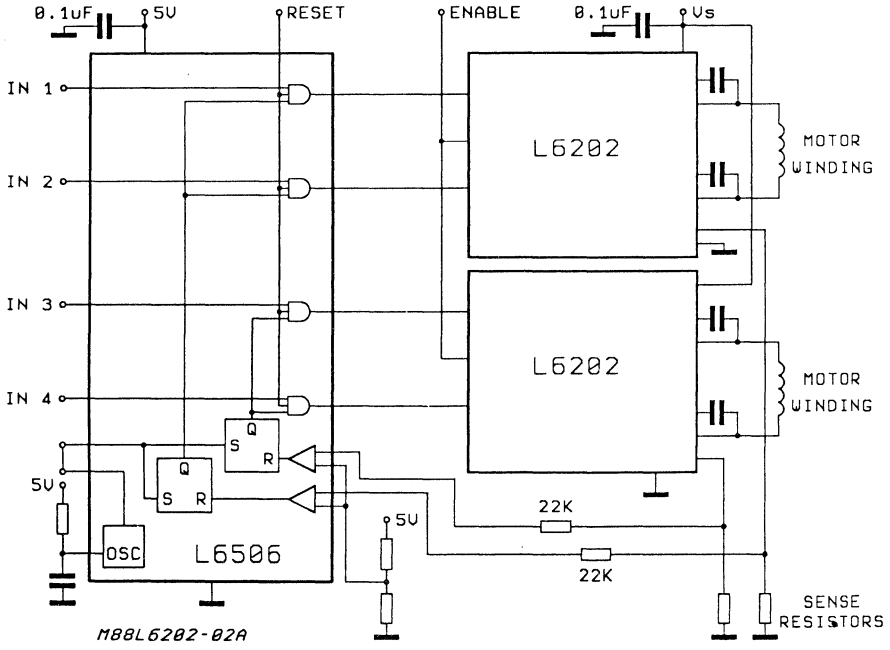


Fig. 19 - Two phase Bipolar stepper motor control circuit with chopper current control and translator

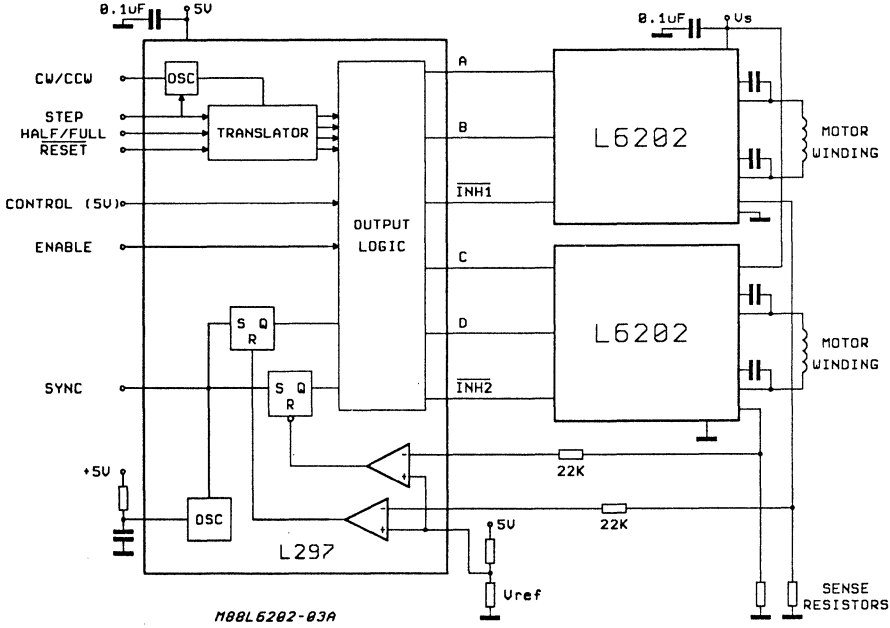
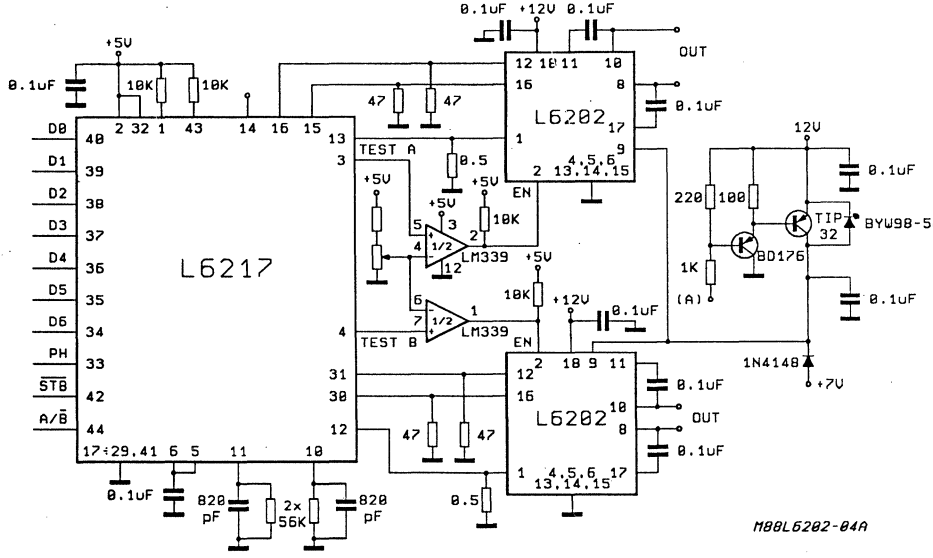


Fig. 20 - High current microstepping controller for stepper motors



THERMAL CHARACTERISTICS

Fig. 21 - R_{th} with two "on board" square heatsink vs. side ℓ

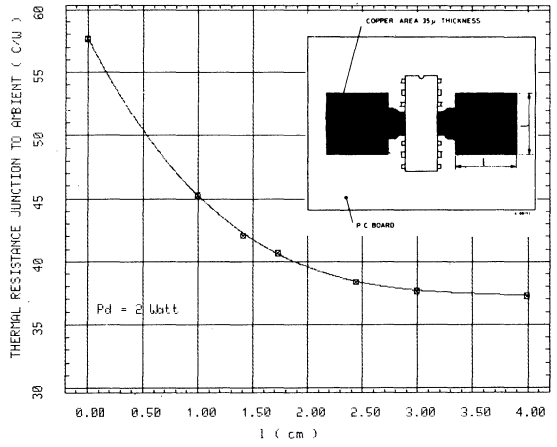


Fig. 22 - Transient thermal resistance for single pulses

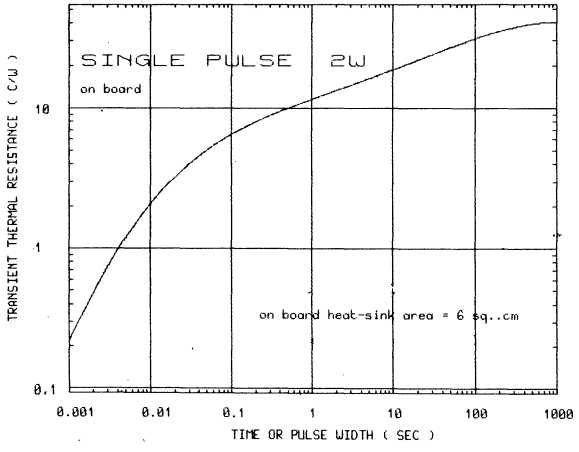
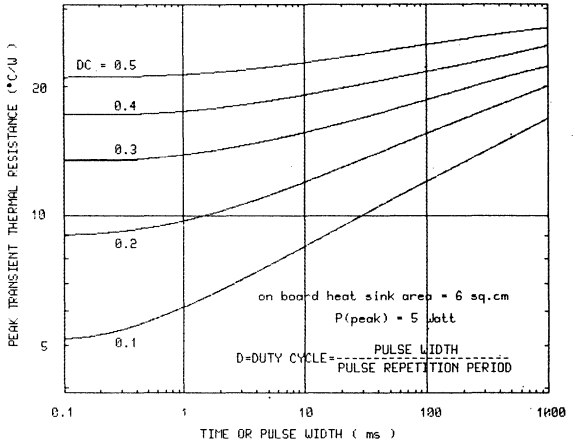


Fig. 23 - Peak transient R_{th} vs. pulse width and duty cycle



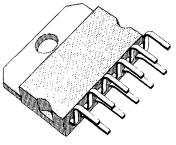
0.3Ω DMOS FULL BRIDGE DRIVER

PRELIMINARY DATA

- SUPPLY VOLTAGE UP TO 48V
- 5A MAX PEAK CURRENT
- TOTAL RMS CURRENT UP TO 4A
- $R_{DS\,(ON)}$ 0.3Ω (TYPICAL VALUE AT 25°C)
- CROSS CONDUCTION PROTECTION
- TTL COMPATIBLE DRIVE
- OPERATING FREQUENCY UP TO 100KHz
- THERMAL SHUTDOWN
- INTERNAL LOGIC SUPPLY
- HIGH EFFICIENCY (TYPICAL 90%)

The L6203 is a full bridge driver for motor control applications realized in Multipower-BCD technology which combines isolated DMOS power transistors with CMOS and Bipolar circuits on the same chip. By using mixed technology it has been possible to optimize the logic circuitry and the power stage to achieve the best possible performance. The DMOS output transistors can deliver 4A RMS at motor supply voltages up to 48V and efficiently at high switch speeds. All the logic inputs are TTL, CMOS and μC compatible. Each channel (half-bridge) of the device is controlled by a separate logic input, while a common enable controls both channels. The L6203 is mounted in a 11-lead Multiwatt package.

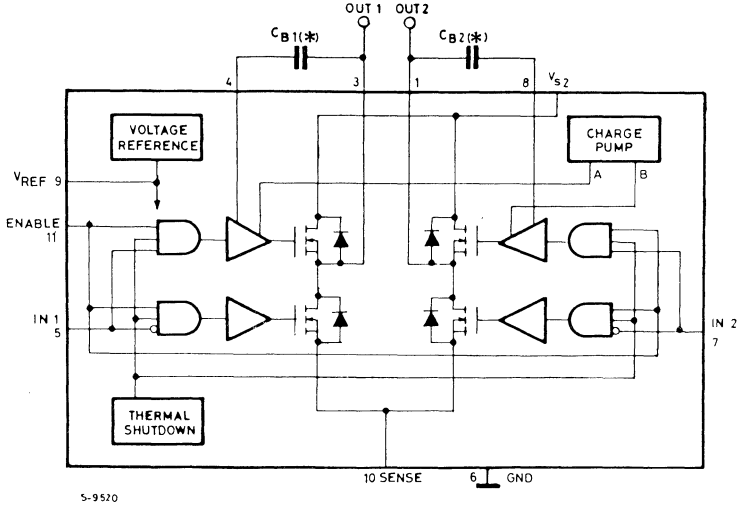
MultiPower BCD Technology



Multiwatt-11

ORDERING NUMBER: L6203

BLOCK DIAGRAM



(*) Suggested value for C_{BOOT1} and C_{BOOT2}: 10nF

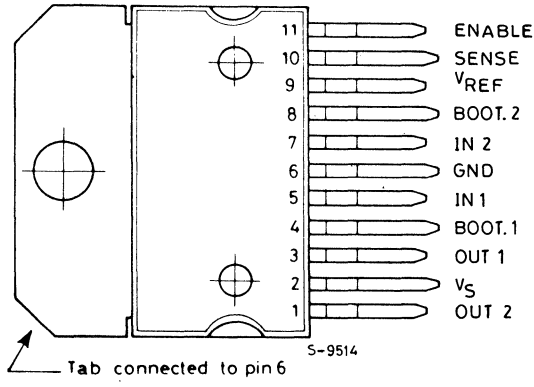
ABSOLUTE MAXIMUM RATINGS

V_S	Power supply	52	V
V_{OD}	Differential output voltage (Between pins 1 and 3)	60	V
V_{IN}, V_{EN}	Input or Enable voltage	-0.3 to 7	V
I_o	Pulsed output current (note 1)	5	A
	- non repetitive ($<$ 1ms)	10	A
V_{sense}	Sensing voltage	-1 to 4	V
V_b	Boostrap peak voltage	60	V
P_{tot}	Total power dissipation (T_{case} = 90°C)	20	W
	(T_{amb} = 70°C free air)	2.3	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Note 1 : Pulse width limited only by junction temperature and the transient thermal impedance.

CONNECTION DIAGRAM

(Top view)



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	35	°C/W

PIN FUNCTIONS

PIN	NAME	FUNCTION
1	OUT2	Output of the half bridge.
2	V_s	Supply voltage.
3	OUT1	Output of the half bridge.
4	BOOT1	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
5	IN1	Digital input from the motor controller.
6	GND	Common ground terminal.
7	IN2	Digital input from the motor controller.
8	BOOT2	A boostrap capacitor connected to this pin ensures efficient driving of the upper POWER DMOS transistor at high switching frequencies.
9	V_{ref}	Internal voltage reference, a capacitor from this pin to GND increases stability of the POWER DMOS logic drive cricuit.
10	SENSE	A resistance R_{sense} connected to this pin provides feedback for motor current control.
11	ENABLE	When a logic high is present on this pin the DMOS POWER transistors are enabled to be selectively driven by IN1 and IN2.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits T_j = 25°C, V_s = 42V, unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		12	36	48	V
V_{ref}	Reference voltage			13.5		V
I_{REF}	Output current				2	mA
I_s	Quiescent supply current	EN = H V_{IN} = L EN = H V_{IN} = H I_L = 0 EN = L Fig. 10		10 10 8		mA mA mA
f_c	Commutation frequency (*)			30	100	KHz
T_j	Thermal shutdown			150		°C
T_d	Dead time protection			100		ns
TRANSISTORS						
OFF						
I_{DSS}	Leakage current	Fig. 11 V_s = 52V			1	mA
ON						
R_{DS}	On resistance			0.3		Ω
$V_{DS\ (ON)}$	Drain source voltage	I_{DS} = 3A		0.9		V
V_{sens}	Sensing voltage		-1		4	V
SOURCE DRAIN DIODE						
V_{sd}	Forward ON voltage	I_{SD} = 3A EN = L		1,35(**)		V
t_{rr}	Reverse recovery time	I_F = 3A $\frac{dif}{dt}$ = 25A/μs		300		ns
t_{fr}	Forward recovery time			200		ns
LOGIC LEVELS						
$V_{IN\,L}$, $V_{EN\,L}$	Input Low voltage		-0.3		0.8	V
$V_{IN\,H}$, $V_{EN\,H}$	Input High voltage		2		7	V
$I_{IN\,L}$, $I_{EN\,L}$	Input Low current	V_{IN}, V_{EN} = L			-10	μA
$I_{IN\,H}$, $I_{EN\,H}$	Input High current	V_{IN}, V_{EN} = H		30		μA
LOGIC CONTROL TO POWER DRIVE TIMING						
t_1 (V_i)	Source current turn-off delay	Fig. 12		300		ns
t_2 (V_i)	Source current fall time	Fig. 12		200		ns
t_3 (V_i)	Source current turn-on delay	Fig. 12		400		ns
t_4 (V_i)	Source current rise time	Fig. 12		200		ns
t_5 (V_i)	Sink current turn-off delay	Fig. 13		300		ns
t_6 (V_i)	Sink current fall time	Fig. 13		200		ns
t_7 (V_i)	Sink current turn-on delay	Fig. 13		400		ns
t_8 (V_i)	Sink current rise time	Fig. 13		200		ns

(*) Limited by power dissipation
(**) In synchronous rectification the drain-source voltage drops V_{DS} is shown in Fig. 4.

Fig. 1 - Typical I_s normalized vs. T_j

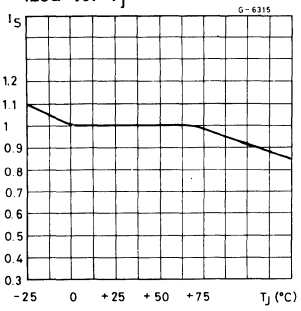


Fig. 2 - Quiescent current vs. frequency

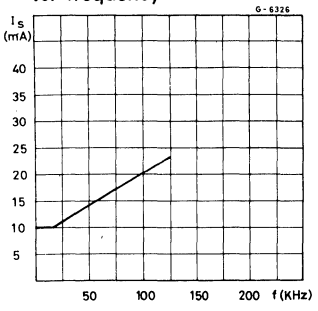


Fig. 3 - Typical I_s normalized vs. V_s

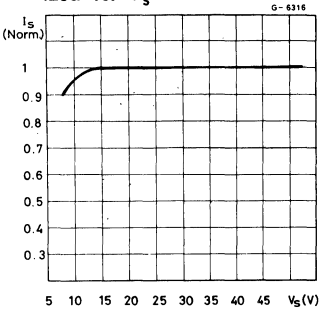


Fig. 4 - Typical diode behaviour in synchronous rectification

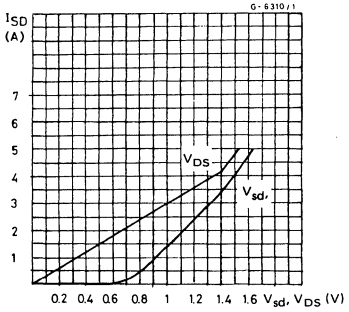


Fig. 5 - Typical $R_{DS\ (ON)}$ vs. $V_s \cong V_{ref}$

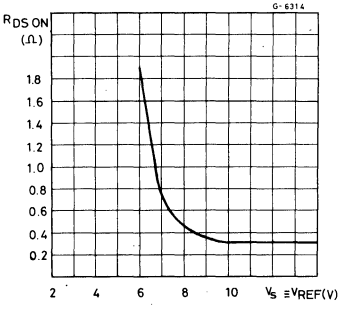


Fig. 6 - $R_{DS\ (ON)}$ normalized at 25°C vs. temperature typical values

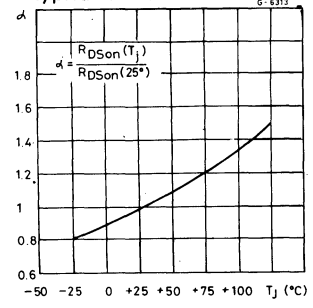


Fig. 7 - $R_{DS\ (ON)}$ vs. DMOS transistor current

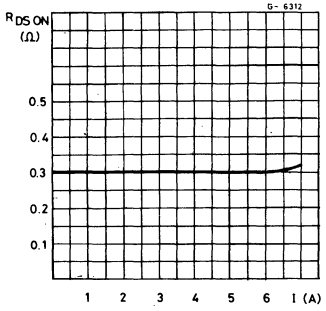


Fig. 8 - Typical power dissipation vs. I_L

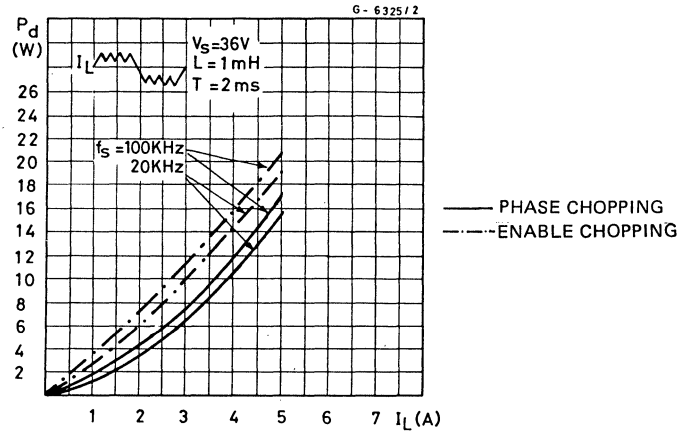


Fig. 8a - Two phase chopping

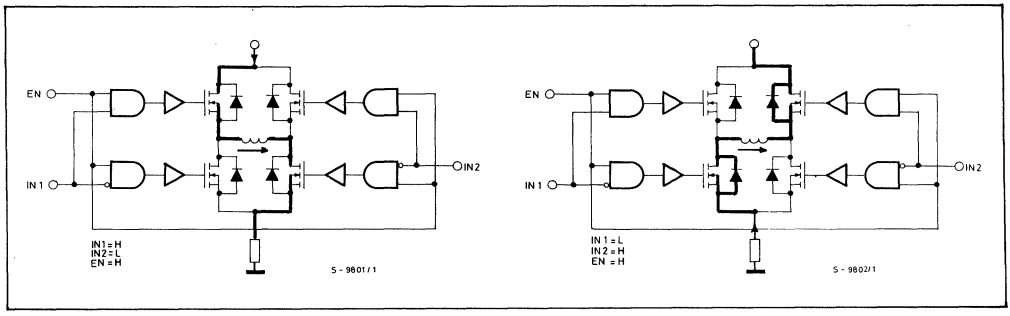


Fig. 8b - One phase chopping

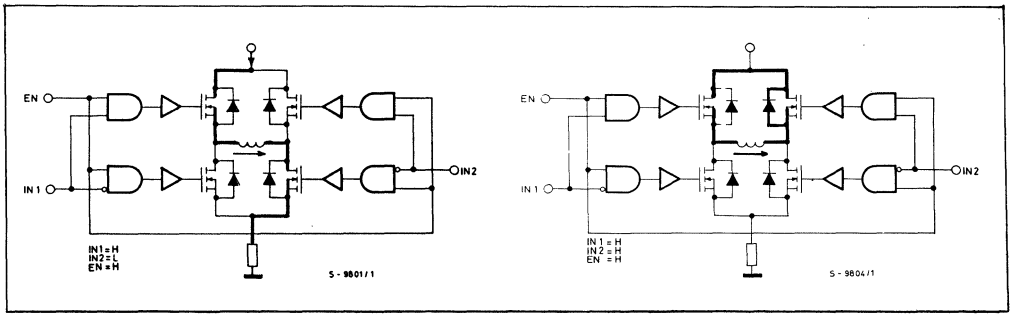
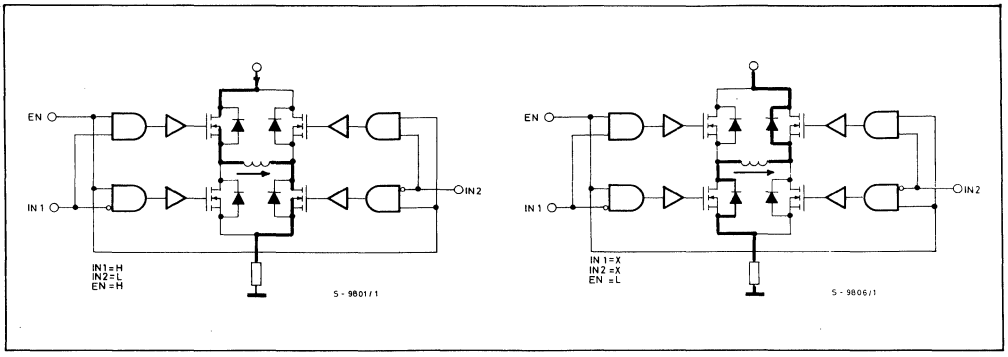


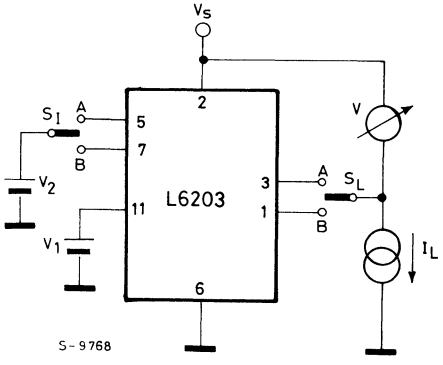
Fig. 8c - Enable chopping



TEST CIRCUITS

Fig. 9 - Saturation voltage

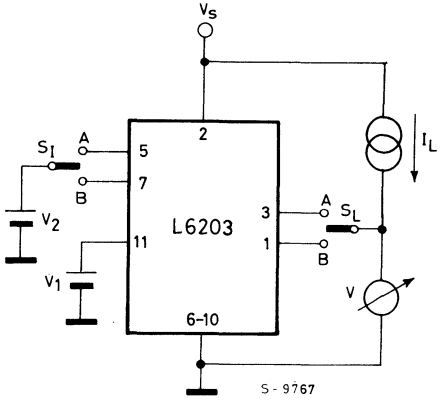
a) Source outputs



For IN1 source output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "H"

For IN2 source output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "H"

b) Sink outputs



For IN1 sink output saturation : V_1 = "H", S_I = A, S_L = A } V_2 = "L"

For IN2 sink output saturation : V_1 = "H", S_I = B, S_L = B } V_2 = "L"

TEST CIRCUITS (continued)

Fig. 10 - Quiescent current

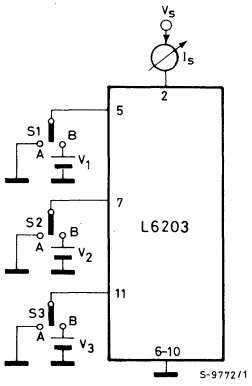
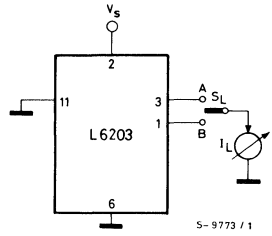
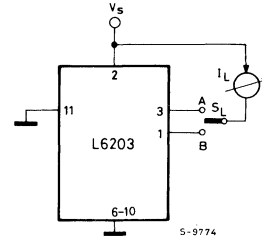


Fig. 11 - Leakage current

a) Source outputs



b) Sink outputs



SWITCHING TIMES

Fig. 12 - Source current delay times vs. input chopper

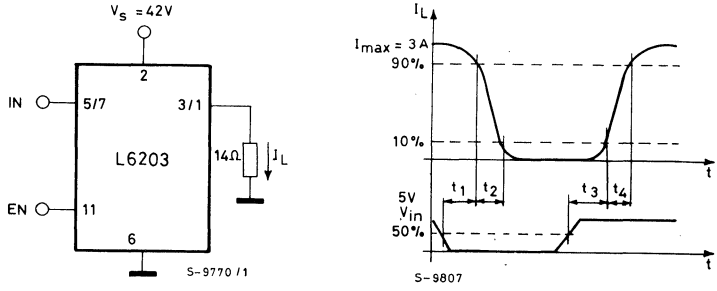
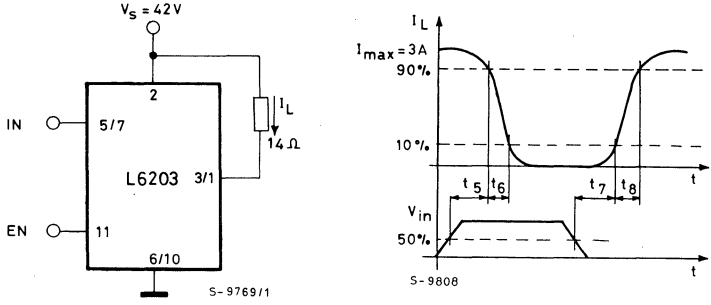


Fig. 13 - Sink current delay times vs. input chopper



CIRCUIT DESCRIPTION

The L6203 is a monolithic full bridge switching motor driver realized in the new Multipower-BCD technology which allows the integration of multiple, isolated DMOS power transistors plus mixed CMOS/bipolar control circuits. In this way it has been possible to make all the control inputs TTL, CMOS and μC compatible and eliminate the necessity of external MOS drive components.

LOGIC DRIVE

INPUTS			OUTPUT MOSFETS (*)
	IN1	IN2	
V_{EN} = H	L	L	Sink 1, Sink 2
	L	H	Sink 1, Source 2
	H	L	Source 1, Sink 2
	H	H	Source 1, Source 2
V_{EN} = L	X	X	All transistors turned OFF

L = Low H = High X = Don't care

(*) Members referred to INPUT 1 or INPUT2 controlled outputs stages

CROSS CONDUCTION

Although the device guarantees the absence of cross-conduction, the presence of the intrinsic diodes in the POWER DMOS structure causes the generation of current spikes on the sensing terminals. This is due to charge-discharge phenomena in the capacitors C1 & C2 associated with the drain source junctions (Fig. 14). When the output switches from high to low, a current spike is generated associated with the capacitor C1. On the low-to-high transition a spike of the same polarity is generated by C2, preceded by a spike of the opposite polarity due to the charging of the input capacity of the lower POWER DMOS transistor. (Fig. 15)

Fig. 14 - Intrinsic structures in the POWER MOS transistors

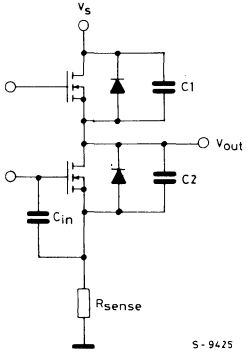
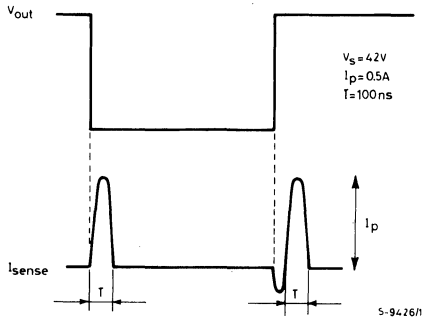


Fig. 15 - Current typical spikes on the sensing pin



TRANSISTOR OPERATION

ON STATE

When one of the POWER DMOS transistor is ON it can be considered as a resistor $R_{DS(ON)}$ (= 0.3Ω) throughout the recommended operating range. In this condition the dissipated power is given by:

$$P_{ON} = R_{DS(ON)} \cdot I_{DS}^2$$

The low $R_{DS(ON)}$ of the Multipower-BCD process can provide high currents with low power dissipation.

OFF STATE

When one of the POWER DMOS transistor is OFF the V_{DS} voltage is equal to the supply voltage and only the leakage current I_{DSS} flows. The power dissipation during this period is given by:

$$P_{OFF} = V_s \cdot I_{DSS}$$

The power dissipation is in the order of pW and is negligible in comparison to that dissipated in the ON STATE.

TRANSITIONS

Like all MOS power transistors the DMOS POWER transistors have as intrinsic diode between their source and drain that can operate as a fast freewheeling diode in switched mode

applications. During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\ (ON)}\ I_D$ and when the voltage reaches the diode voltage it is clamped to its characteristic. When the ENABLE input is low, the POWER MOS is OFF and the diode carries all of the recirculation current. The power dissipated in the transitional times in the cycle depends upon the voltage and current waveforms in the application.

$$P_{trans.} = I_{DS}(t) \cdot V_{DS}(t)$$

BOOSTRAP CAPACITORS

To ensure that the POWER DMOS transistors are driven correctly gate source voltage of about 10V must be guaranteed for all of the N-channel DMOS transistors. This is no problem for the lower POWER DMOS transistors as their sources are refered to ground but a gate voltage greater than the supply voltage is necessary to drive the upper transistors. In the L6203 this achieved by an internal charge pump circuit that guarantees correct DC drive in combination with the boostrap circuit charges the external C_B capacitors when the source transistor is OFF and the sink transistor is ON giving lower commutation losses in switched mode operation. For efficient charging the value of the boostrap capacitor should be greater than the input capacitance of the power transistor which is around 1nF. It is recommended that a capacitance of at least 10nF is used for the bootstrap. If a smaller capacitor is used there is a risk that the POWER transistors will not be fully turned on and they will show a higher $R_{DS\ (ON)}$. On the other hand if a elevated value is used it is possible that a current spike may be produced in the sense resistor.

REFERENCE

To stabilise the internal drive circuit it is recommended that a capacitor be placed between this pin and ground. A value of 0.22μF should be sufficient for most applications.

This pin is also protected against a short circuit to ground.

DEAD TIME

To protect the device against simultaneous conduction in both arms of the bridge and the resulting rail to rail short, the logic control circuit provides a dead time greater than 40ns.

THERMAL PROTECTION

A thermal protection circuit has been included that will disable the device if the junction temperature e reaches 150°C. When the temperature has fallen to a safe level the device restarts under the control of the input and enable signals.

APPLICATION INFORMATION

RECIRCULATION

During recirculation with the ENABLE input high, the voltage drop across the transistor is $R_{DS\ (ON)} \cdot I_L$ for voltages less than 0.7V and is clamped at a voltage depending on the characteristics of the source-drain diode for greater voltages. Although the device is protected against cross conduction, current spikes can appear on the current sense pin due to charge/discharge phenomena in the intrinsic source drain capacitances. In the application this does not cause any problems because the voltage created across the sense resistor is usually much less than the peak value, although a small RC filter can be added if necessary.

POWER DISSIPATION

In order to achieve the high performance provided by the L6203 some attention must be paid to ensure that it has an adequate PCB area to dissipate the heat. The first stage of any thermal design is to calculate the dissipated power in the application, for this example the half step operation shown in figure 16 is considered.

RISE TIME T_r

When an arm of the half bridge is turned on current begins to flow in the inductive load until the maximum current I_L is reached after a time T_r. The dissipated energy $E_{OFF/ON}$ is in this case:

$$E_{OFF/ON} = [R_{DS\ (ON)} \cdot I_L^2 \cdot T_r] \cdot 2/3$$

ON TIME T_{ON}

During this time the energy dissipated is due to the ON resistance of the transistors E_{ON} and the commutation E_{COM}. As two of the POWER DMOS transistors are ON E_{ON} is given by:

$$E_{ON} = I_L^2 \cdot R_{DS(ON)} \cdot 2 \cdot T_{ON}$$

In the commutation the energy dissipated is:

$$E_{COM} = V_s \cdot I_L \cdot T_{COM} \cdot f_{SWITCH} \cdot T_{ON}$$

Where:

T_{COM} = Commutation Time and it is assumed that;
$T_{COM} = T_{TURN-ON} = T_{TURN-OFF} = 100ns$
f_{SWITCH} = Chopper frequency

FALL TIME T_f

For this example it is assumed that the energy dissipated in this part of the cycle takes the same form as that shown for the rise time:

$$E_{ON/OFF} = [R_{DS(ON)} \cdot I_L^2 \cdot T_f] \cdot 2/3$$

QUIESCENT ENERGY

The last contribution to the energy dissipation is due to the quiescent supply current and is given by:

$$E_{QUIESCENT} = I_{QUIESCENT} \cdot V_s \cdot T$$

TOTAL ENERGY PER CYCLE

$$E_{TOT} = E_{OFF/ON} + E_{ON} + E_{COM} + E_{ON/OFF} + E_{QUIESCENT}$$

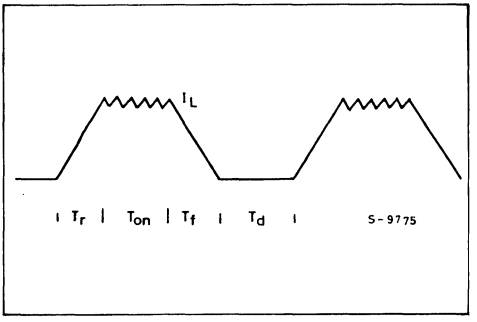
The Total Power Dissipation P_{DIS} is simply:

$$P_{DIS} = E_{TOT}/T$$

T_r = Rise time
T_{ON} = ON time
T_f = Fall time
T_d = Dead time
T = Period

$$T = T_r + T_{ON} + T_f + T_d$$

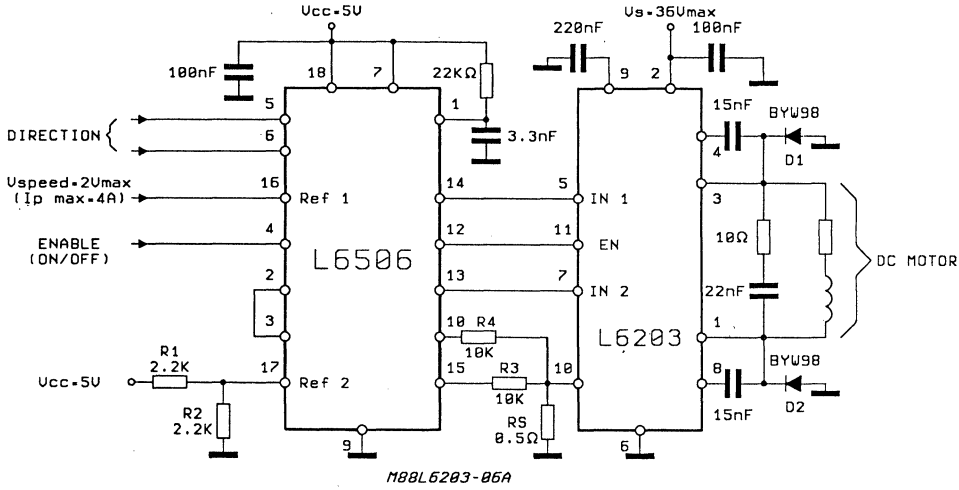
Fig. 16



DC MOTOR SPEED CONTROL

Since the L6203 integrates a full H-Bridge in a single package it si idealy suited for controlling small DC motors. When used for DC motor control the L6203 provides the power stage required for both speed and direction control. The L6203 can be combined with a current regulator like the L6506 to implement a transconductance amplifier for speed control, as shown in figure 17.
In this configuration the L6506 sense the voltage across the sense resistor, R_{SENSE}, to monitor the motor current. The L6506 then compares the sensed voltage to control the speed or during the input signals to the L6203.
Between the sense resistor and each sense input of the L6506 a resistor must be foreseen; if the connections between the outputs of the L6506 and the inputs of the L6202 need a long path, a resistor must be connected between each input of the L6202 and ground.
A snubber network made by the series of R and C must be foreseen very near to the outputs pins of the L6203.
The following formulas can be used :
$R \cong V_s/I_p$
$C = I_p/(dv/dt)$ where
V_s is the max supply voltage foreseen on the application;
I_p is the peak of the load current;
dv/dt is the needed rise time of the output voltage (200V/μsec is generally used).
A diode (BYW98) is connected between each power output pin and ground as well.
If the power supply cannot sink current, a suitable large capacitance must be used and connected near the supply pin of the L6202.
Sometimes a capacitor at pin 17 of the L6506 let application better work.

Fig. 17 - Bidirectional DC motor control



BIPOLAR STEPPER MOTORS APPLICATIONS

Bipolar stepper motors can be driven with an L297 or L6506, two L6203 bridge BCD drivers and very few external components. Together these three chips form a complete microprocessor-to-stepper motor interface.
As shown in Fig. 18 and Fig. 19, the controller connect directly to the two bridge BCD drivers. External component requirements are minimal: an RC network to set the chopper frequency, a resistive divider to establish the comparator reference voltage (pin 15 for L297, pin 10 and 15 for L6506) and a snubber network made by R and C in series.
The following formulas can be used :

$R \simeq V_s/I_p$
$C = I_p/(dv/dt)$ where V_s is the max. Supply Voltage foreseen on the application;
I_p is the peak of the load current;
dv/dt is the needed rise time of the output voltage (200V/μs is generally used). Depending on the Printed Circuit Board design, a resistor between each input of the L6203 and ground could be requested. These solutions have a very high efficiency because of low power dissipation.

HIGH CURRENT MICROSTEP DRIVE FOR STEPPER MOTORS

The L6203 can be used in conjunction with the L6217 to (figure 20) implement a high current microstepping controller for stepper motors.

In this application the L6217 is used as a control circuit and its outputs are used only to drive the inputs of the L6203. The application allows easy interface to a microprocessor since the L6217 may be connected directly to the microprocessor bus.

In the circuit shown in Figure 20, the L6217 senses the motor current by monitoring the voltage across the sense resistors, R_{SENSE}, and compares this value to the output of a 6 bit (7 bit if the L6217A is used) D to A Converter. The L6217 controls the current using a frequency modulated, constant off time, switching controller. The off time of each coil may be set using and external resistor and capacitor connected to PTA and PTB.

In this configuration the microprocessor simply loads the appropriate value for the direction of current flow through the coil and the data for the DAC into the L6217. The L6217 and L6203 then forms the complete interface between the micro and the motor.

When the pins 3 and 4 of the L6217 (Test A and B) are low, the bridges must be in tri-state condition.
For this reason two LM339 comparators must be used. The outputs of the comparators act on the enable inputs of the L6203 ICs.
A bilevel operation can be used for decreasing the minimum controllable load current. The mi-

nimum current that can be controlled is given by the following expression :

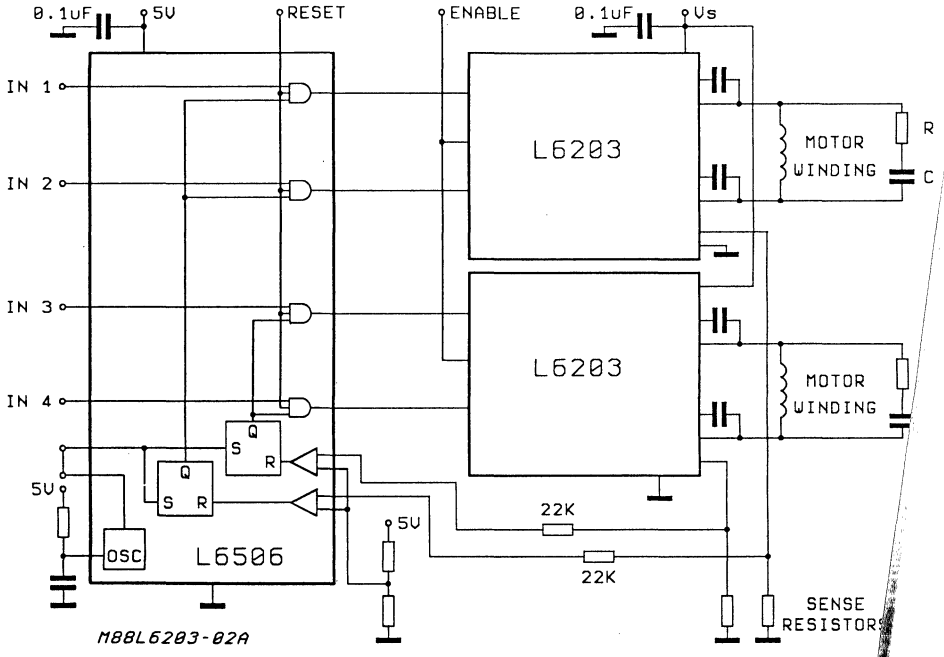
$$I_L \text{ (avg.)} = \frac{V_s}{R_{sense} + (2R_{DSon} + R_{LOAD})/DC}$$

where R_{LOAD} is the equivalent resistance of the load DC is the duty cycle given by

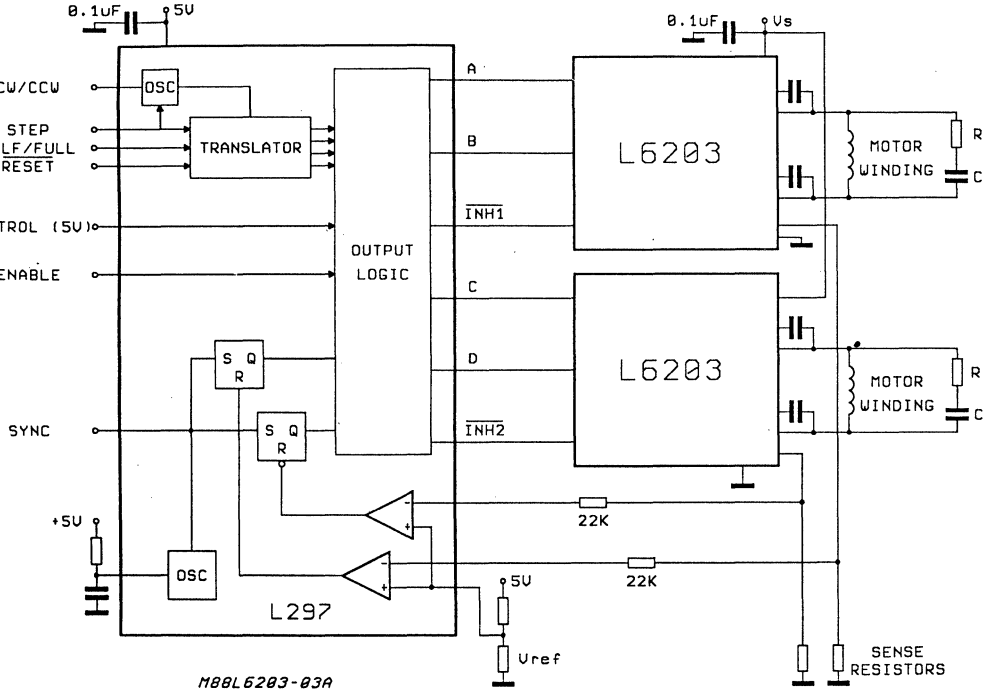
$$\frac{T_{on}}{T_{on} + T_{off}}$$

If 12V is forced on pin (Reference voltage) a the supply voltage V_s is reduced below 12V t on resistance tends to increase above the norm guaranteed 0.3ohm.
Consequently the minimum current will also reduced, as given in the above expression. Wher minimum current operation is required, a high gnal at point (A) can disable the pnp transisto in fig. 20. So it's possible to operate at a V_s (7V - V_{BE}).

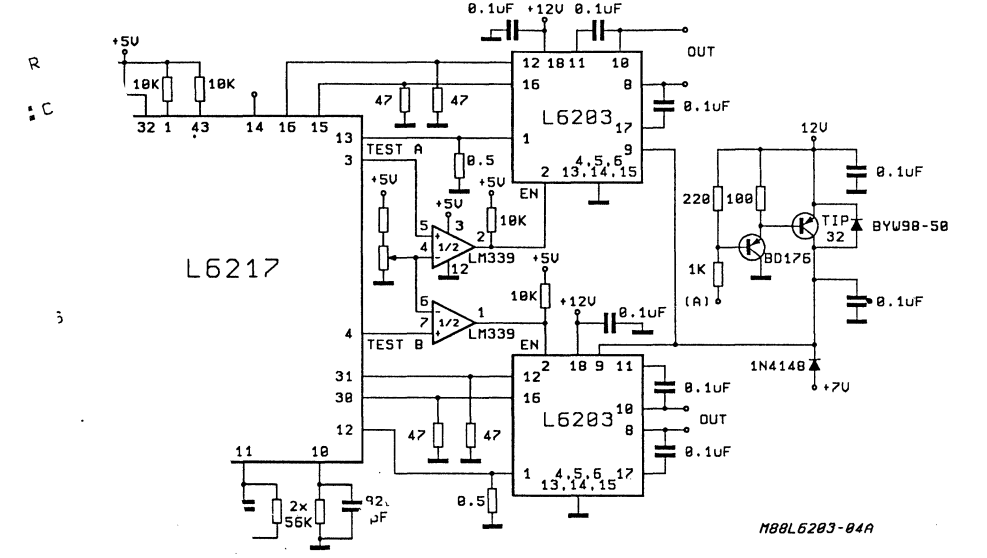
Fig. 18 - Two phase Bipolar stepper motor control circuit with chopper current control



g. 19 - Two phase Bipolar stepper motor control circuit with chopper current control and translator



gh current microstepping controller for stepper motors



THERMAL CHARACTERISTICS

Fig. 21 - $R_{th\ j\text{-}amb}$ of Multiwatt package vs. dissipated power

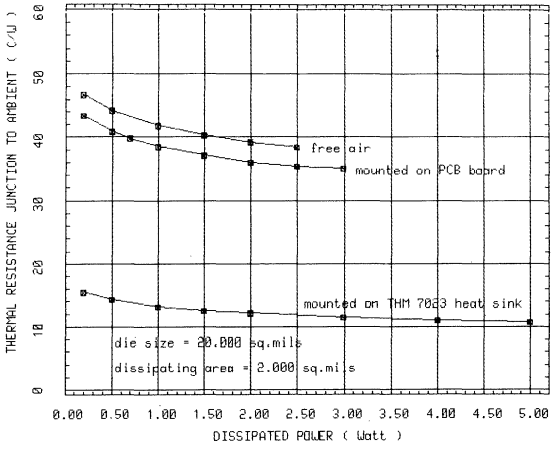
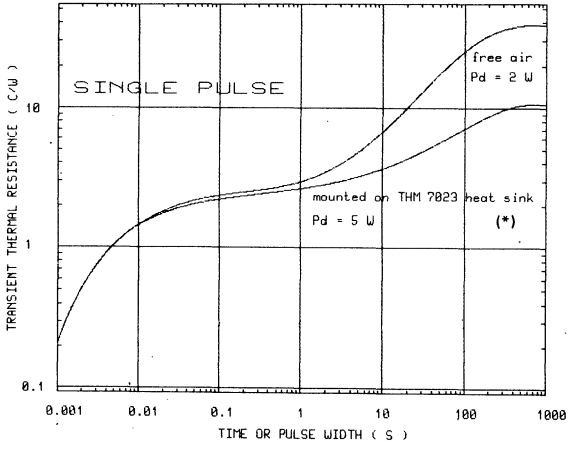
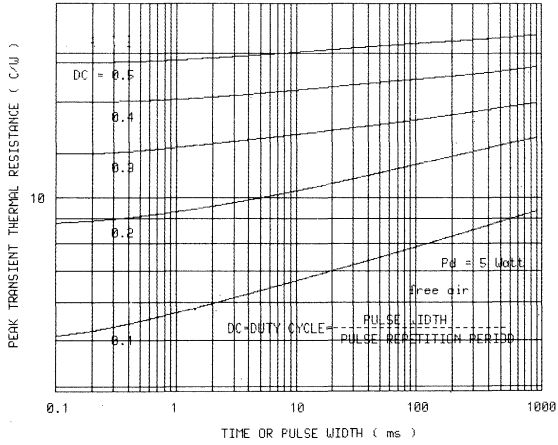


Fig. 22 - Comparison of transient R_{th} for single pulses with and without heatsink



(*) $R_{th} \cong 9°C/W$

g. 23 - Peak transient R_{th} vs. pulse width and duty cycle



SGS-THOMSON MICROELECTRONICS

L6210

DUAL SCHOTTKY DIODE BRIDGE

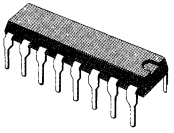
- MONOLITHIC ARRAY OF EIGHT SCHOTTKY DIODES
- HIGH EFFICIENCY
- 4A PEAK CURRENT
- LOW FORWARD VOLTAGE
- FAST RECOVERY TIME
- TWO SEPARATED DIODE BRIDGES

The L6210 is a monolithic IC containing eight Schottky diodes arranged as two separated diode bridges.

This diodes connection makes this device versatile in many applications.

They are used particular in bipolar stepper motor applications, where high efficient operation, due to low forward voltage drop and fast reverse recovery time, are required.

The L6210 is available in a 16 Pin Powerdip Package (12+2+2) designed for the 0 to 70°C ambient temperature range.



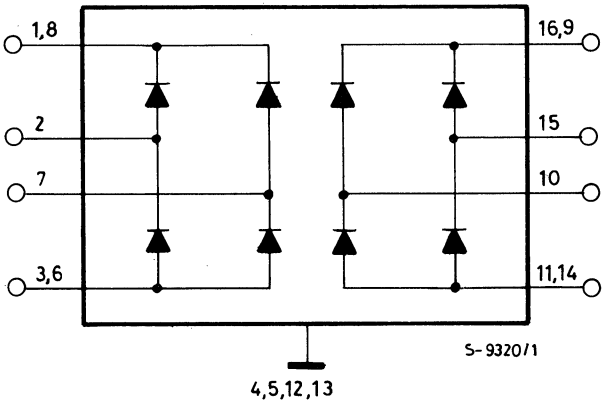
Powerdip 12+2+2

ORDERING NUMBER: L6210

ABSOLUTE MAXIMUM RATINGS

I_f	Repetitive forward current peak	2	A
V_r	Peak reverse voltage (per diode)	50	V
T_{amb}	Operating ambient temperature	70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

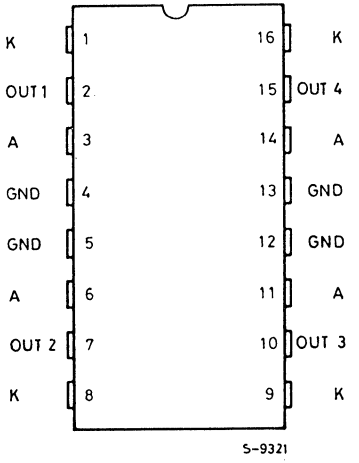
BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal impedance junction-case	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal impedance junction-ambient without external heatsink	max	65	°C/W

CONNECTION DIAGRAM
(Top view)



ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_f	Forward voltage drop	I_f = 100mA		0.65	0.8	V
		I_f = 500mA		0.8	1	
		I_f = 1A		1	1.2	
I_L	Leakage current	V_R = 40V T_{amb} = 25°C			1	mA

NOTE: At forward currents of greater than 1A, a parasitic current of approximately 10 mA may be collected by adiacent diodes.

Fig. 1 - Reverse current vs. voltage

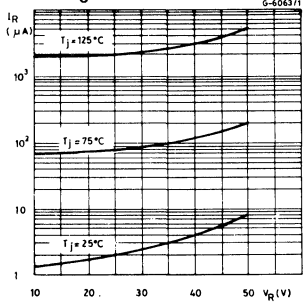
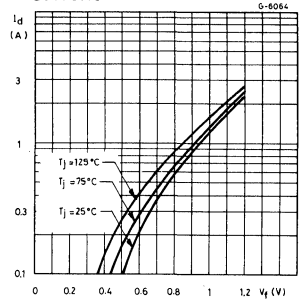


Fig. 2 - Forward voltage vs. current



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the L6210 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board as shown in figure 3 or to an external heatsink (Figure 4).

During soldering the pin temperature must not exceed 260°C and the soldering time must not be longer then 12s. The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 3 - Example of P.C. board copper area which is used as heatsink

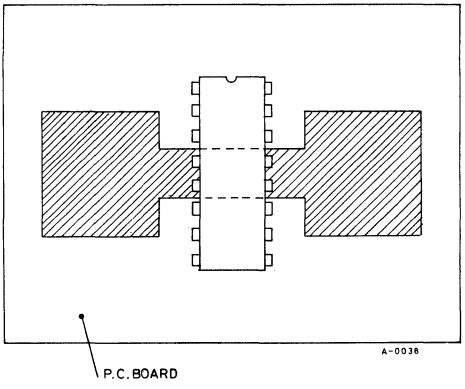
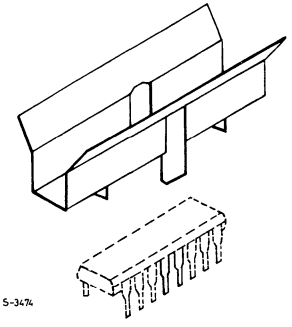


Fig. 4 - Example of an external heatsink



HIGH CURRENT SOLENOID DRIVER

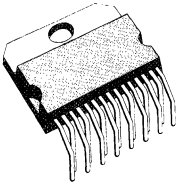
PRELIMINARY DATA

- HIGH VOLTAGE OPERATION (UP TO 50 V)
- HIGH OUTPUT CURRENT CAPABILITY (UP TO 6 A)
- LOW SATURATION VOLTAGE
- TTL-COMPATIBLE INPUT
- OUTPUT SHORT CIRCUIT PROTECTION (TO GROUND, TO SUPPLY AND ACROSS THE LOAD)
- THERMAL SHUTDOWN
- OVERDRIVING PROTECTION
- LATCHED DIAGNOSTIC OUTPUT

DESCRIPTION

The L6212 is a monolithic switch-mode solenoid driver designed for fast, high-current applications such as hammer driving in printers and electronic typewriters. Power dissipation is reduced by efficient switch-mode operation. An extra feature of the L6212 is a latched diagnostic output which indicates when the output is short circuit.

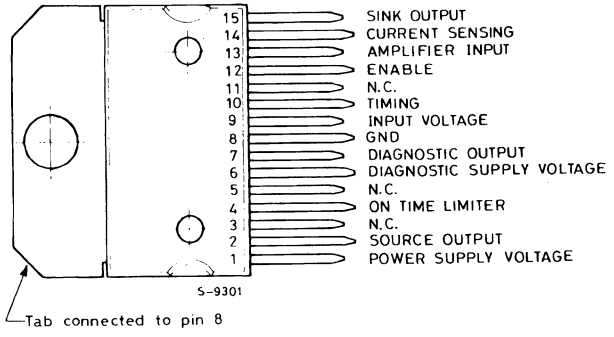
The L6212 is supplied in an 15-lead Multiwatt plastic power package.



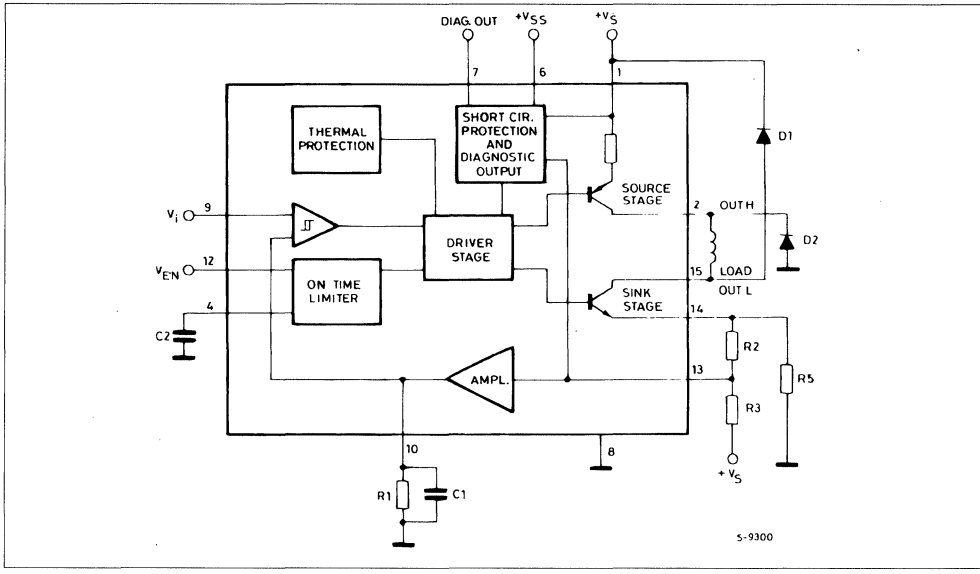
Multiwatt-15
(Horizontal)

ORDER CODE : L6212

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Power Supply Voltage	50	V
V_{ss}	Logic Supply Voltage	7	V
V_{EN}	Enable Voltage	7	V
V_I	Input Voltage	7	V
I_p	Peak Output Current (repetitive)	6.5	A
P_{tot}	Total Power Dissipation (at T_{case} = 75 °C)	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Themal Resistance Junction-ambient	Max	35	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_s = 37 V, V_{ss} = 5 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Power Supply Voltage (pin 1)		12		46	V
I_d	Quiescent Drain Current	V_{EN} = H		20	30	mA
		$V_i \geq 0.6$ V V_{EN} = L		70		mA
V_{ss}	Logic Supply Voltage (pin 6)		4.5		7	V
I_{ss}	Quiescent Logic Supply Current	V_{DIAG} = L		5	8	mA
		DIAG Output at High Impedance		10	100	µA
V_i	Input Voltage (pin 9)	Operating Output	0.6			V
		Non-operative Output			0.45	V
I_i	Input Current (pin 9)	$V_i \geq 0.6$ V			–2	µA
		$V_i \leq 0.45$ V			–5	µA
V_{ENABLE}	Enable Input Current (pin 12)	Low Level	–0.3		0.8	V
		High Level	2.4			
I_{ENABLE}	Enable Input Current	V_{EN} = L V_i = 0.8 V			–100	µA
		V_{EN} = H V_e = 2.4 V			100	
$V_{sat\ H}$	Source Output Saturation Volt.	I_p = 5.5 A			2.5	V
$V_{sat\ L}$	Sink Output Saturation Volt.	I_{out} = 5.5 A			2.5	V
$V_{sat\ H} + V_{sat\ L}$	Total Saturation Voltage	I_{out} = 5.5 A			4.5	V
$I_{leakage}$	Output Leakage Current Source PNP	V_s = 45 V $V_i \leq 0.45$ V			2	mA
$I_{leakage}$	Output Leakage Current Sink NPN	V_s = 45 V $V_i \leq 0.45$ V			2	mA
K	On Time Limiter Constant (*)	V_{EN} = L		120		
V_{DIAG}	Diagnostic Saturation Voltage (pin 7)	I_{DIAG} = 10 mA			0.4	V
I_{DIAG}	Diagnostic Leakage Current (pin 7)	V_{DIAG} = 40 V			10	µA
$\frac{V_{pin\ 10}}{V_{pin\ 13}}$	OP AMP DC Voltage Gain	$V_{pin\ 13}$ = 100 to 800 mV		5		
$V_{pin\ 10}$		$I_{pin\ 10}$ = 1 mA	4.5			V
$I_{pin\ 10}$		$V_{pin\ 10}$ = 4 V $V_9 = V_{13} = 0$			10	µA
		$V_{pin\ 10}$ = 2 V V_{13} = 0.9 V	1		1.5	mA
I_{sense}	Input Bias Current (pin 13)			–1		µA
V_{sense}	Sensing Voltage (pin 14) (**)				0.9	V

(*) After a time interval $t_{max} = KC_2$, the output stages are disabled.
(**) Allowed range of V_{sense} without the intervention of the short circuit protection.

Figure 1 : Output Current Waveforms.

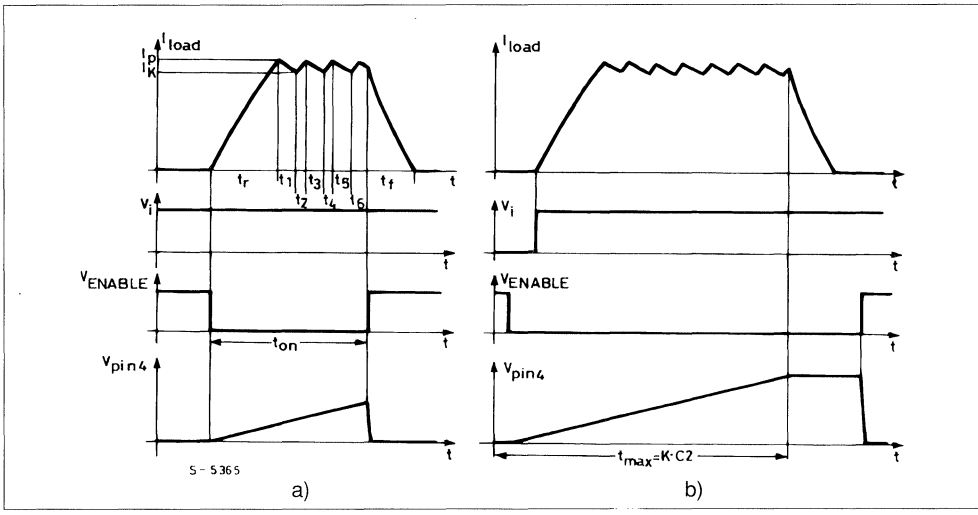
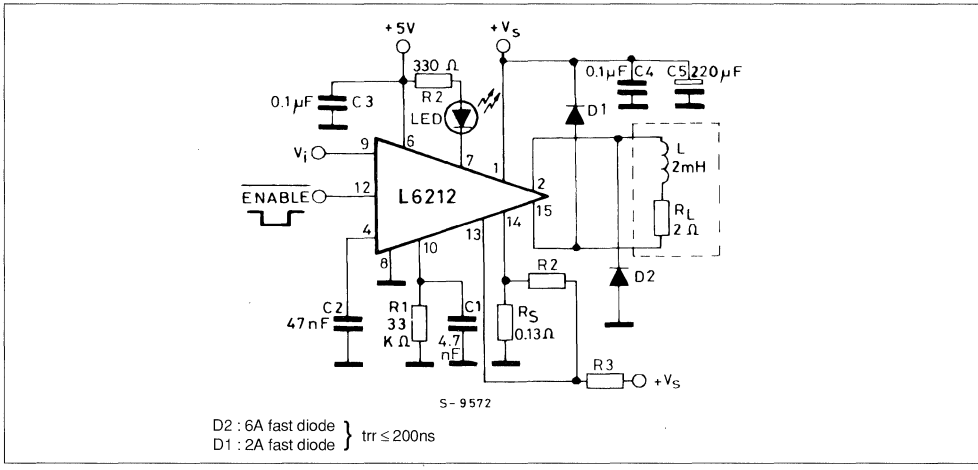


Figure 2 : Test and Typical Application Circuit.



CIRCUIT OPERATION

The L6212 works as a transconductance amplifier : it can supply an output current directly proportional to an input voltage level (V_i). Furthermore, it allows complete switching control of the output current waveform (see Fig. 1).

The following explanation refers to the Block Diagram, to Fig. 1 and to the typical application circuit of Fig. 2.

The t_{on} time is fixed by the width of the Enable input signal (TTL compatible) : it is active low and enables the output stages "source" and "sink". At the end of t_{on}, the load current I_{load} recirculates through D1 and D2, allowing fast current turn-off.

The rise time t_r depends on the load characteristics, on V_I and on the supply voltage value (V_s, pin 1).

During the t_{on} time I_{load} is converter into a voltage signal by means of the external sensing resistance R_s connected to pin 13. This signal, amplified by the op amp charges the external RC network at pin 10 (R1, C1). The voltage at this pin is sensed by the inverting input of a comparator. The voltage on the non-inverting input of this one is fixed by the external voltage V_i (pin 9).

After, t_r, the comparator switches and the output stage "source" is switched off. The comparator output is confirmed by the voltage on the non-inverting input, which decreases of a constant fraction of V_i (1/10), allowing hysteresis operation. The current in the load now flows through D2.

Two cases are possible : the time constant of the recirculation phase is higher than R1, C1 ; the time constant is lower than R1, C1. In the first case, the voltage sended on the non-inverting input of the comparator is just the value proportional to I_{load}. In the second case, when the current decreases too quickly, the comparator senses the voltage signal stored in the R1, C1 network.

In the first case t_1 depends on the load characteristics, while in the second case it depends only on the value of R1, C1.

In the other word, R1, C1 fixed the minimum value of t_1 ($t_1 \geq 1/10$ R1 x C1. Note that C1 should be chosen in the range 2.7 to 10 nF for stability reasons of the op amp).

After t_1, the comparator switches again : the output is confirmed by the voltage on the non-inverting input, which reaches V_i again (hysteresis).

Now the cycle starts again : t_2, t_4 and t_6 have the same characteristics as t_r, while t_3 and t_5 are similar to t_1. The peak current I_p depends on V_i as shown in the typical transfer function of Fig. 3.

It can be seen that for V_i lower than 450 mV the device is not operating.

For V_i included between 450 and 600 mV, the operation is not guaranteed.

The other parts of the device have protection and diagnostic functions. At pin 4 is connected an external capacitor C2, charged at constant current when the Enable is low.

After time interval equal to K · C1 (K is defined in the table of Electrical Characteristics and has the dimensions of Ω) the output stages are switched off independently by the Input signal.

This avoids the load being driven in construction for an excessive period of time (overdriving protection).

The action of this protection is shown in Fig. 1b. Note that the voltage ramp at pin 4 starts whenever the Enable signal becomes active (low state), regardless of the Input signal. To reset pin 4 and to restore the normal conditions, pin 12 must return high. This protection can be disabled by grounding pin 4.

In order to keep constant the energy delivered to the load, when the supply voltage changes, it's possible to modify the output maximum peak current (I_p) by means the external voltage divider R2 and R3 which "senses" the supply voltage.

I_p is given by :

$$I_p = \frac{V_i\,(R_s + R2 + R3) - 5\,V_s\,(R2 + R_s)}{5\,R3\,R_s}$$

so the variation of I_p versus V_s is :

$$\Delta I_p = -\frac{R2 + R_s}{R3\,R_s}$$

The thermal protection included in the L6212 has hysteresis.

It switches off the output stages whenever the junction temperature increases too much. After a fall of about 20°C, the circuit starts again.

Finally, the device is protected against any type of short circuit at the outputs : to ground, to supply and across the load.

When the source stage current is higher than 7A and/or when the pin 13 voltage is higher then 1 V (i.e. for a sink current greater than 1 V/R_s) the output stages are switched off and the device is inhibited.

This condition is indicated at the open-collector output DIAG (pin 7) ; internal flip-flop F/F changes and forces the output transistor into saturation. The F/F

must be supplied independently through V_{SS} (pin 6). The DIAG signal is reset and the output stages made operative by switching off the supply voltage at pin 1 and then by switching the device on again.

After that, two cases are possible : the reason for the "bad operation" is till present and the protection acts again ; the reason has been removed and the device starts to work properly.

Figure 3 : Peak Output Current vs. Input Voltage.

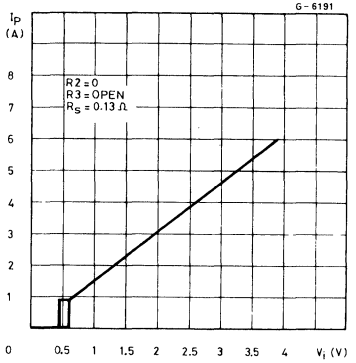


Figure 4 : Peak Output Current vs. Input Voltage.

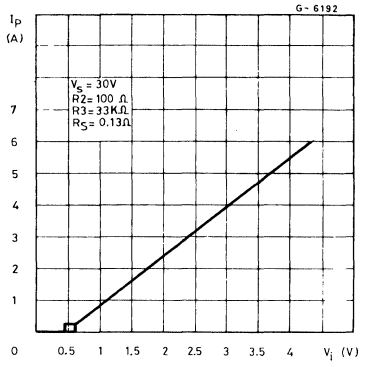
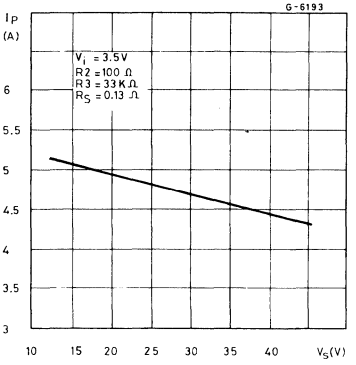


Figure 5 : Peak Output Current vs. Supply Voltage.



STEPPER MOTOR DRIVER

- MICROSTEPPING
- BIPOLAR OUTPUT CURRENT UP TO 400 mA
- LOW SATURATION VOLTAGE
- BUILT-IN FAST RECOVERY DIODES
- OUTPUT CURRENT DIGITALLY PROGRAMMABLE
- 6 BIT D/A CONVERTERS SET OUTPUT CURRENT
- THERMAL SHUTDOWN

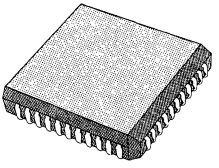
DESCRIPTION

The L6217 is a monolithic IC that controls and drives both phases of a Bipolar Stepper Motor with PWM control of the phase current. The output current level of each phase is programmed by a 6 bit D/A converter so that the device may be used in full-step, half-step and micro-step applications. The inputs for the D/A converters and the phase inputs to select the direction of current flow are latched to minimize the interface to a microprocessor.

The power section of the device is a dual H-Bridge drive with internal clamp diodes for current recirculation. To maintain the degree of accuracy required for micro-stepping the motor current is internally sensed and compared to the output of the D/A converter.

A monostable, programmed by an RC network sets the motor current decay time.

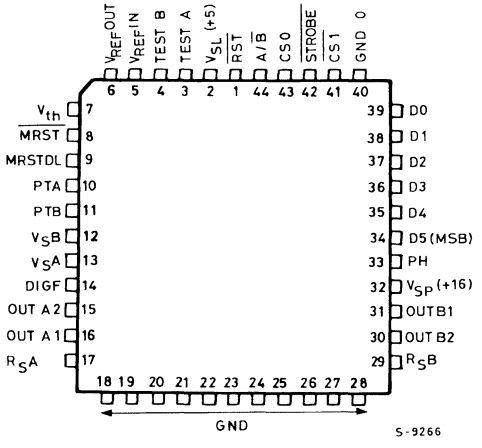
The L6217 is supplied in a 44 pin PLCC with 11 of the 44 pins used for heatsinking.



PLCC 44
(Plastic Chip-Carrier)

ORDER CODE : L6217

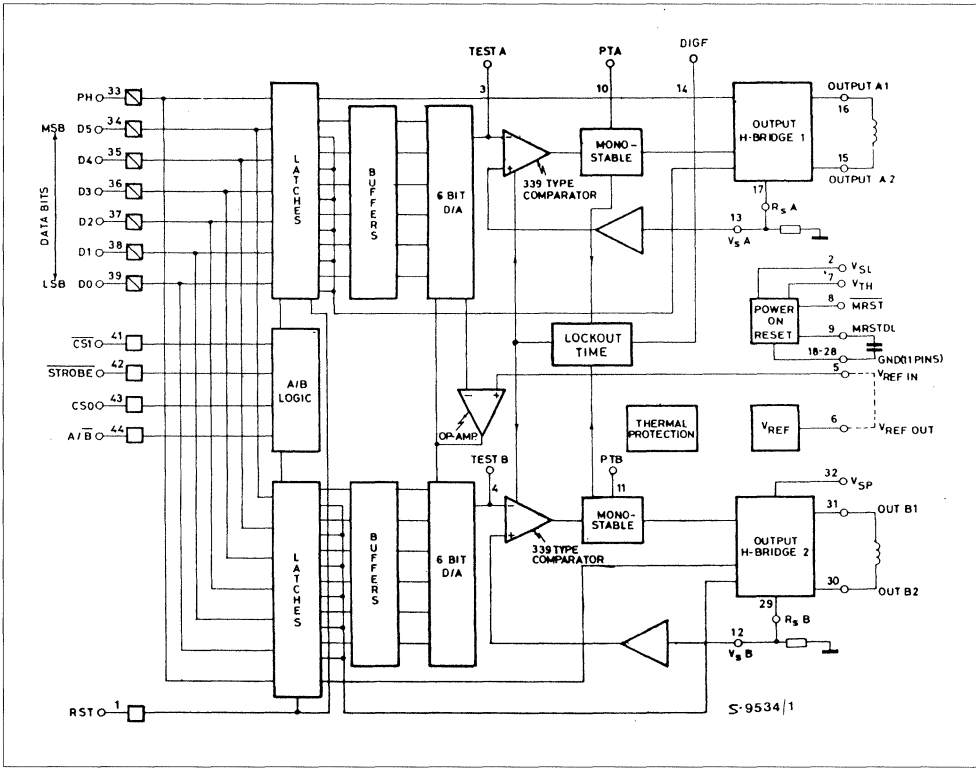
PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{si}	Logic Supply Voltage	7	V
V_{sp}	Motor Supply Voltage	18	V
V_i	Logic Input Voltage	6	V
V_{ref}	Reference Input Voltage	V_{si}	V
I_o	Output Peak Current	500	mA
T_j	Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Impedance Junction-Case	Max.	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal Impedance Junction-Ambient	Max.	80	°C/W

PIN FUNCTION DESCRIPTION

N°	Name	Function
1	$\overline{R_{st}}$	Active low input resets the D/A latches to 0 and disables the output.
38,39	D0 - D5	Data inputs for the D/A converter (D0 = LSB). For a data input of 00, the corresponding outputs are held in the off state.
44	A/B	Channel select for input data. Pin A/B selects channel A when high.
33	PH	Logic input selects direction of current flow in output bridge from A1 (B1) to A2 (B2) for PH = 1.
42	$\overline{\text{Strobe}}$	Active low input latches input data (D0-D5 and PH) into input latch.
9	MRST DL	The capacitor on this pin programs the power on reset delay according to the formula : $T_{DR} = (0.35)\ (C)\ 10^6$
8	MRST	Power-on reset circuit output. (micro reset signal). This output remains low from power on until the delay capacitor has charged past the delay threshold.
10	P_tA	Pulse time A, an external parallel RC network tied to ground defines T_{off} time for channel A. ($T_{off} = 0.69$ R2C2).
11	P_tB	Pulse time B, an external parallel RC network tied to ground defines toll time for channel B. ($T_{off} = 0.69$ R3C3).
5	$V_{ref\ In}$	Voltage applied to this point sets the reference for the D/A converter and threfore sets the maximum output current. (see equation 1, next two pages).
18 to 28	Gnd	Ground connection and also conducts heat to the P.C. board.
40	Gnd 0	Pin must be connected to ground.
2	V_{sl}	Logic Supply Voltage
32	V_{sp}	Motor Supply Voltage
16,15 31,30	Out A1 - A2 B1 - B2	H - Bridge outputs.
43,41	CS0, $\overline{CS1}$	Chip select inputs CS0 is active high, $\overline{CS1}$ is active low.
17,29	R_sA - R_sB	Sense resistor from this pin to ground set the peak output current.
13,12	V_sA - V_sB	Analog inputs for sensing motor current, separate inputs are provides to allow filtering of the sense voltage if required.
3,4	Test A & B	These pins are for testing of D/A outputs.
6	$V_{ref\ out}$	2.5 V band gap reference.
7	V_{th}	Reset Threshold Voltage
14	DIGF	Can be used to modify the internal comparator lockout time. In microstepping typical application a 1.8 KΩ resistor must be connected between this pin and ground.

ELECTRICAL CHARACTERISTICS (V_{cc} = 5.0 V, T_j = 25 °C unless otherwise specified noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{sp}	Motor Supply Voltage		8		16	V
V_{si}	Logic Supply Voltage		4.75		5.25	V

LOGIC INPUTS (D0-D6, CS0, $\overline{CS1}$, PH, $\overline{RST}$ and A/$\overline{B}$)

V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2		V_{si}	V
I_{IL}	Input Low Current	V_I = 0.4 V			– 400	µA
I_{IH}	Input High Current	V_I = 2.4 V			10	µA

CURRENT CONTROL AND D TO A SECTION

V_{ref}	Reference Voltage	V_{CC} = 5.0 V	2.45	2.50	2.55	V
V_{rin}	Reference Input Range		2.0		3.0	V
	Monotonicity of D to A		– 0.5		+ 0.5	LSB
	Linearity of D to A		– 1		+ 1	LSB
I_{op}	Peak Output Current (gain of current loop)	V_{ref} = 2.40 V R_{sense} = 2 Ω Data = 7 F (Hex)	225	252	277	mA
I_o	Output Matching	V_{ref} = 2.38 V			5	%

MONOSTABLE

T_{off}	Cutoff Time	R_t = 56 KΩ C_t = 820 pF	28		36	µs
T_d	Turn-off Delay			1		µs
I_{off}	Output Leakage Current	Data = 00 (Hex)			100	µA

RESET CIRCUITRY

V_{th}	Reset Threshold Voltage		3.9	4.1	4.3	V
	Reset Threshold Hysteresis		70	100		mV
I_{so}	Delay Capacitor Charging Current	V_C = 2.5 V	7	10	14	µA
I_{si}	Delay Capacitor Discharge Current	V_C = 2.5 V	10			mA
V_{dth}	Delay Threshold Voltage		3.25	3.5	3.75	V
V_{dhys}	Hysteresis Voltage on Delay Threshold		70	100		mV
I_{ol}	Output Leakage Current	V_O = 5 V			200	µA
V_{sat}	Output Saturation of Reset Out	I_O = 2 mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SOURCE DIODE - TRANSISTOR PAIRS						
V_{sat}	Saturation Voltage	I_O = 400 mA		1.3	1.8	V
V_f	Diode Forward Voltage	I_O = 400 mA		0.8	1.2	V
SINK DIODE - TRANSISTOR PAIRS						
V_{sat}	Saturation Voltage	I_O = 400 mA		1.1	1.5	V
V_f	Diode Forward Voltage	I_O = 400 mA		0.6	1.0	V
AC CHARACTERISTICS						
$T_sDI(ST)$	DI to Strobe ↓ Setup Time		100			ns
$T_hDI(ST)$	DI to Strobe ↓ Hold Time		500			ns
T_wPI	Pulse Width Low		600			ns
T_cST	Strobe Setup Time		2.5			µs
$T_sA/\overline{B}(ST)$	A/$\overline{B}$ to Strobe ↓ Setup Time		100			ns
$T_sPH(ST)$	PH to Strobe ↓ Setup Time		100			ns

CIRCUIT OPERATION

The current control section of the L6217A is a pulse width modulated control that senses the motor current. When the motor current reaches the peak programmed current the comparator will trigger the monostable turning off the upper transistors. After the t_{off} time equal to 0.69 RC the upper drivers are enabled again.

The peak current is given by the equation :

$$I_{op} = \frac{V_{ref}}{4.69 \cdot R_{sense}} \cdot \frac{D}{64}$$

D = Input data (0 - 63)

When the input data is 00, the ouptut stages are disabled by internal logic so that the output current decays rapidly to zero.

An internal generated lockout time avoids the use of an external RC network between the sensing resistor (R_SA, R_SB) and the corresponding input (V_SA, V_SB), by disabling the comparator sensing during the lockout time. This time is typically 2.5µs.

Figure 1 : Microstepping (typical application).

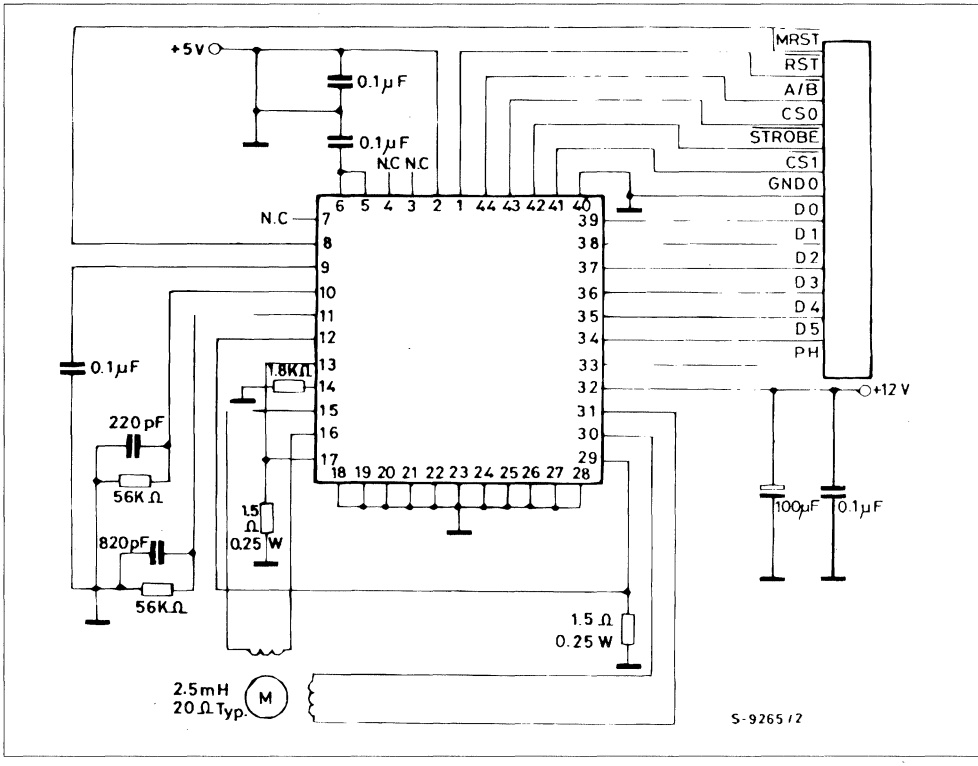


Figure 2 : Microcomputer Interface Timing.

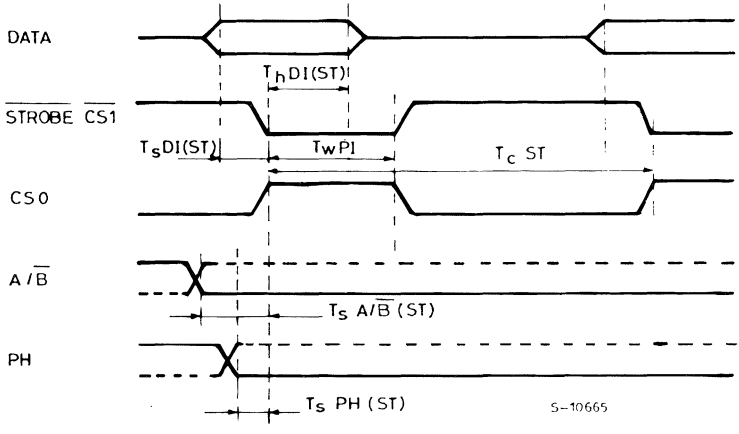


Figure 3 : T_d, T_{off} and $T_{lock\ out}$.

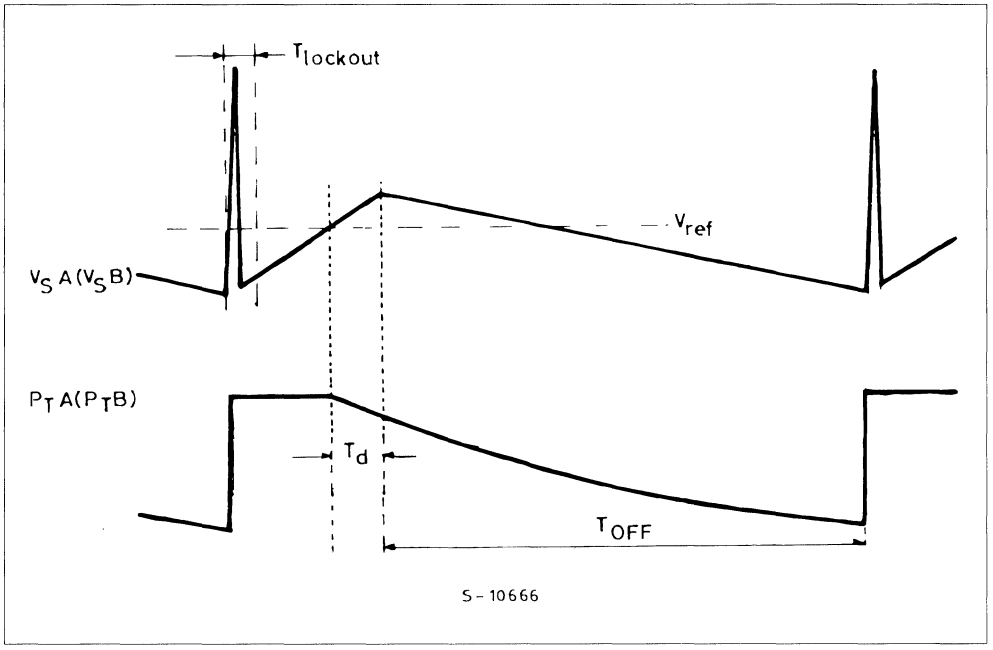
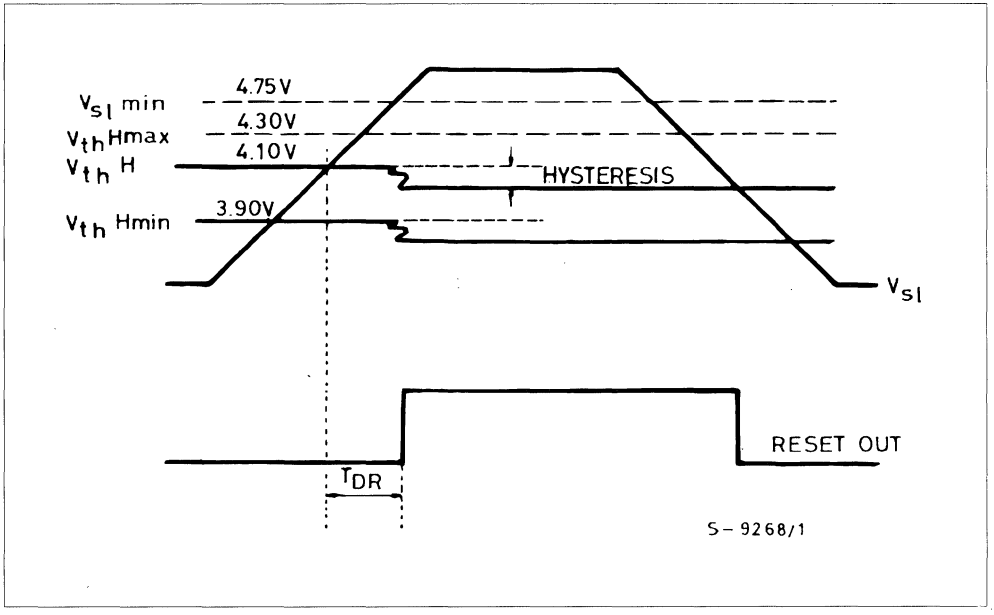


Figure 4 : Reset Waveforms.



L6217A

STEPPER MOTOR DRIVER

- MICROSTEPPING
- BIPOLAR OUTPUT CURRENT UP TO 400 mA
- LOW SATURATION VOLTAGE
- BUILT-IN FAST RECOVERY DIODES
- OUTPUT CURRENT DIGITALLY PROGRAMMABLE
- 7 BIT D/A CONVERTERS SET OUTPUT CURRENT
- THERMAL SHUTDOWN

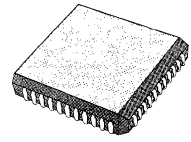
DESCRIPTION

The L6217A is a monolithic IC that controls and drivers both phases of a Bipolar Stepper Motor with PWM control of the phase current. The output current level of each phase is programmed by a 7 bit D/A converter so that the device may be used in full-step, half-step and micro-step applications. The inputs for the D/A converters and the phase inputs to select the direction of current flow are latched to minimize the interface to a microprocessor.

The power section of the device is a dual H-Bridge drive with internal clamp diodes for current circulation. To maintain the degree of accuracy required for microprostepping, the motor current is internally sensed and compared to the output of the D/A converter.

A monostable, programmed by and RC network sets the motor current decay time.

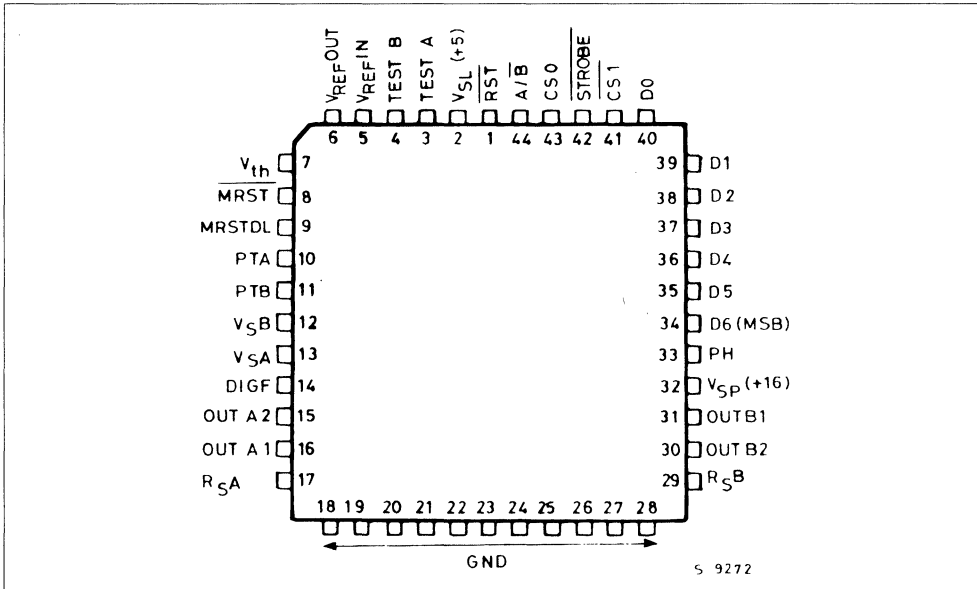
The L6217A is supplied in a 44 pin in PLCC with 11 of the 44 pins used for heatsinking.



PLCC 44
(Plastic Chip-Carrier)

ORDERING NUMBER : L6217A

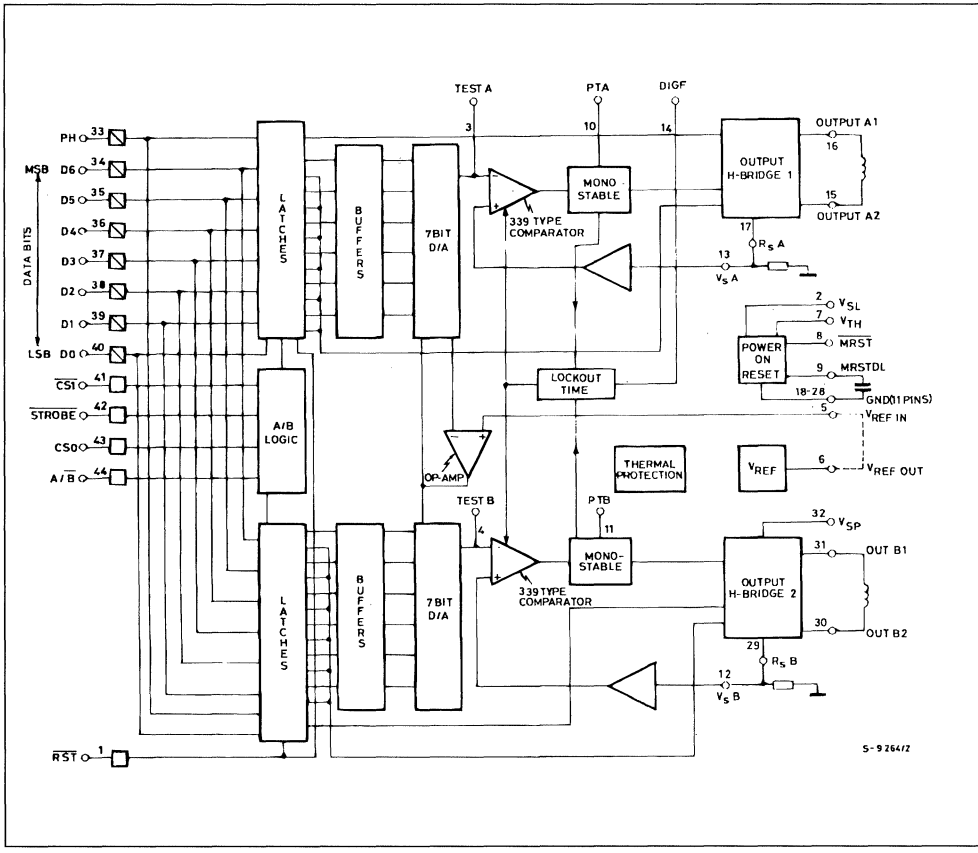
CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{si}	Logic Supply Voltage	7	V
V_{sp}	Motor Supply Voltage	18	V
V_I	Logic Input Voltage	6	V
V_{ref}	Reference Input Voltage	V_{si}	V
I_o	Ouptut Peak Current	500	mA
T_j	Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature	– 55 to + 15	°C

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Impedance Junction-case	Max	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal Impedance Junction-ambient	Max	80	°C/W

PIN FUNCTION DESCRIPTION

N°	Name	Function
1	$\overline{R_{st}}$	Active low input resets the D/A latches to 0 and disables the output.
40, 34	D0-D6	Data inputs for the D/A converter. (D0 = LSB) For a data input of 00, the corresponding outputs are held in the off state.
44	A/$\overline{B}$	Channel select for input data. Pin A/$\overline{B}$ selects channel A when high.
33	PH	Logic input selects direction of current flow in output bridge from A1 (B1) to A2 (B2) for PH = 1.
42	$\overline{Strobe}$	Active low input latches input data (D0, D6 and PH) into input latch.
9	MRST DL	The capacitor on this pin programs the power on reset delay according to the formula : $T_{DR} = (0.35)\ (C)\ 10^6$
8	$\overline{MRST}$	Power-on reset circuit output. (micro reset signal). This output remains low from power on until the delay capacitor has charged past the delay threshold.
10	P_tA	Pulse time A, an external parallel RC network tied to ground defines t_{off} time for channel A. ($T_{off} = 0.69$ RC).
11	P_tB	Pulse time B, an external parallel RC network tied to ground defines t_{off} time for channel B. ($T_{off} = 0.69$ RC).
5	$V_{ref\ in}$	Voltage applied to this points sets the reference for the D/A converter and threfore sets the maximum output current.
18 to 28	Gnd	Ground connection and also conduct heat to the P.C. board.
2	V_{si}	Logic Supply Voltage
32	V_{sp}	Motor Supply Voltage
16, 15 31, 30	Out A1-A2 B1-B2	H-Bridge Outputs.
43, 41	CS0, $\overline{CS1}$	Chip select inputs CS0 is active high, $\overline{CS1}$ is active low.
17, 29	$R_sA - R_sB$	Sense resistor from this pin to ground set the peak output current.
13, 12	$V_sA - V_sB$	Analog inputs for sensing the motor current, separate inputs are provides to allow filtering of the sense voltage if required.
3,4	Test A & B	These pins are for testing of D/A outputs.
6	$V_{ref\ out}$	2.5 V Band Gap Reference
7	V_{th}	Reset Threshold Voltage
14	DIGF	Can be used to modify the internal comparator lockout time. In microstepping typical application a 1.8 KΩ resistor must be connected between this pin and ground.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_j = 25 °C unless otherwise specified noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{sp}	Motor Supply Voltage		8		16	V
V_{si}	Logic Supply Voltage		4.75		5.25	V

LOGIC INPUTS (D0-D6, CS0, $\overline{CS1}$, PH, $\overline{RST}$ and A/$\overline{B}$)

V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2		V_{si}	V
I_{IL}	Input Low Current	V_I = 0.4 V			– 400	µA
I_{IH}	Input High Current	V_I = 2.4 V			10	µA

CURRENT CONTROL AND D TO A SECTION

V_{ref}	Reference Voltage	V_{CC} = 5.0 V	2.45	2.50	2.55	V
V_{rin}	Reference Input Range		2.0		3.0	V
	Monotonicity of D to A		– 0.5		+ 0.5	LSB
	Linearity of D to A		– 1		+ 1	LSB
I_{op}	Peak Output Current (gain of current loop)	V_{ref} = 2.38 V R_{sense} = 2 Ω Data = 7 F (Hex)	225	252	277	mA
I_o	Ouptut Matching	V_{ref} = 2.38 V			5	%

MONOSTABLE

T_{off}	Cutoff Time	R_t = 56 KΩ C_t = 820 pF	28		36	µs
T_d	Turn-off Delay			1		µs
I_{off}	Ouptut Leakage Current	Data = 00 (Hex)			100	µA

RESET CIRCUITY

V_{th}	Reset Threshold Voltage		3.9	4.1	4.3	V
	Reset Threshold Hysteresis		70	100		mV
I_{so}	Delay Capacitor Charging Current	V_C = 2.5 V	7	10	14	µA
I_{si}	Delay Capacitor Discharge Current	V_C = 2.5 V	10			mA
V_{dth}	Delay Threshold Voltage		3.25	3.5	3.75	V
V_{dhys}	Hysteresis Voltage on Delay Threshold		70	100		mV
I_{ol}	Output Leakage Current	V_O = 5 V			200	µA
V_{sat}	Output Saturation of Reset Out	I_O = 2 mA			0.4	V

SOURCE DIODE - TRANSISTOR PAIRS

V_{sat}	Saturation Voltage	I_O = 400 mA		1.3	1.8	V
V_f	Diode Forward Voltage	I_O = 400 mA		0.8	1.2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SINK DIODE - TRANSISTOR PAIRS						
V_{sat}	Saturation Voltage	I_O = 400 mA		1.1	1.5	V
V_f	Diode Forward Voltage	I_O = 400 mA		0.6	1.0	V
AC CHARACTERISTICS						
$T_sDI(ST)$	DI to Strobe ↓ Setup Time		100			ns
$T_hDI(ST)$	DI to Strobe ↓ Hold Time		500			ns
T_wPI	Pulse Width Low		600			ns
T_cST	Strobe Setup Time		2.5			µs
$T_sA/\overline{B}(ST)$	A/$\overline{B}$ to Strobe ↓ Setup Time		100			ns
$T_sPH(ST)$	PH to Strobe ↓ Setup Time		100			ns

CIRCUIT OPERATION

The current control section of the L6217A is a pulse width modulated control that senses the motor current. When the motor current reaches the peak programmed current the comparator will trigger the monostable turning off the upper transistors. After the t_{off} time equal to 0.69 RC the upper drivers are enabled again.

The peak current is given by the equation :

$$I_{op} = \frac{V_{ref}}{4.69 \bullet R_{sense}} \bullet \frac{D}{128.}$$

D = Input data (0 - 7F H)

When the input data is 00, the output stages are disabled by internal logic so that the output current decays rapidly to zero.

An internal generated lockout time avoids the use of an external RC network between the sensing resistor (R_SA, R_SB) and the corresponding input (V_SA, V_SB), by disabling the comparator sensing during the lockout time. This time is typically 2.5 µs.

Figure 1 : Microstepping Typical Application.

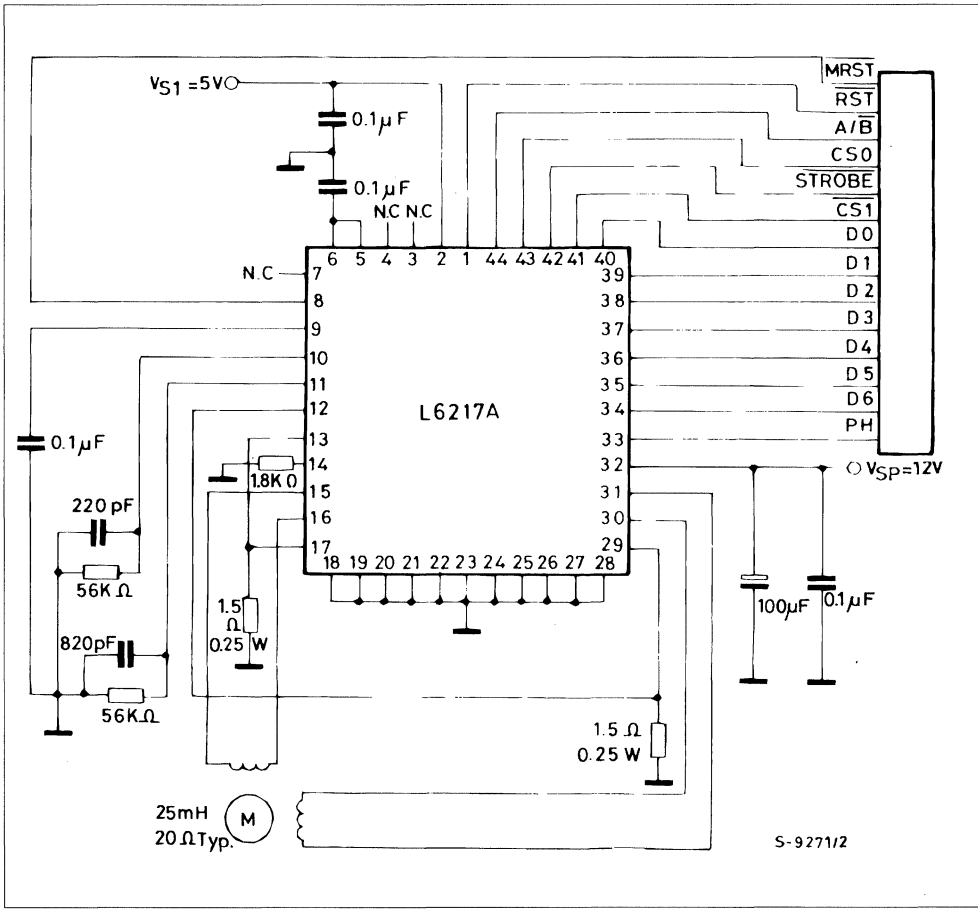


Figure 2 : Microcomputer Interface Timing.

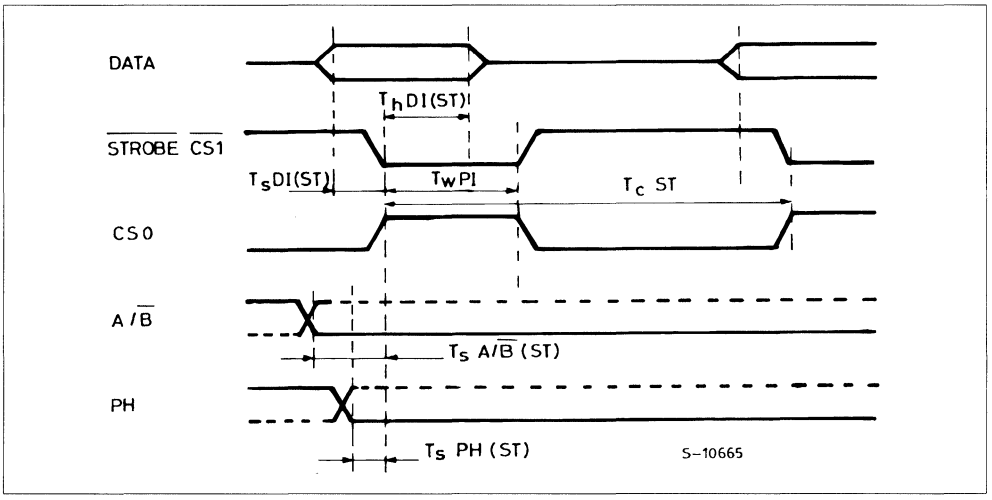


Figure 3 : T_d, T_{OFF} and $T_{lock\ out}$.

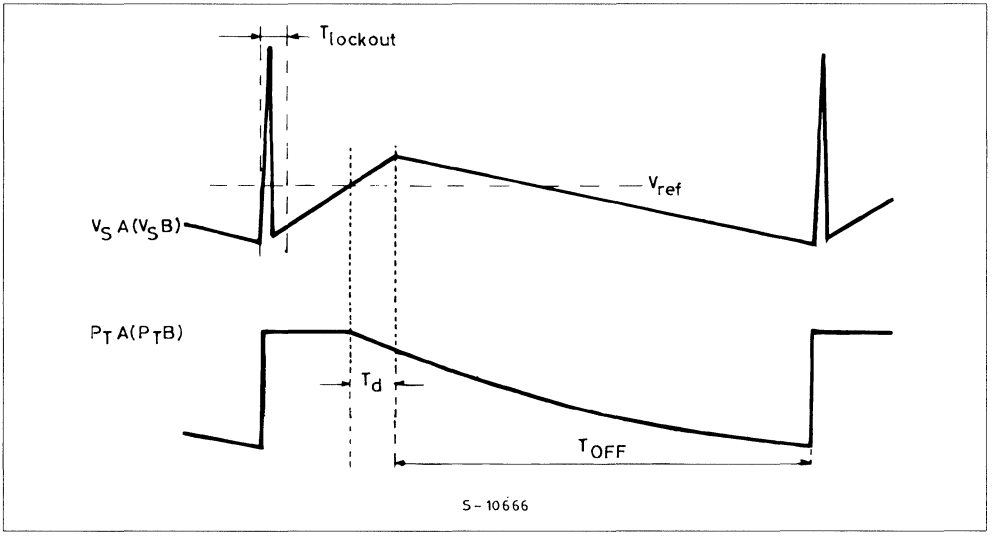
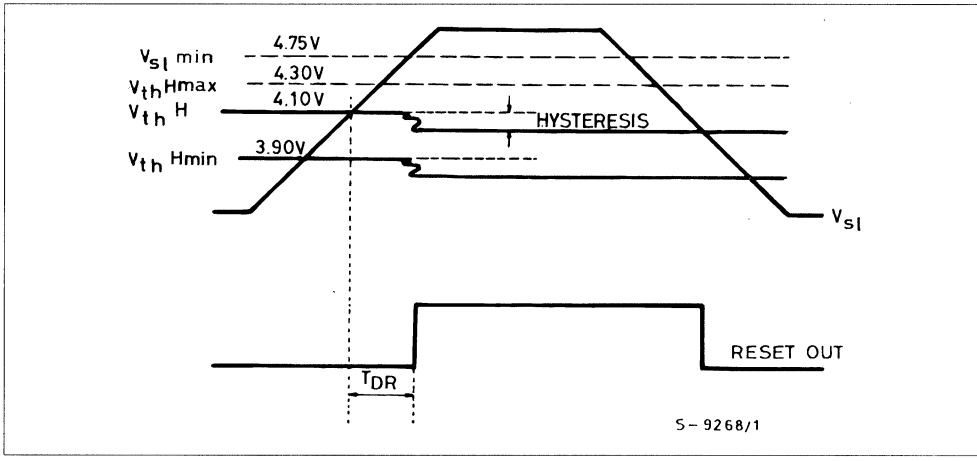


Figure 4 : Reset Waveforms.



QUAD DARLINGTON SWITCHES

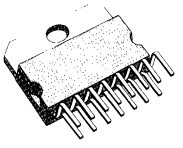
- TWO NON INVERTING + TWO INVERTING INPUTS WITH INHIBIT
- OUTPUT VOLTAGE UP TO 50 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

DESCRIPTION

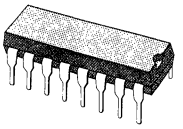
The L6220 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common inhibit input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available : the L6220 mounted in a Powerdip 12 + 2 + 2 package and the L6220N mounted in a 15-lead Multiwatt package.



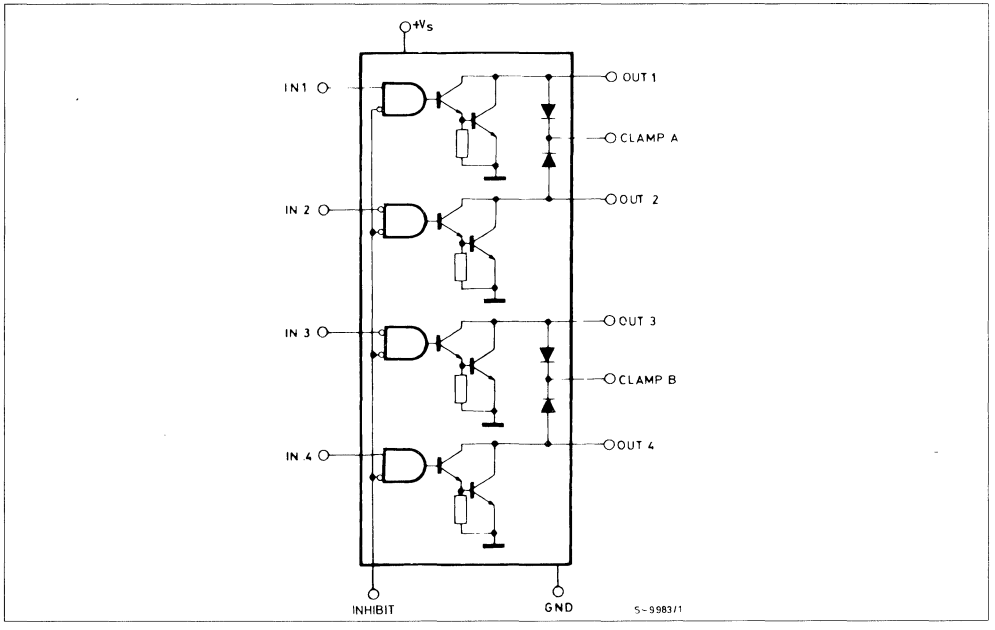
Multiwatt 15



Powerdip 12 + 2 + 2

ORDER CODES : L6220
L6220N

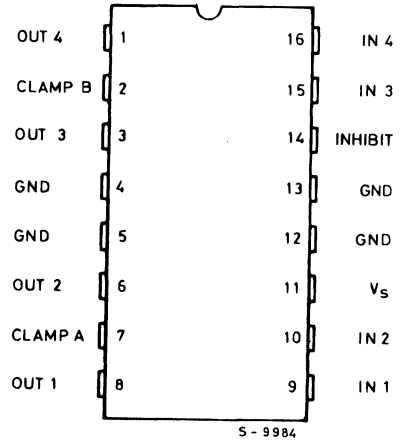
BLOCK DIAGRAM



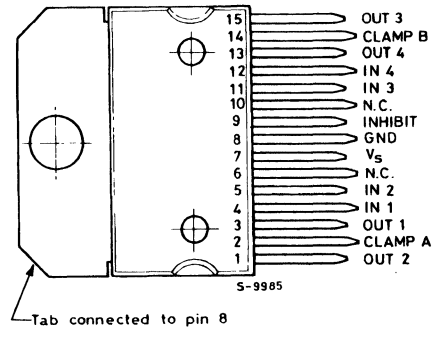
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Ouput Voltage	50	V
V_s	Logic Supply Voltage	7	V
V_{IN}, V_{INH}	Input Voltage, Inhibit Voltage	V_s	
I_C	Continuous Collector Current (for each channel)	1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector Peak Current (non repetitive, t = 10 µs)	3.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
I_{sub}	Output Substrate Current	350	mA
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C (Powerdip) at T_{case} = 90 °C (Multiwatt) at T_{amb} = 70 °C (Powerdip) at T_{amb} = 70 °C (Multiwatt)	4.3 20 1 2.3	W W W W

CONNECTION DIAGRAMS (top views)



L6220 (Powerdip)



L6220N (Multiwatt-15)

THERMAL DATA

			Powerdip	Multiwatt–15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	-
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	-	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	35 °C/W

TRUTH TABLE

Inhibit	Input 1, 4	Power Out	Inhibit	Inputs 2, 3	Power Out
L	H	ON	L	L	ON
L	L	OFF	L	H	OFF
H	X	OFF	H	X	OFF

For each input : H = High level
L = Low level
X = Don't care

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
INHIBIT	Inhibit Input to all Drivers
V_S	Logic Supply Voltage
GND	Common Ground

ELECTRICAL CHARACTERISTICS Refer to the test circuits Fig. 1 to Fig. 9 (V_S = 5V, T_{amb} = 25°C unless otherwise specified)

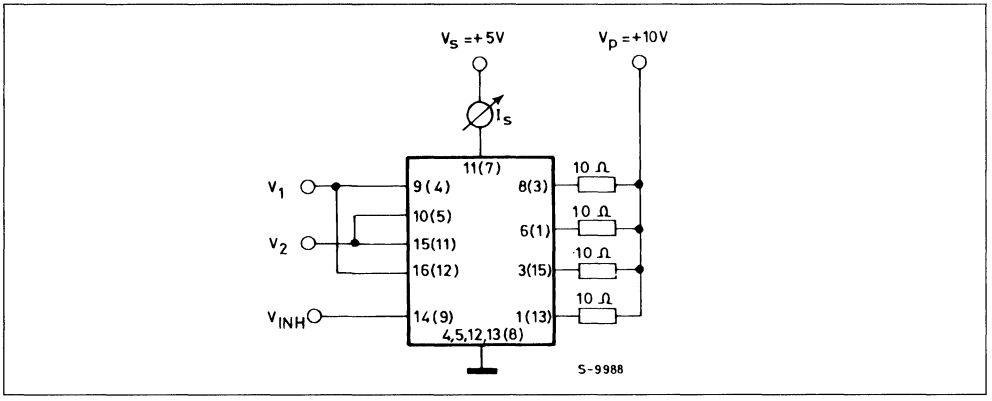
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Logic Supply Voltage			4.5		5.5	V
I_s	Logic Supply Current	All Outputs ON I_C = 0.7 A				20	mA
		All Outputs OFF				20	mA
$V_{CE\ (sus)}$	Output Sustaining Voltage	I_C =100 mA $V_{INH} = V_{INH}H$		46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50 V $V_{IN\ 1.4} = V_{IN}H$				1	mA
$V_{CE\ (sat)}$	Collector Emitter Saturation Voltage (one output on ; all others off.)	V_s = 4.5 V $V_{IN\ 2.3} = V_{IN}L$ $V_{INH} = V_{INH}L$	I_C = 0.6 A			1	V
			I_C = 1 A			1.2	V
			I_C = 1.8 A			1.6	V
$V_{IN}L$, $V_{INH}L$	Input Low Voltage					0.8	V
$I_{IN}L$, $I_{INH}L$	Input Low Current	$V_{IN} = V_{IN}L$ $V_{INH} = V_{INH}L$				– 100	µA
$V_{IN}H$, $V_{INH}H$	Input High Voltage			2.0			V
$I_{IN}H$, $I_{INH}H$	Input High Current	$V_{IN} = V_{IN}H$ $V_{INH} = V_{INH}H$				± 10	µA
I_R	Clamp Diode Leakage Current	V_R = 50 V $V_{INH} = V_{INH}H$				100	µA
V_F	Clamp Diode Forward Voltage	I_F = 1 A				1.6	V
		I_F = 1.8 A				2.0	V
$t_{d\ (on)}$	Turn on Delay Time	V_p = 5 V R_L = 10 Ω				2	µs
$t_{d\ (off)}$	Turn off Delay Time	V_p = 5 V R_L = 10 Ω				5	µs
ΔI_s	Logic Supply Current Variation	V_{IN} = 5 V V_{EN} = 5 V I_{out} = – 500 mA for each Channel				150	mA

TEST CIRCUITS

(X) = Referred to Multiwatt package

X = Referred to Powerdip package

Figure 1 : Logic Supply Current.



Set V_1 = 4.5V, V_2 = 0.8V, V_{INH} = 4.5V or V_1 = 0.8V, V_2 = 4.5V, V_{INH} = 0.8 for I_S (all outputs off).
Set V_1 = 2V, V_2 = 0.8V, V_{INH} = 0.8V for I_S (all outputs on).

Figure 2 : Output Sustaining Voltage.

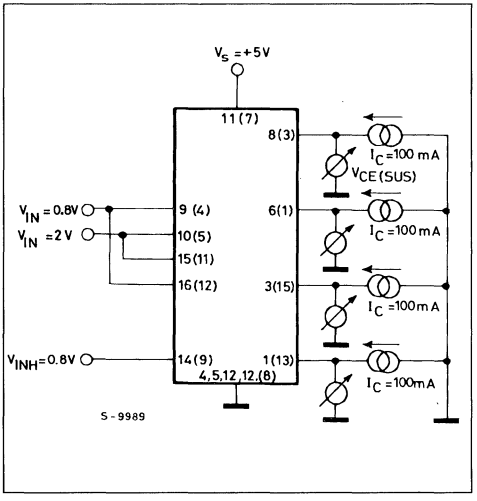


Figure 3 : Output Leakage Current.

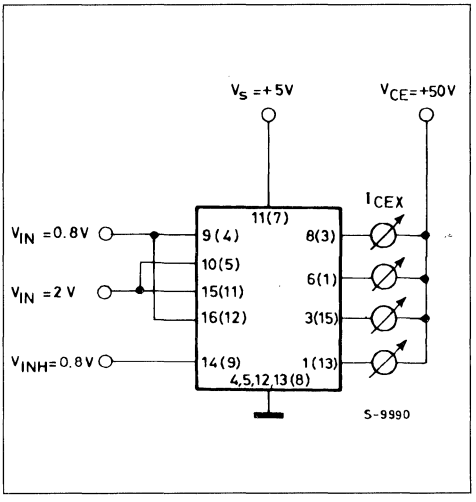


Figure 4 : Collector-emitter Saturation Voltage.

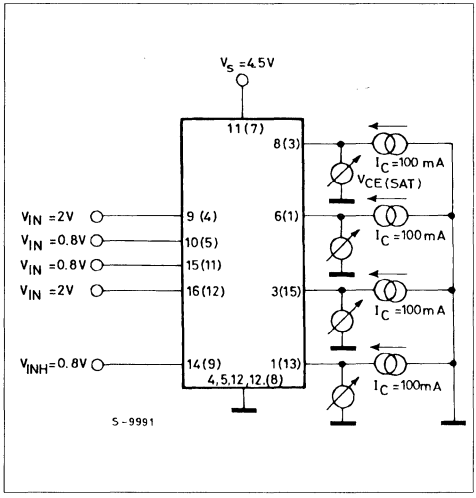
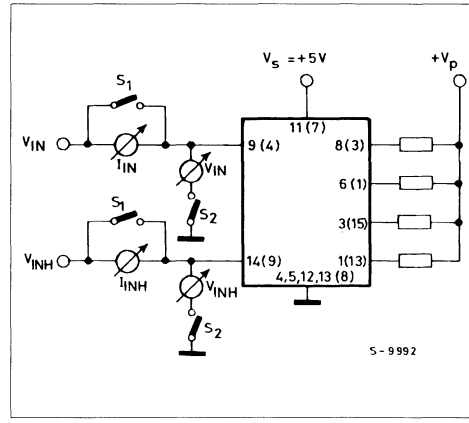


Figure 5 : Logic Input Characteristics.



Set S_1, S_2 open, V_{IN}, V_{INH} = 0.8V for I_{IN} L, I_{INH} L
Set S_1, S_2 open, V_{IN}, V_{INH} = 2V for I_{IN} H, I_{INH} H
Set S_1, S_2 close, V_{IN}, V_{INH} = 0.8V for V_{IN} L, V_{INH} L
Set S_1, S_2 close, V_{IN}, V_{INH} = 2V for V_{IN} H, V_{INH} H.

Figure 6 : Clamp Diode Leakage Current.

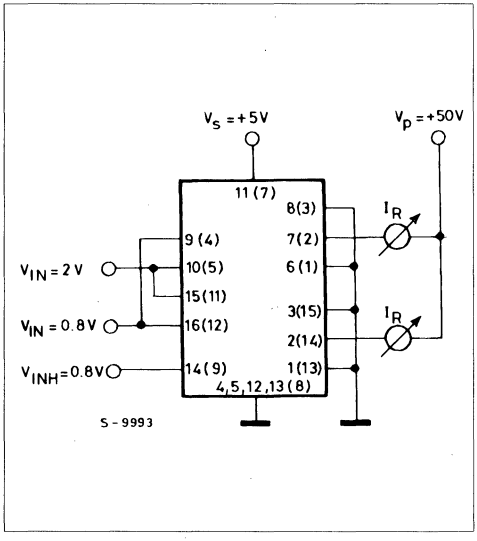


Figure 7 : Clamp Diode Forward Voltage.

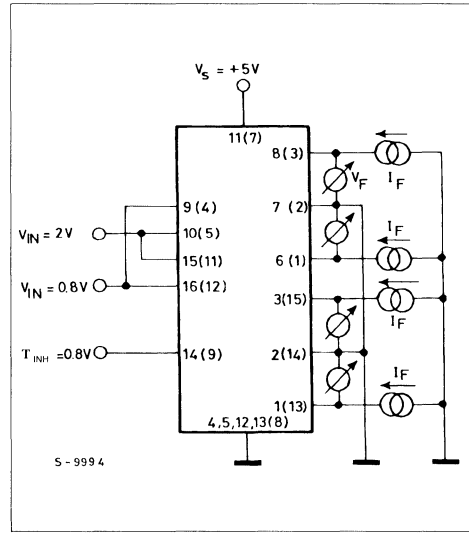


Figure 8 : Switching Times Test Circuit.

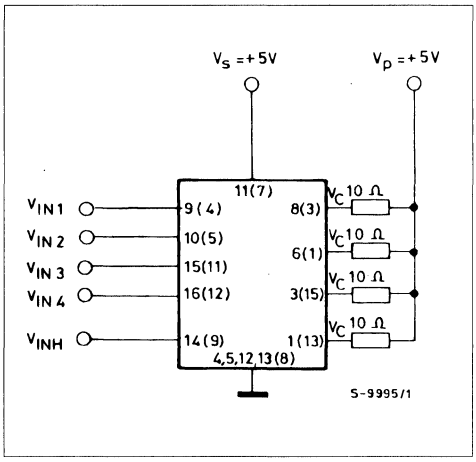


Figure 9 : Switching Times Waveforms.

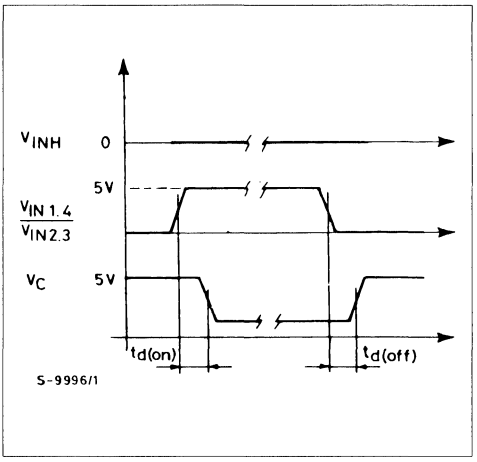


Figure 10 : Collector Saturation Voltage vs. Collector Current.

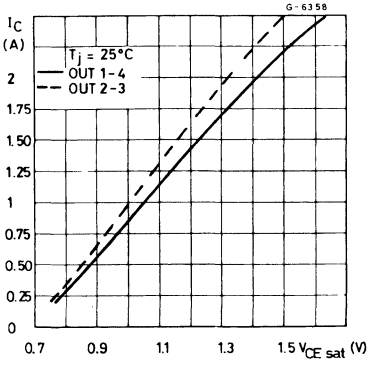


Figure 11 : Free- wheeling Diode Forward Voltage vs. Diode Current.

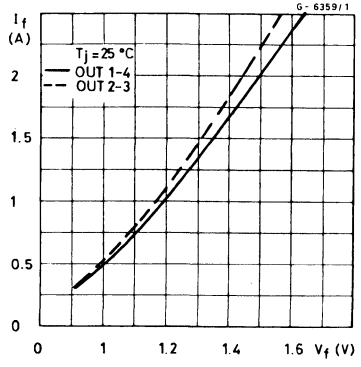


Figure 12 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1 A.

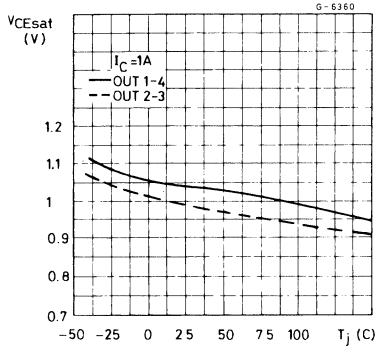


Figure 13 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_f = 1A .

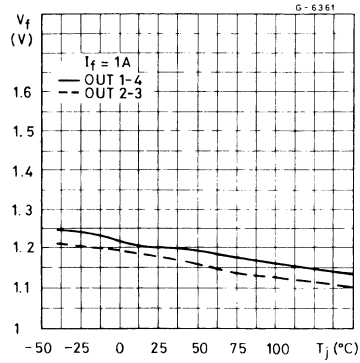


Figure 14 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1.8A.

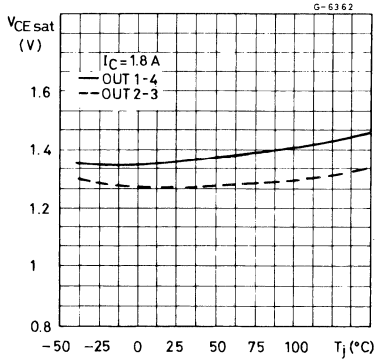


Figure 15 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_F = 1.8A.

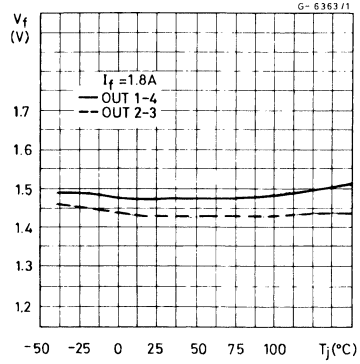


Figure 16.

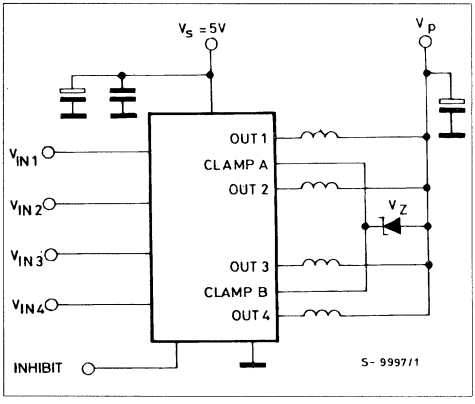
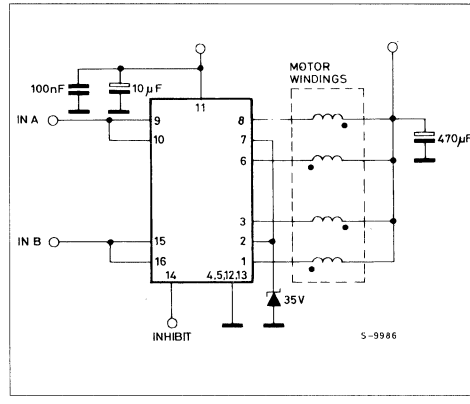


Figure 17 : Unipolar Stepper Motor Driver.



APPLICATION INFORMATION

When inductive loads are driven by L6220/N, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (Fig. 16). For reliability it is suggested that the zener is chosen so that $V_p + V_z < 35$ V.

The reasons for this are two fold :

1) The zener voltage changes in temperature and current.
2) The instantaneous power must be limited to avoid the reverse second breakdown.

The particular internal logic allows an easier full step driving using only two input signals.

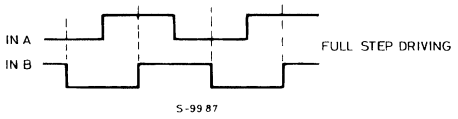


Figure 18 : Allowed Peak Collector-current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6220).

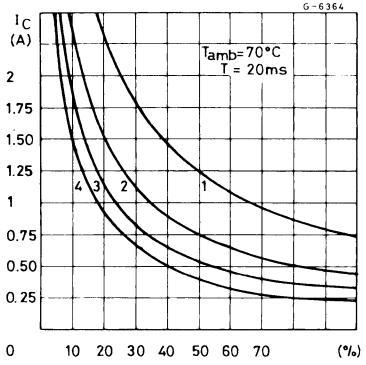
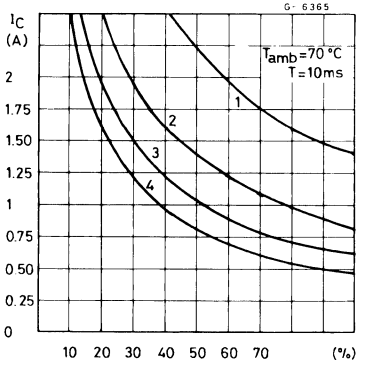


Figure 19 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6220N).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L6220 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 20) or to an external heatsink (Fig. 21).

The diagram of figure 22 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side " α" of two equal square copper areas having a thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 20 : Example of P.C. Board Copper area which is used as Heatsink.

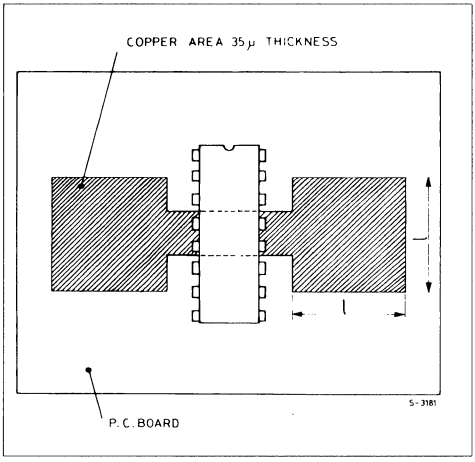


Figure 21 : External Heatsink Mounting Example.

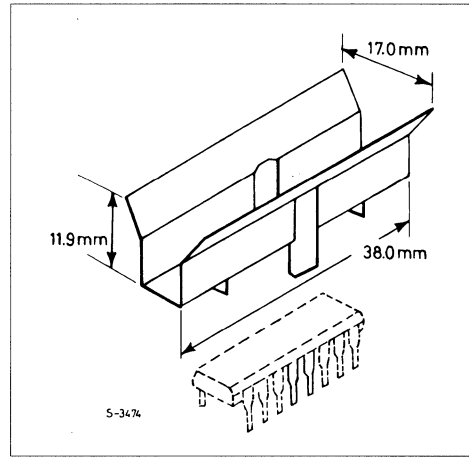


Figure 22 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".

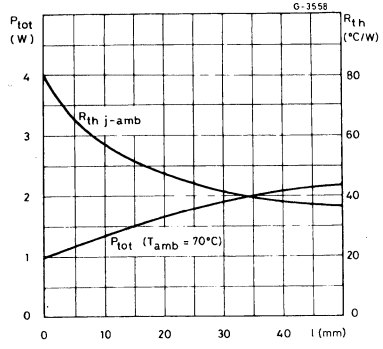
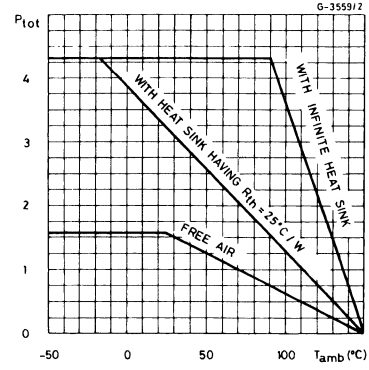


Figure 23 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



QUAD DARLINGTON SWITCH

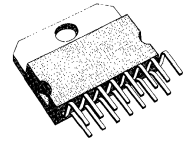
- FOUR NON INVERTING INPUTS WITH ENABLE
- OUTPUT VOLTAGE UP TO 50 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES

DESCRIPTION

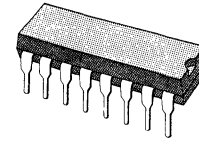
The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive device loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

Two versions are available : the L6221A mounted in a Powerdip 12 + 2 + 2 package and the L6221N mounted in a 15--lead Multiwatt package.



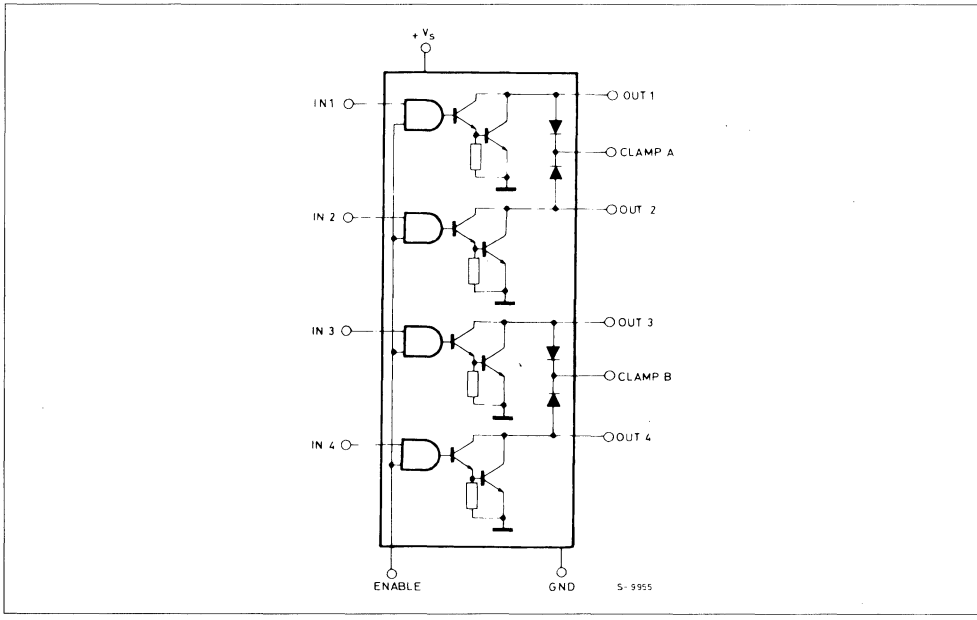
Multiwatt 15



Powerdip 12 + 2 + 2

ORDER CODES : L6221A
L6221N

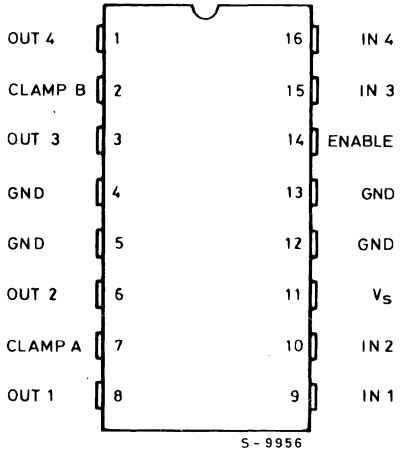
BLOCK DIAGRAM



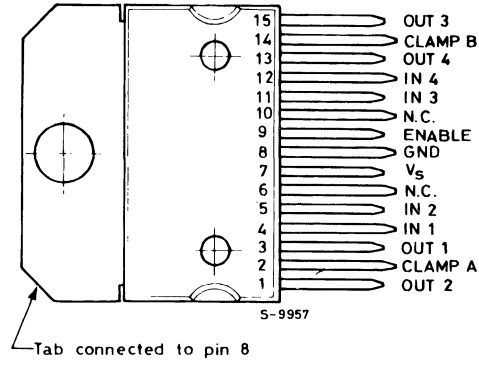
ABSOLUTE MAXIMUM RATINGS

V_o	Output Voltage	50	V
V_s	Logic Supply Voltage	7	V
V_{IN}, V_{EN}	Input Voltage, Enable Voltage	V_s	
I_C	Continuous Collector Current (for each channel)	1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector Peak Current (non repetitive, t = 10 µs)	3.2	A
T_{op}	Operating Temperature Range (junction)	− 40 to + 150	°C
T_{stg}	Storage Temperature Range	− 55 to + 150	°C
I_{sub}	Output Substrate Current	350	mA
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C (powerdip) at T_{case} = 90 °C (multiwatt) at T_{amb} = 70 °C (powerdip) at T_{amb} = 70 °C (multiwatt)	4.3 20 1 2.3	W W W W

PIN CONNECTIONS (top views)



L6221A (Powerdip)



L6221N (Multiwatt-15)

THERMAL DATA

			Powerdip	Multiwatt-15
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14 °C/W	–
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	–	3 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80 °C/W	35 °C/W

TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input : H = High level
L = Low level
X = Don't care

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
ENABLE	Enable Input to All Drivers
V_S	Logic Supply Voltage
GND	Common Ground

ELECTRICAL CHARACTERISTICS Refer to the test circuit to Fig. 1 to Fig. 9
(VS = 5V, Tamb = 25 °C unless otherwise specified)

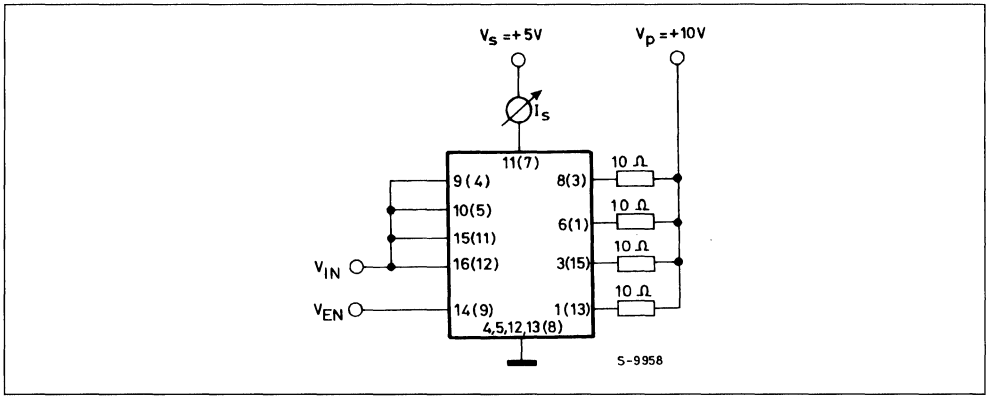
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Logic Supply Voltage			4.5		5.5	V
I_s	Logic Supply Current	All Outputs ON I_C = 0.7 A				20	m A
		All Outputs OFF				20	m A
$V_{CE(sus)}$	Output Sustaining Voltage	V_{IN} = V_{INL} V_{EN} = V_{ENH} I_C = 100 mA		46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50V V_{EN} = V_{ENH} V_{IN} = V_{INL}				1	mA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage (one input on ; all others inputs off.)	V_s = 4.5V V_{IN} = V_{INH} V_{EN} = V_{ENH}	I_C = 0.6 A			1	V
			I_C = 1 A			1.2	V
			I_C = 1.8 A			1.6	V
V_{INL}, V_{ENL}	Input Low Voltage					0.8	V
I_{INL}, I_{ENL}	Input Low Current	V_{IN} = V_{INL} V_{EN} = V_{ENL}				– 100	µ A
V_{INL}, V_{ENH}	Input High Voltage			2.0			V
I_{INH} , I_{ENH}	Input High Current	V_{IN} = V_{INH} V_{EN} = V_{ENH}				± 10	µ A
I_R	Clamp Diode Leakage Current	V_R = 50 V V_{EN} = V_{ENH} V_{IN} = V_{INL}				100	µ A
V_F	Clamp Diode Forward Voltage	I_F = 1 A				1.6	V
		I_F = 1.8 A				2.0	V
$t_{d\ (on)}$	Turn on Delay Time	V_p = 5V R_L = 10Ω				2	µ s
$t_{d\ (off)}$	Turn off Delay Time	V_p = 5V R_L = 10Ω				5	µ s
ΔI_s	Logic Supply Current Variation	V_{IN} = 5V V_{EN} = 5V I_{out} = – 500 mA for Each Channel				150	m A

TEST CIRCUITS

(X) = Referred to Multiwatt package

X = Referred to Powerdip package

Figure 1 : Logic supply current.



Set V_{IN} = 4.5V, V_{EN} = 0.8V, or V_{IN} = 0.8V, V_{EN} = 4.5V, for I_S (all outputs off)
Set V_{IN} = 2V, V_{EN} = 2V, for I_S (all outputs on)

Figure 2 : Output Sustaining Voltage.

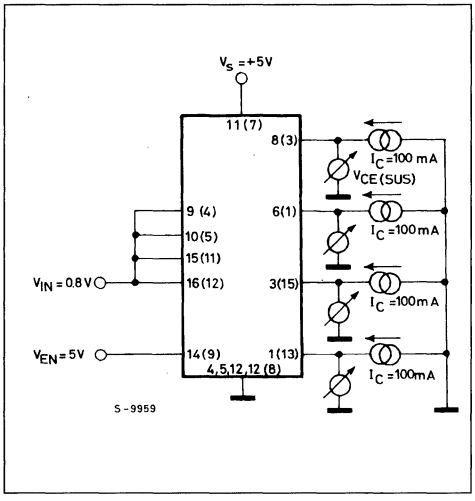


Figure 3 : Output Leakage Current.

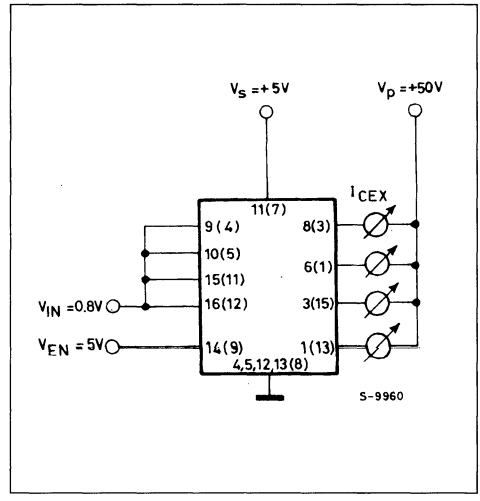


Figure 4 : Collector-emitter Saturation Voltage.

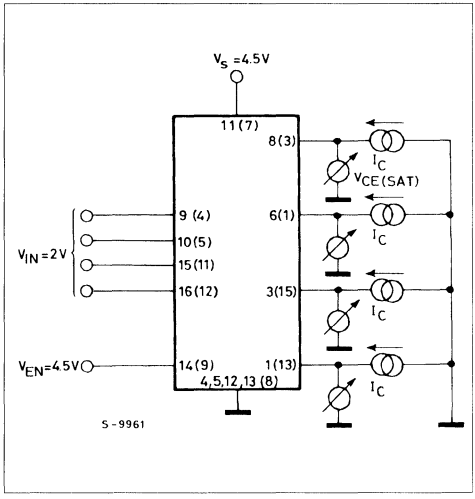
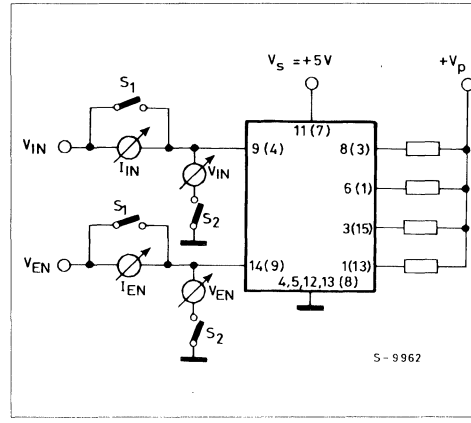


Figure 5 : Logic Input Characteristics.



Set S_1, S_2 open, V_{IN}, V_{EN} = 0.8V for I_{IN} L, I_{EN} L
Set S_1, S_2 open, V_{IN}, V_{EN} = 2V for I_{IN} H, I_{EN} H
Set S_1, S_2 close, V_{IN}, V_{EN} = 0.8V for V_{IN} L, V_{EN} L
Set S_1, S_2 close, V_{IN}, V_{EN} = 2V for V_{IN} H, V_{EN} H

Figure 6 : Clamp Diode Leakage Current.

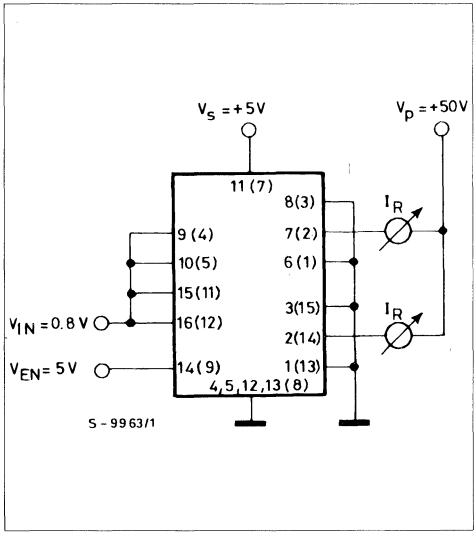


Figure 7 : Clamp Diode Forward Voltage.

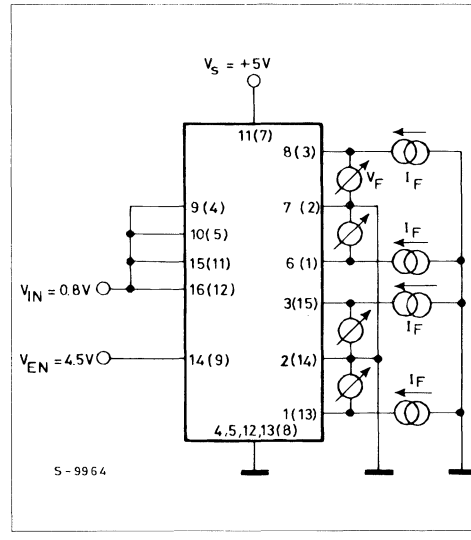


Figure 8 : Switching Times Test Circuit.

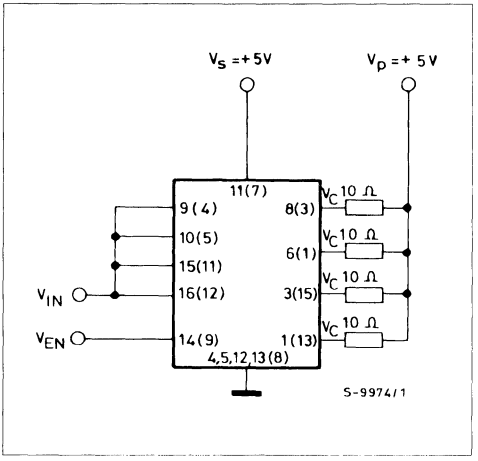


Figure 9 : Switching TImes Waveforms.

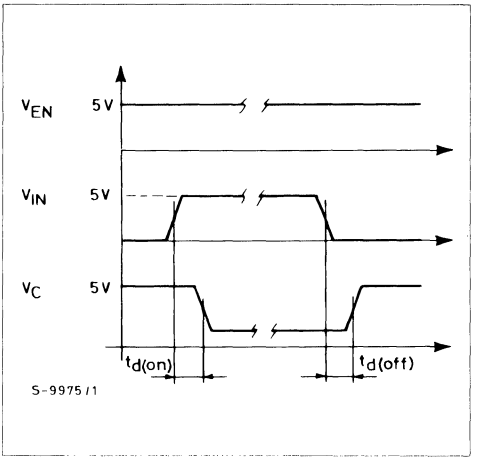


Figure 10 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221A).

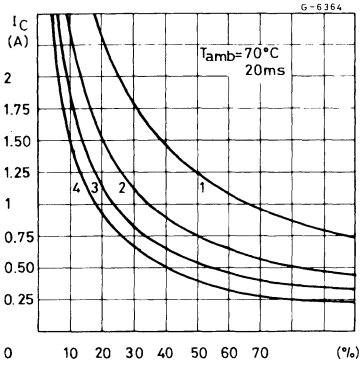


Figure 11 : Allowed Peak Collector Current vs. Duty Cycle for 1, 2, 3 or 4 Contemporary Working Outputs (L6221N).

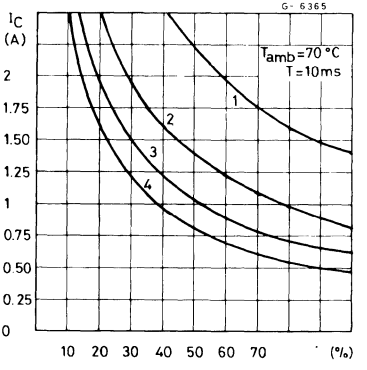


Figure 12 : Collector Saturation Voltage vs. Collector Current.

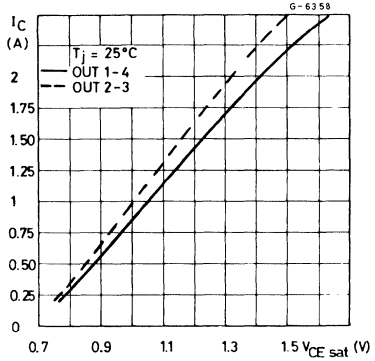


Figure 13 : Free-wheeling Diode Forward Voltage vs. Diode Current .

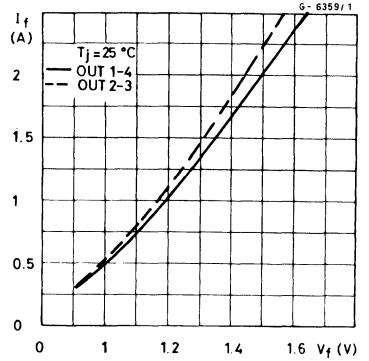


Figure 14 : Collector Saturation Voltage vs. Junction Temperature at I_C = 1A.

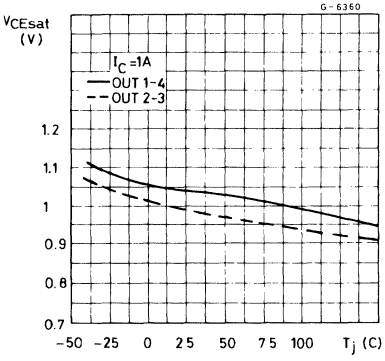


Figure 15 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at I_F = 1A.

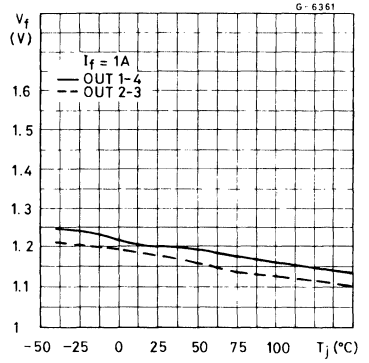


Figure 16 : Saturation Voltage vs. Junction Temperature at IC = 1.8A.

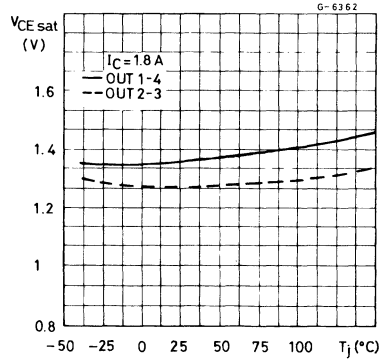


Figure 17 : Free-wheeling Diode Forward Voltage vs. Junction Temperature at If = 1.8A.

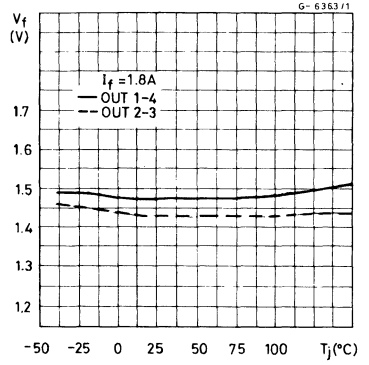
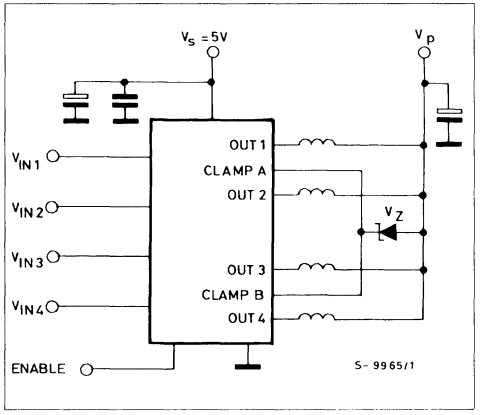


Figure 18.



APPLICATION INFORMATION

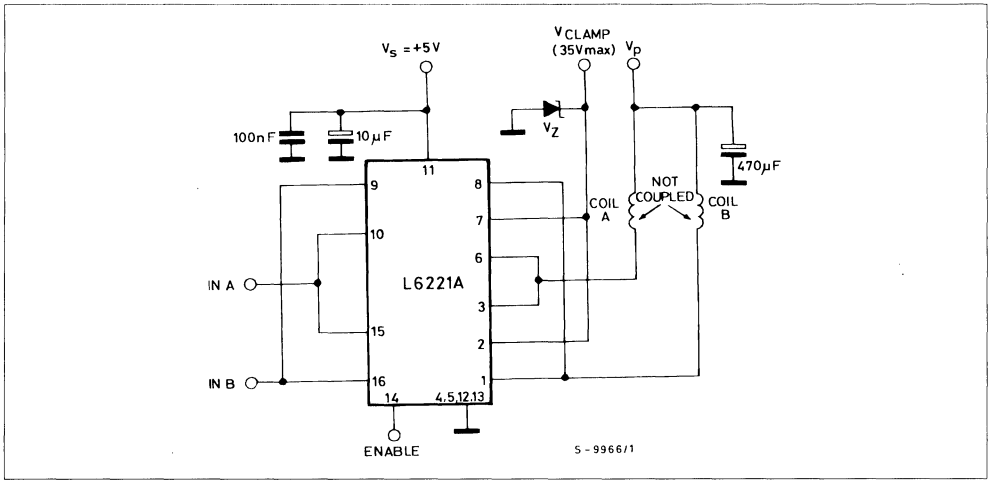
When inductive loads are driven by L6221A/N, a zener diode in series with the integral free-wheeling diodes increases the voltage across which energy stored in the load is discharged and therefore speeds the current decay (fig. 18).

For reliability it is suggested that the zener is chosen so that $V_p + V_z < 35$ V.

The reasons for this are two fold :

1) The zener voltage changes in temperature and current.
2) The instantaneous power must be limited to avoid the reverse second breakdown.

Figure 19 : Driver for Solenoids up to 3A.



Some care must be taken to ensure that the collectors are placed close together to avoid different current partitioning at turn-off.

We suggest to put in parallel channel 1 and 4 and channel 2 and 3 as shown in figure 19 for the similar electrical characteristics of the logic section (turn-on and turn-off delay time) and the power stages (collector saturation voltage, free-wheeling diode forward voltage).

Figure 20 : Saturation Voltage vs. Collector Current.

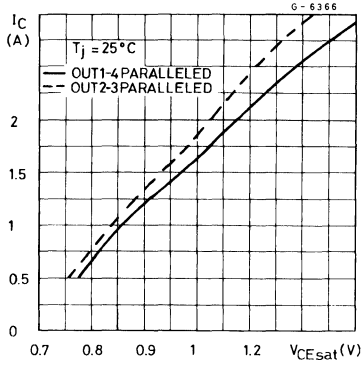


Figure 21 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221A).

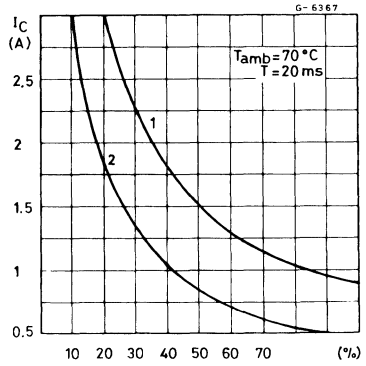
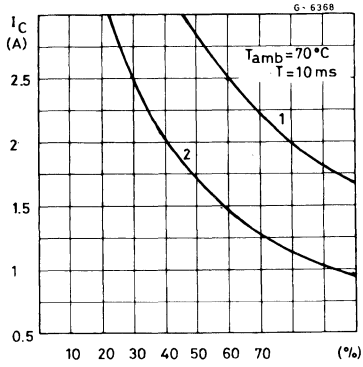


Figure 22 : Peak Collector Current vs. Duty Cycle for 1 or 2 Paralleled Outputs Driven (L6221N).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the L6221A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 23) or to an external heatsink (Fig. 24).

The diagram of figure 25 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side " α" of two equal square copper areas having a thickness of 35μ (1.4 mils). During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 23 : Example of P.C. Board Copper Area Which is Used as Heatsink.

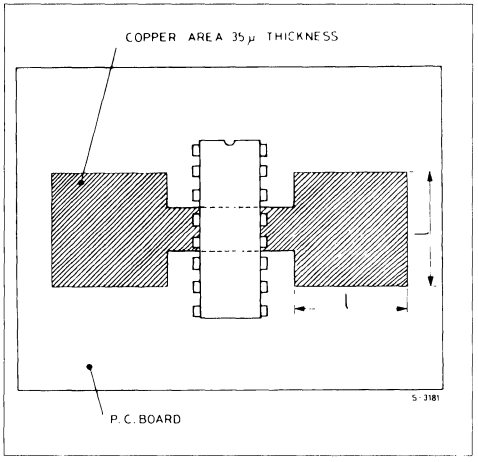


Figure 24 : External Heatsink Mounting Example.

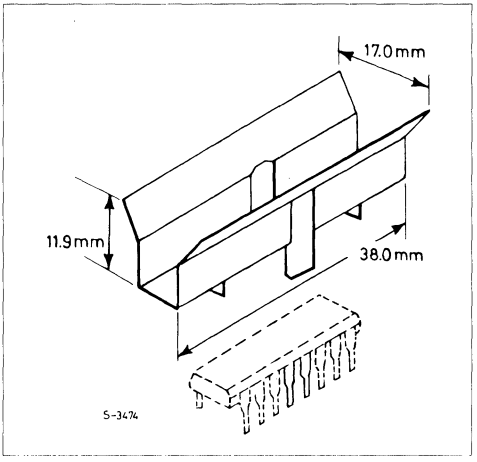


Figure 25 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side " α".

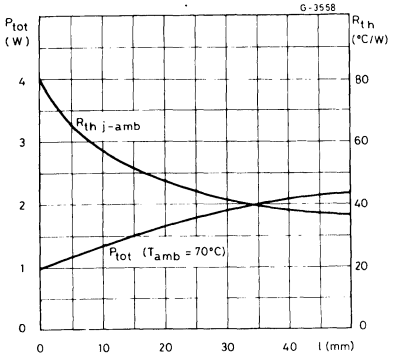
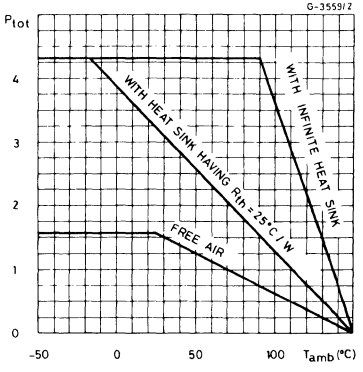


Figure 26 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



QUAD TRANSISTOR SWITCH

- OUTPUT VOLTAGE TO 50 V
- OUTPUT CURRENT TO 1.2 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL SUPPRESSION DIODE

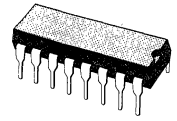
DESCRIPTION

The L6222 monolithic quad transistor switch is designed for high current, high voltage switching applications.

Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits. Each switch consists of an open-collector transistor plus a clamp diode for applications with inductive loads.

The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

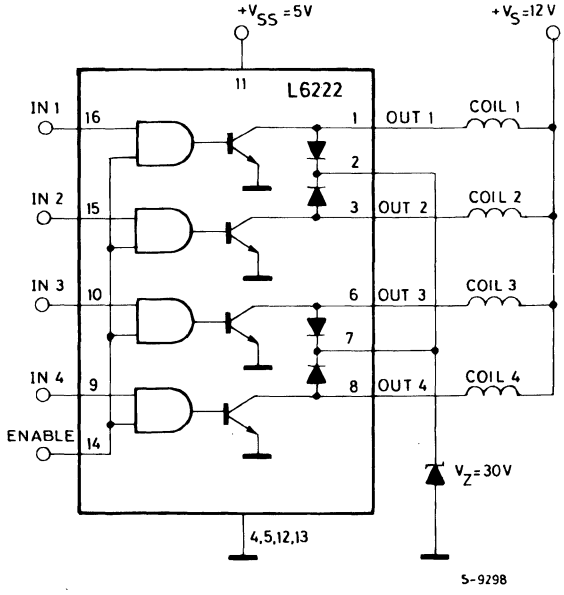
This device is intended to drive coils such as relays, solenoids, unipolar stepper motors, LED, etc.



Powerdip 12 + 2 + 2

ORDER CODE : L6222

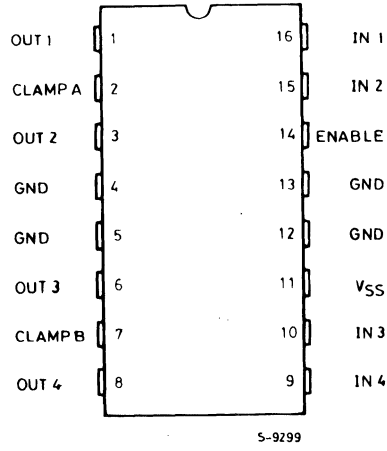
Figure 1 : Unipolar Stepper Motor Drive.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Output Voltage	50	V
V_{ss}	Logic Supply Voltage	7	V
V_{IN}	Input Voltage	15	V
I_C	Collector Current (PEAK)	1.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C

CONNECTION DIAGRAM (top view)



TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input : H = High level
L = Low level
X = Don't care

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	° C / W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	14	° C / W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless specified)

Symbol	Parameter	Test Conditions		Min.	Unit	Max.	Typ.
V_{SS}	Logic Supply Voltage			4.50		7	V
$V_{CE\ (sus)}$	Output Sustaining Voltage	V_{IN} = 0.8 V I_C = 100 mA		46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50 V V_{IN} = 0.8 V				1	mA
$V_{CE\ (sat)}$	Collector Emitter Saturation Voltage	$V_{IN} \geq$ 2.0V	I_C = 0.1 A			0.2	V
			I_C = 0.4 A			0.5	
			I_C = 0.7 A			0.9	
V_{IL}	Input low Voltage					0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4 V				– 100	µA
V_{IH}	Input High Voltage			2.0			V
I_{IH}	Input High Current	$V_{IN} \geq$ 2.0 V				± 10	µA
I_S	Logic Supply Current	V_{SS} = 5 V	All Outputs ON I_C = 0.7 A		50	85	mA
			All Outputs OFF		8		mA
I_R	Clamp Diode Leakage Current	V_R = 50 V				100	µA
V_F	Clamp Diode Forward Voltage	I_F = 0.7 A				1.6	V
		I_F =1.2 A				2.0	

BIDIRECTIONAL THREE-PHASE BRUSHLESS DC MOTOR DRIVER

PRELIMINARY DATA

- 3A OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- SUPPLY VOLTAGE UP TO 18 V
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3 f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

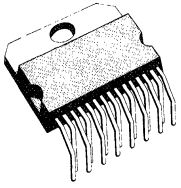
DESCRIPTION

The L6230 is a single-chip driver for three-phase brushless DC motors capable of delivering 3A output current with supply voltages to 18 V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase bidirectional drive. Both delta and wye configurations may be used

To limit EMI esmission the L6230 operates in a linear mode and controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation : during recirculation the output stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL systems, may be used with the L6230 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

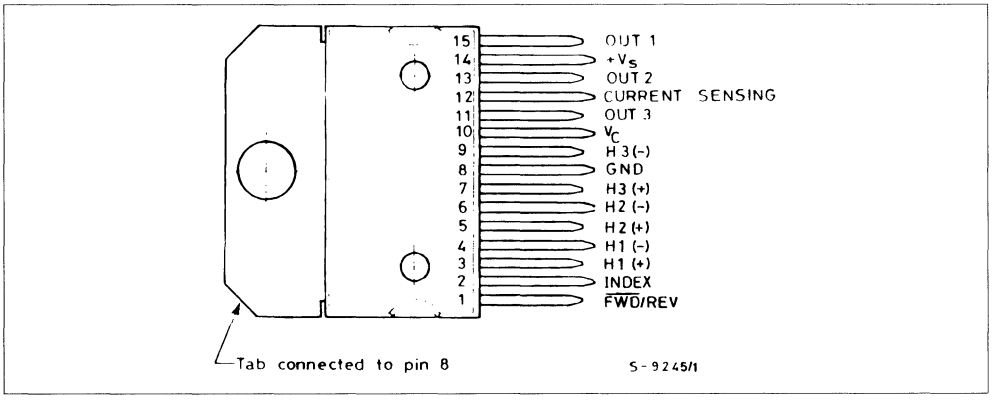
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



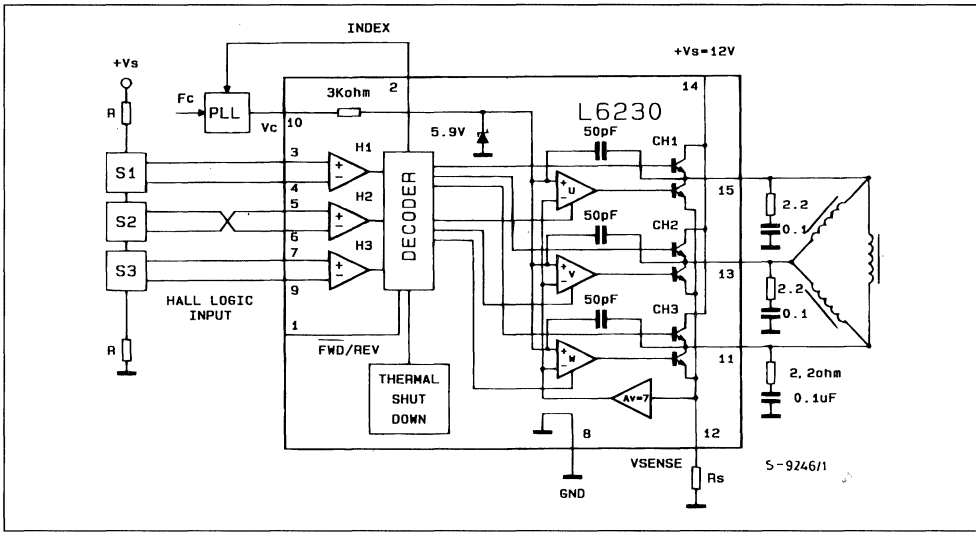
Multiwatt-15
(Horizontal)

ORDER CODE : L6230H

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	20	V
I_o	Peak Output Current Each Channel – Non Repetitive (100 µs) – Repetitive (t = 10 ms) – DC Operation	 4 3.5 3	 A A A
V_i	Logic and Analogic Inputs	V_S	
P_{tot}	Total Power Dissipation T_{case} = 75 °C	25	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

PIN FUNCTIONS

N°	Name	I/O	Function
1	FWD/REV	I	Direction Control. When this pin is low, the motor will run in the forward direction. A high will drive the motor in the reverse direction. Direction is defined by the position of the sensors in the motor.
2	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
3	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
4	H1 (–)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
5	H2 (+)	I	Same as Pin 3 for Channel 2
6	H2 (–)	I	Same as Pin 4 for Channel 2
7	H3 (+)	I	Same as Pin 3 for Channel 3
8	GND		Ground Connection
9	H3 (–)	I	Same as Pin 4 for Channel 3
10	V_c	I	Speed control input. Connected to output of PLL in PLL speed control applications.
11	OUT3	O	Output motor drive for phase 3.
12	SENSE	I	Current Sensing. Input for load current sense voltage for output stage.
13	OUT2	O	Output motor drive for phase 2.
14	V_s		Motor Supply Voltage
15	OUT1	O	Output motor drive for phase 1.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C ; V_s = 12 V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		10	12	18	V
I_s	Quiescent Supply Current			60	100	mA

HALL AMPLIFIERS

V_{CM}	Common Mode Voltage Range		0		10	V
V_{io}	Input Offset Voltage	V_i = 6 V		2	10	mV
I_{ib}	Input Bias Current	V_i = 6 V		2	10	µA
I_{io}	Input Offset Current	V_i = 6 V		0.1		µA

SPEED CONTROL INPUT (V_C)

V_i	Input Voltage Range		0		5	V
I_{ib}	Input Bias Current	$V_C < V_{sens}$		1	5	µA
V_{ic}	Input Clamping Voltage			5.9		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
FWD/REVERSE INPUT						
V_{IH}	Input High Voltage		2		V_s	V
V_{IL}	Input Low Voltage		0		0.8	V
I_{IH}	Input High Current				10	µA
I_{IL}	Input Low Current			– 5	– 50	µA
HALL LOGIC OUTPUT						
V_{LO}	Low Output Voltage	I = 5 mA			0.8	V
I_L	Leakage Current	V_{CE} = 12 V			10	µA
OUTPUT POWER STAGE						
V_{sat}	Total Saturation Voltage	I_o = 1 A I_o = 2 A I_o = 3 A		2.7 3.6 4.2	3.7 4.5	V
V_{OSR}	Ouput Voltage Slew-rate			100		V/ms
V_{sens}	Sens Voltage Range		0		0.7	V
THERMAL SHUTDOWN						
T_j	Junction Temperature		150			°C
T_H	Hysteresis				30	°C

DESCRIPTION

The L6230 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase bidirectional drive.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

The direction of rotation is controlled by the forward/reverse input (pin 1). When this pin is at a low level the motor rotates in the forward direction.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is buffered H1 input). The output of the PLL is connected to the speed control input on the device at pin 10, V_C.

In addition, a 1 V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s, senses the ouptut stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop in the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by :

$$I_o = (V_C - 1) / 7\ R_s$$

The value of the sensing resistor is given by :

$$R_s = (V_X - 1) / (7\ I_{max})$$

where V_X is the full scale voltage of V_C (see fig.2).

In this way the V_C / I_{out} characteristics can be modified as shown in Fig. 2. Note that V_X max is clamped at 5.9 V.

The most important feature of the L6230 is slew rate control. With this device a typical value of 0.1 V/µs is achieved, reducing EMI to a very low value.

In a delta configuration a key feature is three-state operation ; when the current is recirculating the corresponding phase driver is switched off and power dissipation in negligible. Current recirculates through the integrated free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

The L6230 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals in three terminals (of the same polarity) and a TTL level on the other three terminals.

Figure 1 : Truth Table for Forward Rotation.

Hall Effect Diff. Input 1 = Positive 2 = Negative			Upper Driver Status 1 = On 2 = Off			Lower Driver Status 1 = On 2 = Off		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	1	0	0	0	0	1
1	1	0	0	1	0	0	0	1
1	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
0	0	1	0	0	1	0	1	0
0	0	0	1	0	0	0	1	0

Figure 2 : Output Current vs. Control Voltage.

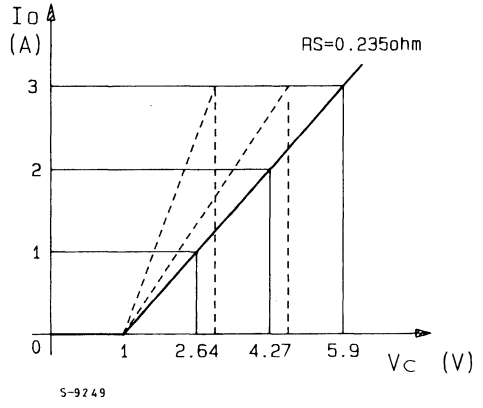
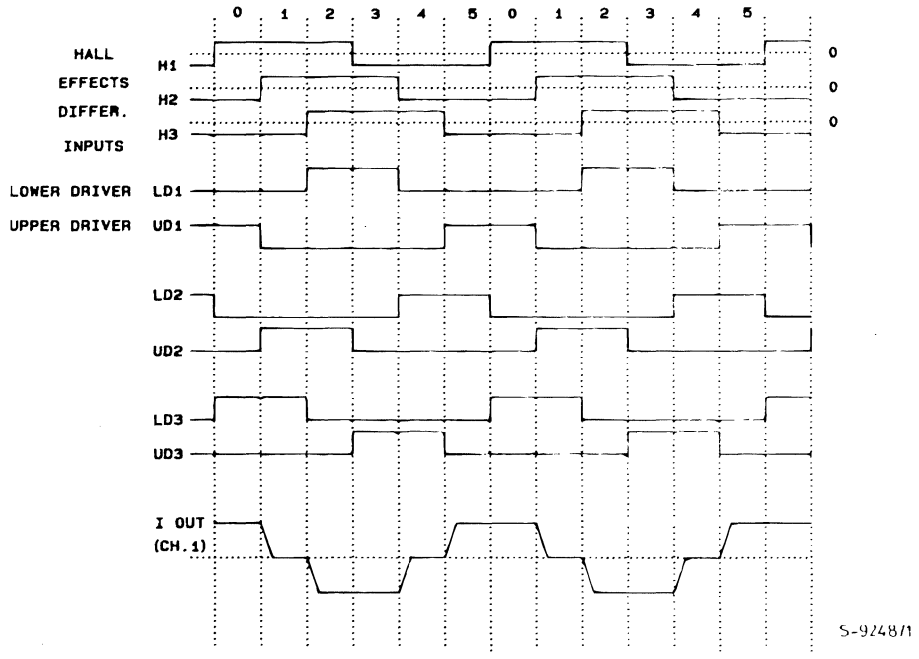


Figure 3 : Timing Diagram.



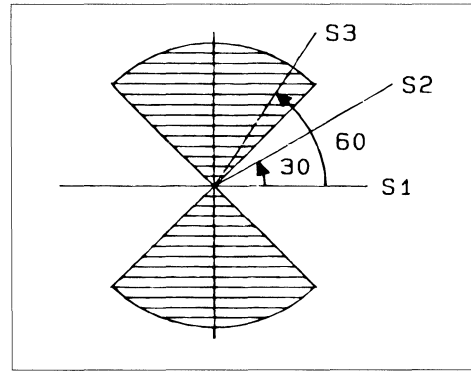
DETERMINING HALL EFFECT SENSOR CODING

The L6230 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig.3, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6230. Note that the rotation in fig. 4 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 4 is a stylized concept for the determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6230 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

For example, let us ecamine the output pattern of a different type of motor (fig. 5). Assuming 90 windows at 180 intervals, then with respect to fig. 4, a similar diagram, fig. 6, results in sensors 60 apart with the windows rotating clockwise. This situation results in a "forward" rotation of the motor.

Figure 4.



Since S3 is the first sensor encountered by the window in fig. 6, this should be used for the L6230 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6230 must go high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3 . By continuing around the diagram, one can develop a pattern which matches that for the L6230.

Figure 5.

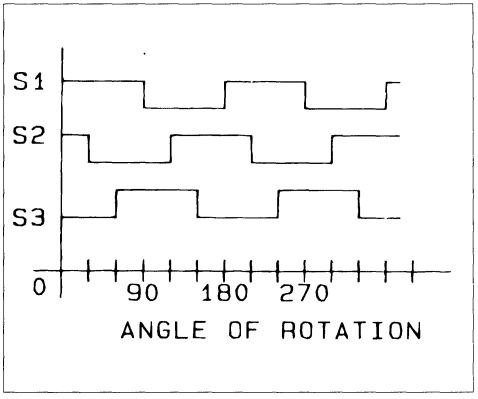
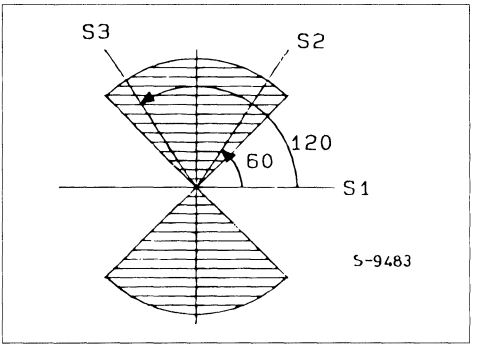


Figure 6.



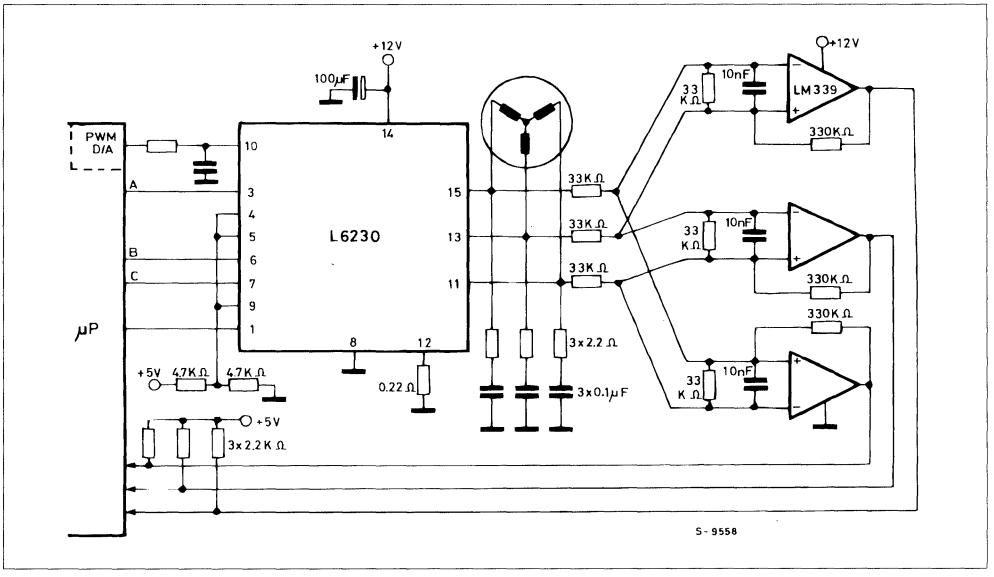
Thus, the conversion table for this particular motor is :

Motor Sensors	L6230 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6230. Since the L6230 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

APPLICATION INFORMATION

Figure 7 : Brushless Motor Control without Hall Sensors.



L6230 can be adapted to a brushless motor without Hall sensors.

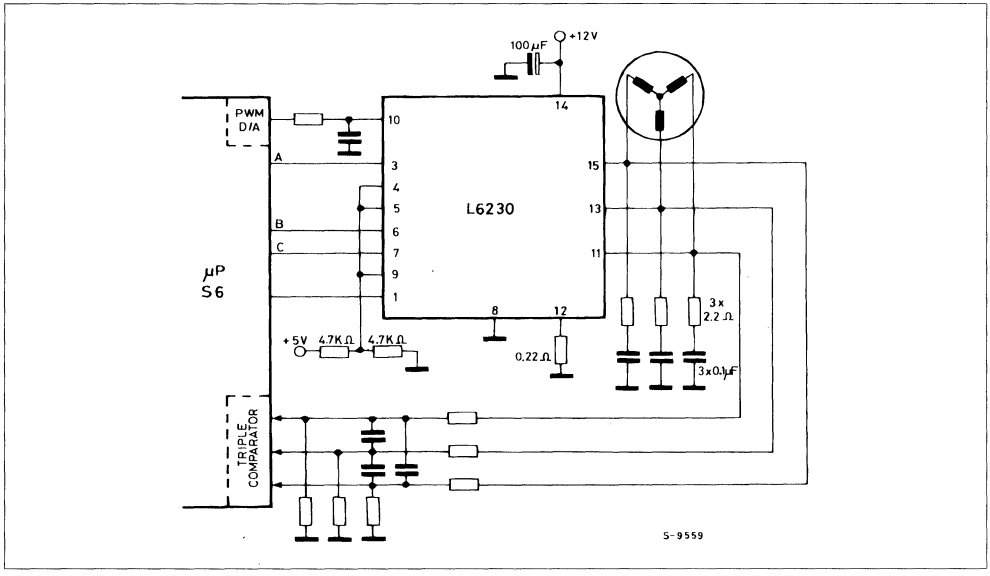
The circuit detects after filtering the back EMF of the motor and use this signal for commutation. This application needs a µP to start up the motor with a rotating clock pulse on the outputs until the back EMF is present.

The µP can also provide the speed regulation loop by software. For a quick performance test of application, it's possible to interconnect the comparator outputs directly to the L6230 inputs. In this case a manual start up is needed.

By using S6 µP with a dedicated ADC or comparator inputs, only passive external components are required.

A discussion with a motor producer give us the information, the cost of 3 phase hall sensors including assembly are in the range of 3 to 4 DM.

Figure 8 : Brushless Motor Control with Dedicated µP.



THREE-PHASE BRUSHLESS DC MOTOR DRIVER

PRELIMINARY DATA

- 3A OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- SUPPLY VOLTAGE UP TO 18 V
- COMPATIBLE WITH ANI f-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- INHIBIT FUNCTION
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3 f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

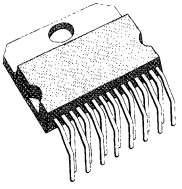
DESCRIPTION

The L6231 is a single-chip driver for three-phase brushless DC motors capable of delivering 3A output current with supply voltages to 18 V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase drive.

To limit EMI emission the L6231 controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation : during recirculation the ouptut stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including f to V and PLL systems, may be used with the L6231 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

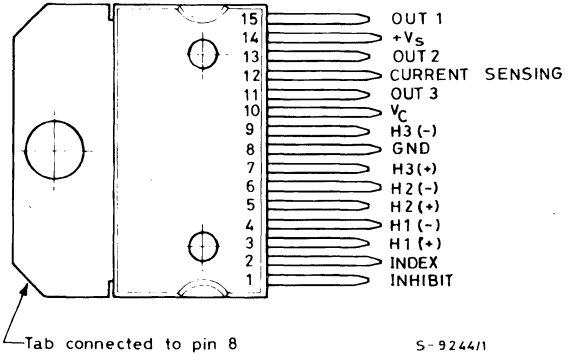
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



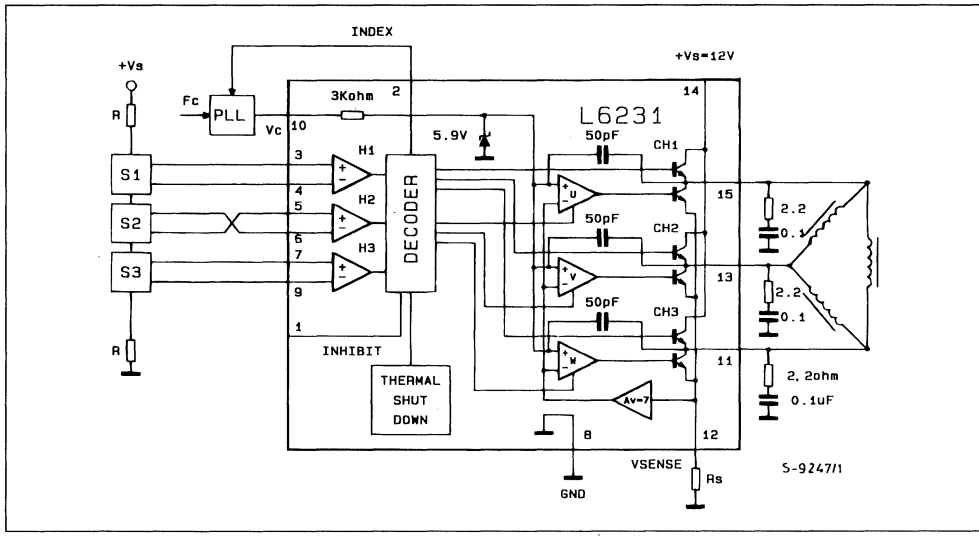
Multiwatt-15
(Horizontal)

ORDER CODE : L6231H

PIN CONNECTION (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	20	V
I_o	Peak Output Current Each Channel - Non Repetitive (100 µs) - Repetitive (t = 10 ms) - DC Operation	 4 3.5 3	 A A A
V_I	Logic and Analogic Inputs	V_s	
P_{tot}	Total Power Dissipation T_{case} = 75 °C	25	W
T_{op}	Operating Temperature Range	0 to 70	°C
T_j, T_{sgt}	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

PIN FUNCTIONS

N°	Name	I/O	Function
1	INHIBIT	I	Output Stage Inhibit. When this pin is high all three output stages are in a high impedance state.
2	INDEX	O	Signal Pulse Proportional to the Motor Speed. In PPL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
3	H1 (+)	I	Positive Input of Differential Amplifier on Channel 1. Interfaces with Hall Effect sensor, S1, from motor.
4	H1 (–)	I	Negative Input of Differential Amplifier on Channel 1. Interfaces with Hall Effect sensor, S1, from motor.
5	H2 (+)	I	Same as Pin 3 for Channel 2.
6	H2 (–)	I	Same as Pin 4 for Channel 2.
7	H3 (+)	I	Same as Pin 3 for Channel 3.
8	GND		Ground Connection.
9	H3 (–)	I	Same as Pin 4 for Channel 3.
10	V_C	I	Speed Control Input. Connected to output of PLL in PLL speed control applications.
11	Out 3.	O	Output Motor Drive for Phase 3.
12	Sense	I	Current Sensing. Input for load current sense voltage for output stage.
13	Out 2	O	Output Motor Drive for Phase 2.
14	V_S		Motor Supply Voltage.
15	Out 1	O	Output Motor Drive for Phase 1.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C ; V_S = 12V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		10	12	18	V
I_S	Quiescent Supply Current			60	100	mA

HALL AMPLIFIERS

V_{CM}	Common Mode Voltage Range		0		10	V
V_{io}	Input Offset Voltage	V_I = 6 V		2	10	mV
V_{Ib}	Input Bias Current	V_I = 6 V		2	10	µA
I_{io}	Input Offset Current	V_I = 6 V		0.1		µA

SPEED CONTROL INPUT (V_C)

V_I	Input Voltage Range		0		5	V
I_{Ib}	Input Bias Current	$V_C < V_{sens}$		1	5	µA
V_{Ic}	Input Clamping Voltage			5.9		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INHIBIT INPUT						
V_{IH}	Input High Voltage		2		V_S	V
V_{IL}	Input Low Voltage		0		0.8	V
I_{IL}	Input High Current				10	µA
I_{IL}	Input Low Current			– 5	– 50	µA
HALL LOGIC OUTPUT						
V_{LO}	Low Output Voltage	I = 5 mA			0.8	V
I_L	Leakage Current	V_{CE} = 12 V			10	µA
OUTPUT POWER STAGE						
V_{sat}	Total Saturation Voltage	I_o = 1A I_o = 2A I_o = 3A		2.7 3.6 4.2	3.7 4.5	V
V_{OSR}	Output Voltage Slew-rate			100		V/ms
V_{sens}	Sens Voltage Range		0		0.7	V
THERMAL SHUTDOWN						
T_j	Junction Temperature		150			°C
T_H	Hysteresis				30	°C

DESCRIPTION

The L6231 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase drive. When the INHIBIT INPUT is high all three OUTPUT ARE PLACED in a high - IMPEDANCE STATE.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is buffered H1 input). The output of the PLL is connected to the speed control input on the device at pin 10, V_C.

In addition, a 1 V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s, senses the ouptut stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by :

$$I_o = \frac{(V_C - 1)}{7\ Rs}$$

The value of the sensing resistor is given by :

$$R_s = (V_X - 1) / (7\ I_{max})$$

where V_X is the full scale voltage of V_C (see fig.2).

In this way the V_C / I_{out} characteristics can be modified as shown in Fig. 2. Note that V_X max is clamped at 5.9 V.

The most important feature of the L6231 is slew rate control. With this device a typical value of 0.1 V/µs is achieved, reducing EMI to a very low value.

Another key feature is three-state operation ; when the current is recirculating the corresponding phase driver is switched off and power dissipation in negligible. Current recirculates through the free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

The L6231 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Figure 1 : Truth Table.

Hall Effect Diff. Input 1 = Positive 0 = Negative			Upper Driver Status 1 = On 0 = Off			Lower Driver Status 1 = On 0 = Off		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	0	0	1	1	0	0
1	1	0	0	0	1	0	1	0
1	1	1	1	0	0	0	1	0
0	1	1	1	0	0	0	0	1
0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	0	0

Figure 2 : Output Current vs. Input Voltage.

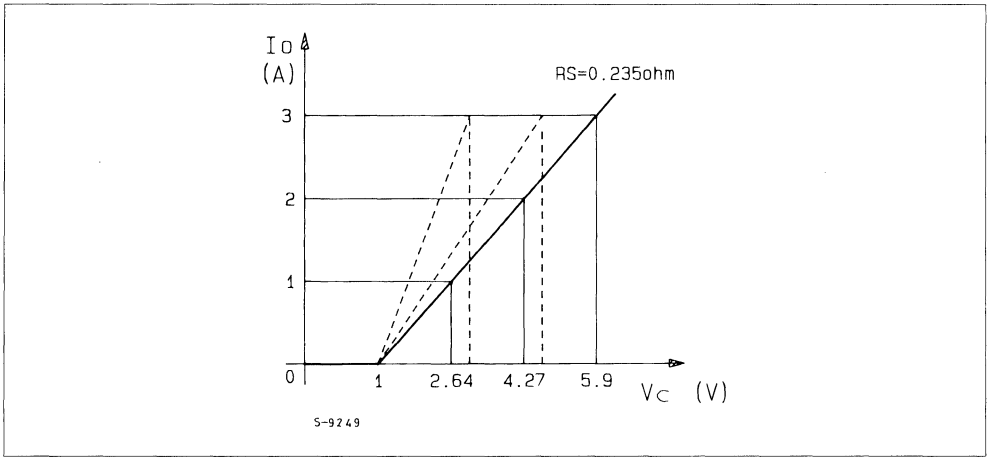
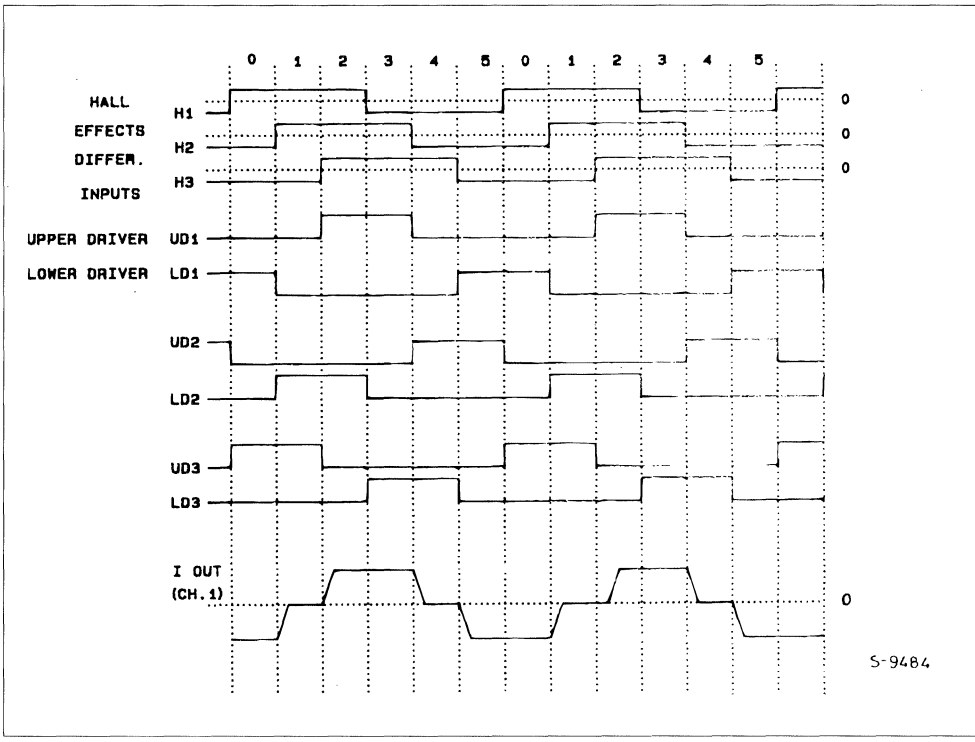


Figure 3 : Timing Diagram.



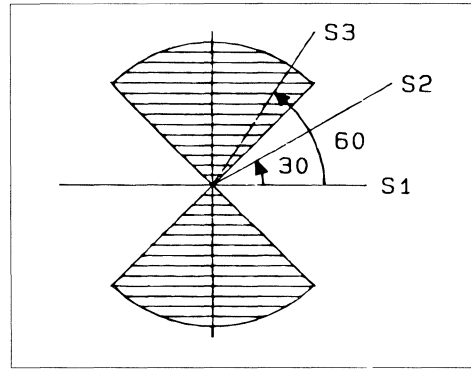
DETERMINING HALL EFFECT SENSOR CODING

The L6231 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig.3, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6231. Note that the rotation in fig. 4 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 4 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6231 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

For example, let us examine the output pattern of a different type of motor (fig. 5). Assuming 90 windows at 180 intervals, then with respect to fig. 4, a similar diagram, fig. 6, results in sensors 60 apart with the windows rotating clockwise. This situation results in a "forward" rotation of the motor.

Figure 4.



Since S3 is the first sensor encountered by the window in fig. 6, this should be used for the L6231 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6231 must go high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By continuing around the diagram, one can develop a pattern which matches that for the L6231.

Figure 5.

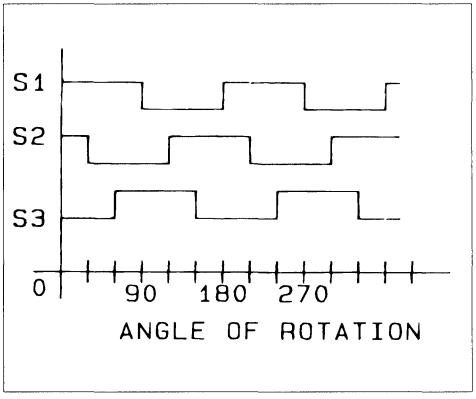
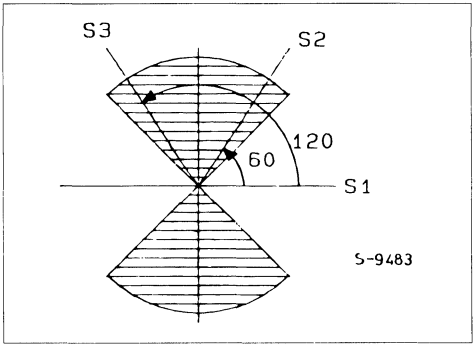


Figure 6.



Thus, the conversion table for this particular motor is :

Motor Sensors	L6230 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6231. Since the L6231 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

SGS-THOMSON MICROELECTRONICS

L6233

PHASE LOCKED FREQUENCY CONTROLLER

ADVANCE DATA

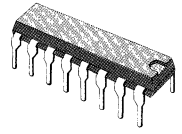
- PRECISION PHASE LOCKED FREQUENCY CONTROL SYSTEM
- XTAL OSCILLATOR
- PROGRAMMABLE REFERENCE FREQUENCY DIVIDERS
- PHASE DETECTOR WITH ABSOLUTE FREQUENCY STEERING
- DIGITAL LOCK INDICATOR
- DOUBLE EDGE OPTION ON THE FREQUENCY FEEDBACK SENSE AMPLIFIER
- TWO HIGH CURRENT OP-AMPS
- 5V REFERENCE OUTPUT

The L6233 is designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these device is universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

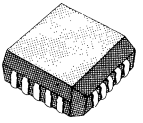
The phase detector on these integrated circuit compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output or other speed detection device. This signal is buffered by a sense amplifier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error and a 5V reference output allows DC operating levels to be accurately set.



DIP-16 Plastic (0.25)

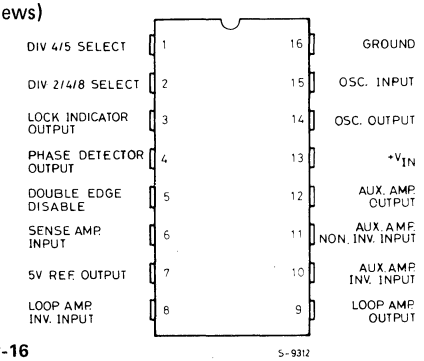


20 PLCC

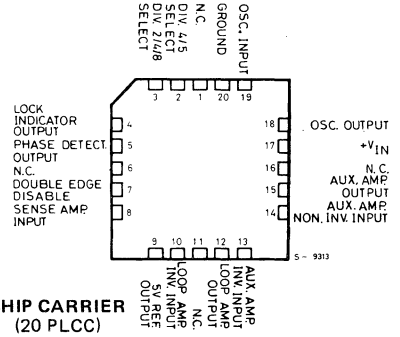
ORDERING NUMBERS: L6233 (DIP-16)
L6233P (20 PLCC)

CONNECTION DIAGRAMS

(Top views)



DIP-16



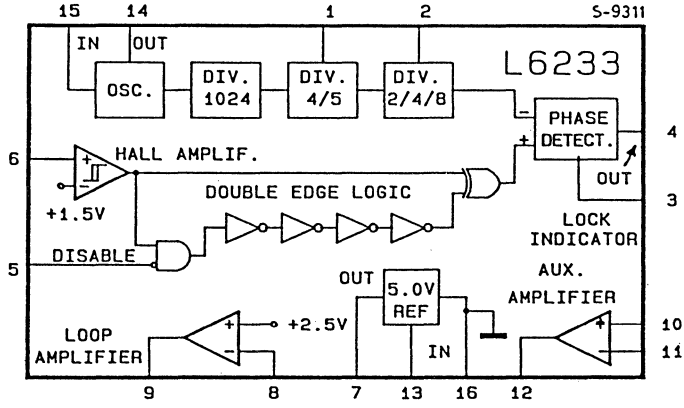
CHIP CARRIER (20 PLCC)

ABSOLUTE MAXIMUM RATINGS

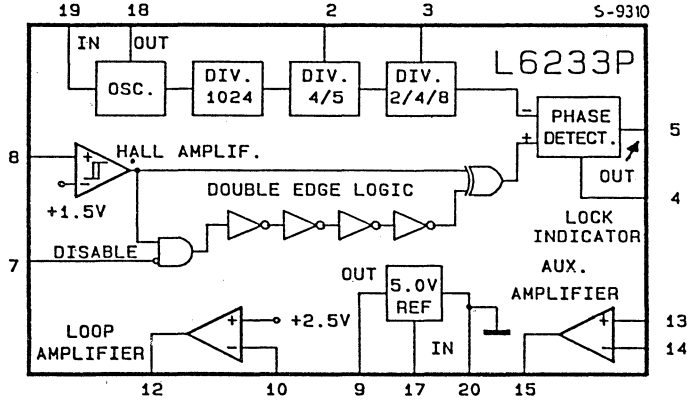
V_s	Supply voltage	14	V
P_{tot}	Power dissipation ($T_{amb} \leqslant 70°C$)	1	W
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

BLOCK DIAGRAMS

(DIP-16)



(PLCC PACKAGE)



ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications hold for T_{amb} = 0°C to +70°C; $+V_{IN}$ = 12V)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_S	Supply current			20		mA
REFERENCE						
V_{REF}	Output voltage		4.75	5.0	5.25	V
ΔV_{REF}	Load Regulation	I_{OUT} = 0 to 7mA		5.0	20	mV
ΔV_{REF}	Line regulation	$+V_{IN}$ = 8 to 12V		2.0	20	mV
I_{SC}	Short circuit current	V_{OUT} = 0V		35		mA
OSCILLATOR						
G_v	DC voltage gain	Oscillator input to oscillator output		16		dB
V_{IB}	Input DC level	Oscillator input pin open, T_j = 25°C		1.3		V
Z_{IN} *	Input impedance	$V_{IN} = V_{IB} \pm 0.5V$, T_j = 25°C		1.6		KΩ
V_o	Output DC level	Oscillator input pin open T_j = 25°C		1.4		V
f_{oMAX}	Maximum operating frequency		10			MHz
DIVIDERS						
f_{oMAX}	Maximum input frequency	Input = $1V_{PP}$ at oscillator input	10			MHz
	Div. 4/5 input current	Input = 5V (Div. by 4)		150	500	μA
		Input = 0V (Div. by 5)	-5.0	0.0	5.0	μA
V_{TH}	Div. 4/5 threshold		0.5	1.6	2.2	V
	Div. 2/4/8 input current	Input = 5V (Div. by 8)		150	500	μA
		Input = 0V (Div. by 2)	-500	-150		μA
	Div. 2/4/8 open circuit voltage	Input current = 0μA (Div. by 4)	1.5	2.5	3.5	V
	Div. by 2 threshold		0.35	0.8		V
	Div. by 4 threshold		1.5		3.5	V
	Div. by 8 threshold	Volts below V_{REF}	0.35	0.8		V
SENSE AMPLIFIER						
V_T	Threshold voltage	Percent of V_{REF}		30		%
H_T	Threshold hysteresis			10		mV
I_b	Input bias current	Input = 1.5V		-0.2		μA
DOUBLE EDGE DISABLE INPUT						
V_i	Input current	Input = 5V (Disabled)		150	500	μA
		Input = 0V (Enabled)	-5.0	0.0	5.0	μA
V_T	Threshold voltage		0.5	1.6	2.2	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
PHASE DETECTOR							
V_{OH}	High output level	Positive Phase/Freq. Error, Volts Below V_{REF}			0.2	0.5	V
V_{OL}	Low output level	Negative Phase/Freq. Error			0.2	0.5	V
V_{OM}	Mid output level	Zero Phase/Freq. Error, Percent of V_{REF}		47	50	53	%
	High level maximum source current	V_{OUT} = 4.3V		2.0	8.0		mA
	Low level maximum sink curr.	V_{OUT} = 0.7V		2.0	5.0		mA
	Mid level output impedance (Note 2)	I_{OUT} = -200 to +200μA	T_j = 25°C		6.0		KΩ
LOCK INDICATOR OUTPUT							
V_{sat}	Saturation voltage	Freq. Error,	I_{OUT} = 5mA		0.3	0.45	V
	Leakage current	Zero Freq. Error	V_{OUT} = 12V		0.1	1.0	μA
LOOP AMPLIFIER							
	NON INV. reference voltage	Percent of V_{REF}		47	50	53	%
I_b	Input bias current	Input = 2.5V		-0.8	-0.2		μA
G_v	Open loop gain			60	75		dB
SVR	Supply voltage rejection	$+V_{IN}$ = 8 to 12V		70	100		dB
I_{SH}	Short circuit current	Source,	V_{OUT} = 0V	16	35		mA
		Sink,	V_{OUT} = 5V	16	30		mA
AUXILIARY OP-AMP							
V_{OS}	Input offset voltage	V_{CM} = 2.5V				8	mV
I_b	Input bias current	V_{CM} = 2.5V			200		mA
I_{os}	Input offset current	V_{CM} = 2.5V			10		mA
G_v	Open loop gain			70	120		dB
SVR	Supply voltage rejection	$+V_{IN}$ = 8 to 12V		70	100		dB
CMR	Common mode rejection	V_{CM} = 0 to 10V		70	100		dB
I_{SH}	Short circuit current	Source,	V_{OUT} = 0V		35		mA
		Sink,	V_{OUT} = 5V		30		mA

* These impedance levels will vary with T_j at about 1700ppm/°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

APPLICATION INFORMATION

Determining the Oscillator Frequency

The frequency at the oscillator is determined by: the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

f_{osc} (Hz) = (Divide Ratio) • (Motor RPM) • (1/60 SEC/MIN) • (No. of Rotor Poles/2) • (× 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option the loop reference frequency can be doubled for a given motor RPM.

Fig. 1 - Recommended Oscillator Configuration Using AT Cut Quartz XTAL

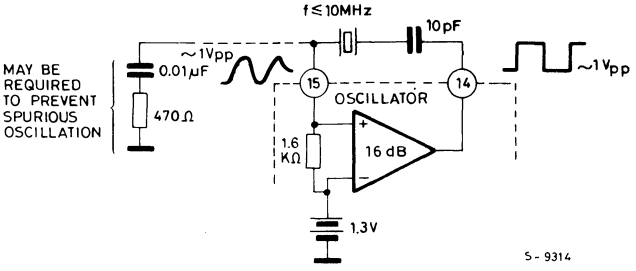


Fig. 2 - External Reference Frequency Input

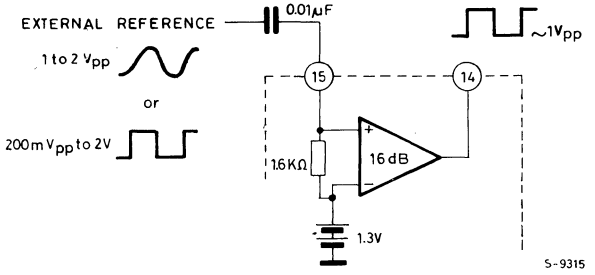
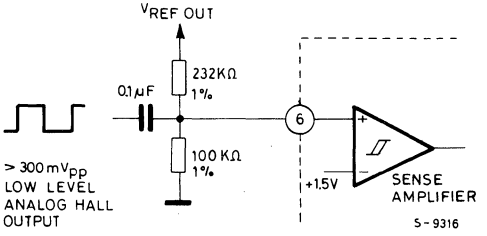


Fig. 3 - Method for Deriving Rotation Feedback Signal From Analog Hall Effect Device



* This signal may require filtering if chopped mode drive scheme is used.

APPLICATION INFORMATION (continued)

Phase detector operation

The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low, the middle state output impedance is high, tipically 6.0KΩ. When there is any static frequency difference between the inputs the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level the remainder of the period. If the phase relationship is reversed then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector, $K\phi$, is $5V/4\pi$, radians, or about 0.4V/radian. The dynamic range of the detector is $\pm 2\pi$ radians.

The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic and the connecting arrows the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge on the-input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from a frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6 or 7.

Fig. 4 - Typical Phase Detector Output Waveforms

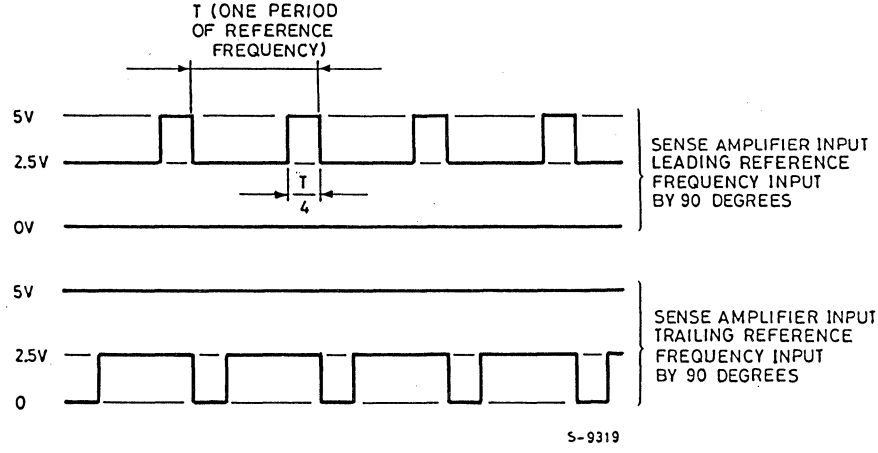


Fig. 5 - Phase Detector State Diagram

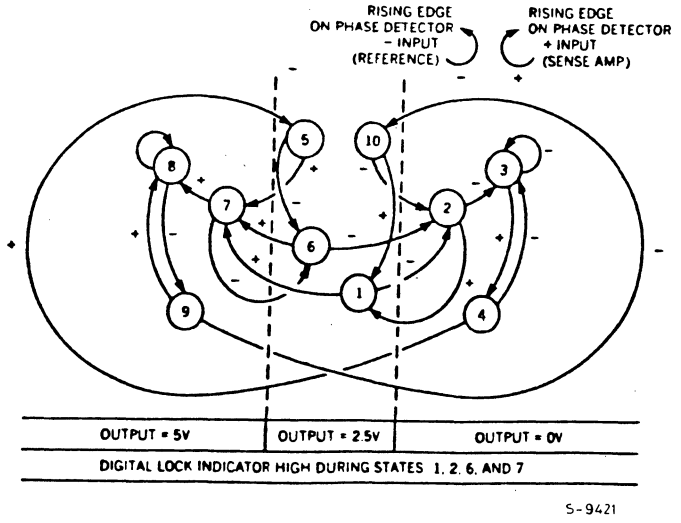
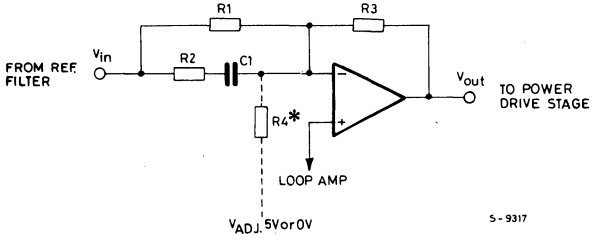


Fig. 6 - Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{R3}{R1} \cdot \frac{1 + S/\omega Z}{1 + S/\omega P}$$

$$\omega P = \frac{1}{R2\,C1}$$

$$\omega Z = \frac{1}{(R1 + R2)\,C1}$$

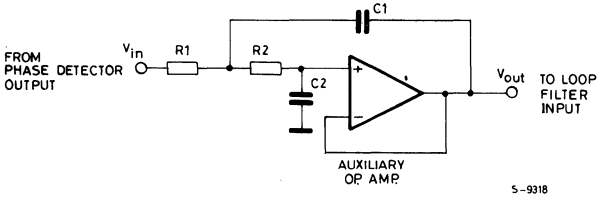
* The statistic phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by :

$$R4 = \frac{2.5V \cdot R3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

$(V_{OUT} - 2.5) > 0$ R4 Goes to 0V
$(V_{OUT} - 2.5) < 0$ R4 Goes to 5.0V

Fig. 7 - Reference Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{1}{1 + \frac{S2}{\omega N} + \frac{S^2}{\omega N^2}}$$

$$\omega N = \frac{1}{\sqrt{R1\,R2\,C1\,C2}}$$

$$\delta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C2}{C1}}\;\frac{R1 + R2}{\sqrt{R1\,R2}}$$

Note: with R1 = R2 $\quad \delta = \sqrt{\frac{C2}{C1}}$

Fig. 8 - Reference Filter Design Aid - Gain Response

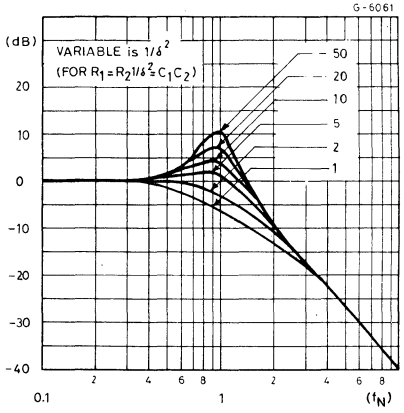
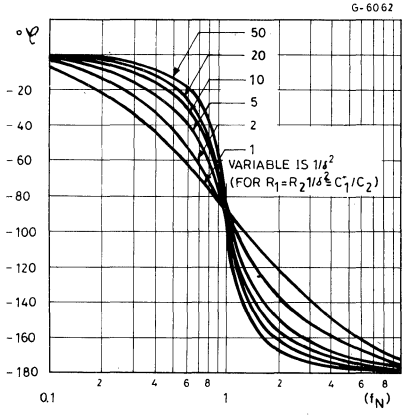


Fig. 9 - Reference Filter Design Aid - Phase Response



SGS-THOMSON MICROELECTRONICS

L6235

R-DAT BRUSHLESS DC MOTOR DRIVER

ADVANCE DATA

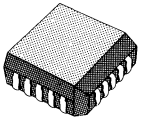
- 400mA OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- INHIBIT FUNCTION
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

The L6235 is single-chip driver for three-phase brushless DC motors capable of delivering 400mA output current with supply voltages to 18V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase drive.

To limit EMI emission the L6235 controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state, reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL system, may be used with the L6235 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

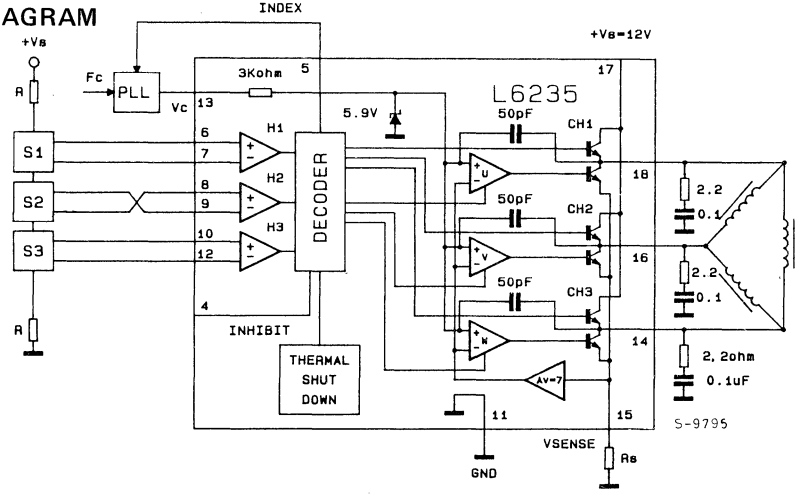
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



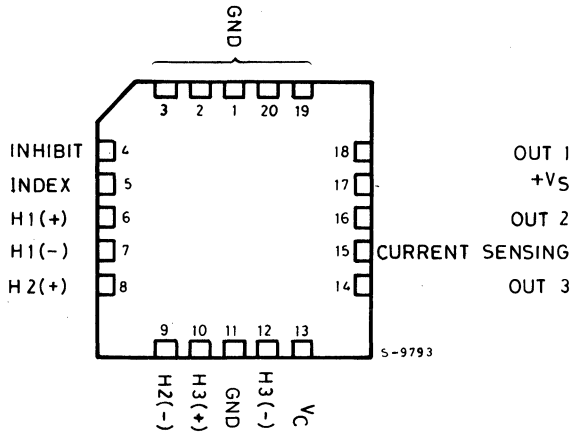
PLCC (15+5)

ORDERING NUMBER: L6235

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	18	V
I_o	Peak output current each channel		
	– non repetitive (100μs)	1.5	A
	– repetitive (80% on - 20% off; t_{on} = 10ms)	500	mA
	– DC operation	400	mA
V_i	Logic and analogic inputs	$+V_s$	
P_{tot}	Total power dissipation at T_{pins} = 50°C	5	W
T_{op}	Operating temperature range	0 to 70	°C
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W
R_{tt}	Transient thermal resistance (t = 2sec.)	max	30	°C/W

PIN FUNCTIONS

N°	NAME	I/O	FUNCTION
4	INHIBIT	I	Output stage inhibit. When this pin is high all three output stages are in a high impedance state!
5	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
6	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
7	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
8	H2 (+)	I	Same as pin 3 for channel 2.
9	H2 (-)	I	Same as pin 4 for channel 2.
10	H3 (+)	I	Same as pin 3 for channel 3.
11	GND		Ground connection.
12	H3 (-)	I	Same as pin 4 for channel 3.
13	V_C	I	Speed control input. Connected to output of PLL in PLL speed control applications.
14	Out 3	O	Output motor drive for phase 3.
15	Sense	I	Current Sensing. Input for load current sense voltage for output stage.
16	Out 2	O	Output motor drive for phase 2.
17	V_S		Motor supply voltage.
18	Out 1	O	Output motor drive for phase 1.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_s = 12V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		10	12		V
I_s	Quiescent supply current	Without Load		30	60	mA
HALL AMPLIFIERS						
V_{CM}	Common mode voltage range		0		10	V
V_{io}	Input offset voltage	V_i = 6V		2	10	mV
I_{ib}	Input bias current	V_i = 6V		2	10	µA
I_{io}	Input offset current	V_i = 6V		0.1		µA
SPEED CONTROL INPUT (V_C)						
V_i	Input voltage range		0		5	V
I_{ib}	Input bias current	$V_C < V_{sens}$		1	5	µA
V_{ic}	Input clamping voltage			5.9		V
INHIBIT INPUT						
V_{IH}	Input high voltage		2		V_s	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current				10	µA
I_{IL}	Input low current			-5	-50	µA
HALL LOGIC OUTPUT						
V_{LO}	Low output voltage	I = 5mA			0.8	V
I_L	Leakage current	V_{CE} = 12V			10	µA
OUTPUT POWER STAGE						
V_{sat}	Total saturation voltage	I_o = 0.15A I_o = 0.4A I_o = 1.0A		2.2 2.5 2.7		V
V_{OSR}	Output voltage slew-rate			100		V/ms
V_{sens}	Sense voltage range		0		0.7	V
THERMAL SHUTDOWN						
T_j	Junction temperature		150			°C
T_H	Hysteresis				30	°C

DESCRIPTION

The L6235 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase drive. When the INHIBIT INPUT is high all three OUTPUTS ARE PLACED in a high - IMPEDANCE STATE.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth table of Fig. 1.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input of the device at pin 10, V_C.

In addition, a 1V offset is added to the speed demand voltage to match the minimum output of the PLL.

An external resistor, R_s, senses the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = \frac{(V_C - 1)}{7\ R_s}$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1)/(7\ I_{max})$$

where V_X is the full scale voltage of V_C.

In this way the V_C/I_{out} characteristics can be modified. Note that V_X max is clamped at 5.9V.

The most important feature of the L6235 is slew rate control. With this device a typical value of 0.1V/μs is achieved, reducing EMI to a very low value.

Another key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the free-wheeling diodes in the acceleration phase and through the motor is steady-state conditions. Torque ripple is also minimized.

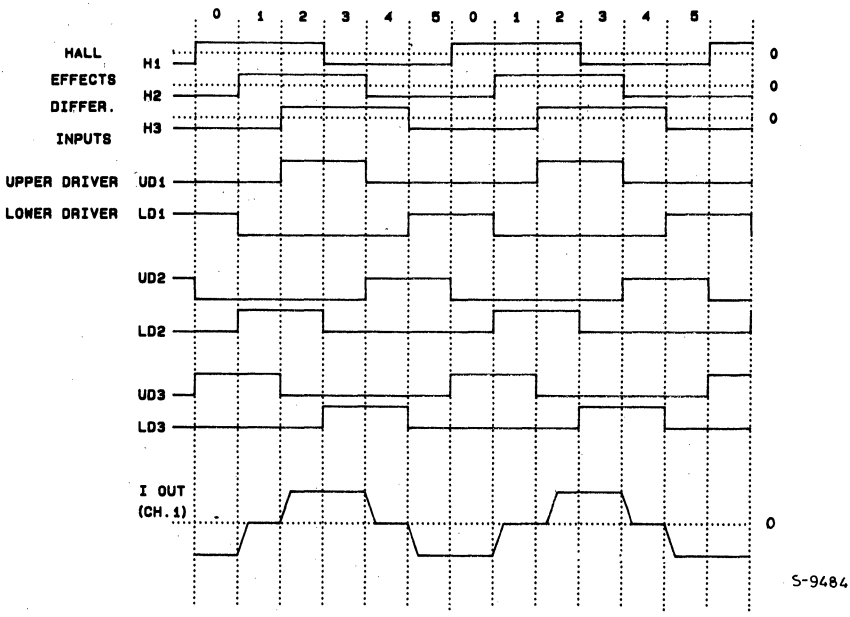
The L6235 can also operate with a brushless motor connected in a star configuration, leaving the centre floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - TRUTH TABLE

HALL EFFECT DIFF. INPUT			UPPER DRIVER STATUS			LOWER DRIVER STATUS		
1 = POSITIVE 0 = NEGATIVE			1 = ON 0 = OFF			1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	0	0	1	1	0	0
1	1	0	0	0	1	0	1	0
1	1	1	1	0	0	0	1	0
0	1	1	1	0	0	0	0	1
0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	0	0

Fig. 2 - Timing diagram

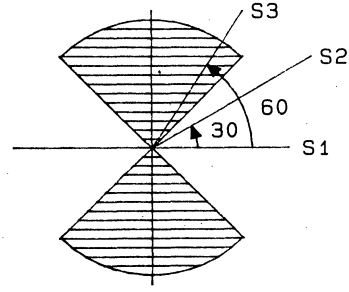


DETERMINING HALL EFFECT SENSOR CODING

The L6335 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 2, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6235. Note that the rotation in fig. 3 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 3 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chosen whose sensor outputs do not match the L6235 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 3



For example, let us examine the output pattern of a different type of motor (fig. 4). Assuming 90 windows at 180 intervals, then with respect to fig. 3, a similar diagram, fig. 5, results in sensors 60 apart with the windows rotating clockwise. The situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 5, this should be used for the L6235 Hall Effect Input, H1. After 30 of rotation CW, the H2 input of the L6235 must go high. The inverse of S1 from the motor would satisfy this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By continuing around the diagram, one can develop a pattern which matches that for the L6235.

Fig. 4

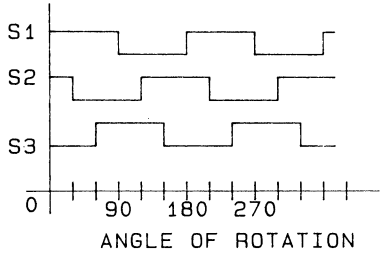
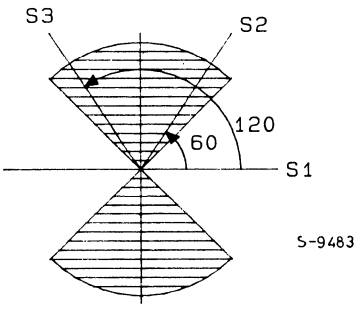


Fig. 5

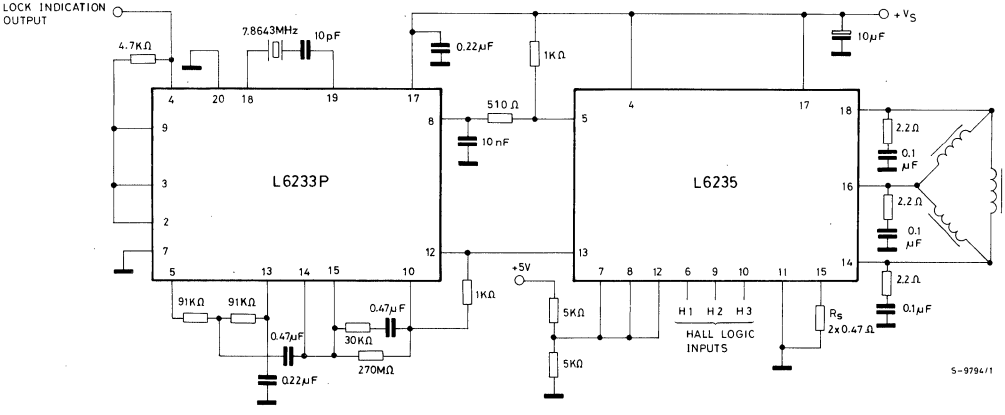


Thus the conversion table for this particular motor is:

Motor Sensors	L6235 Inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 an actual inverter gate is not necessary with the L6235. Since the L6235 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

Fig. 6 - Application circuit using the L6233 PLL-Controller



SGS-THOMSON MICROELECTRONICS

L6236

BIDIRECTIONAL R-DAT BRUSHLESS DC MOTOR DRIVER

ADVANCE DATA

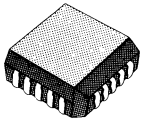
- 400mA OUTPUT CURRENT, CONTROLLED IN LINEAR MODE
- COMPATIBLE WITH ANI F-TO-V CONVERTER AND PLL SPEED CONTROL SYSTEM
- SLEW RATE LIMITING FOR EMI REDUCTION
- CONNECTS DIRECTLY TO HALL EFFECT CELLS
- THERMAL SHUTDOWN WITH HYSTERESIS
- THREE-STATE OPERATION ALLOWS NEGLIGIBLE POWER DISSIPATION DURING 1/3f CYCLE
- INTERNAL PROTECTION DIODES
- FEW EXTERNAL COMPONENTS

The L6236 is a single-chip driver for three-phase brushless DC motors capable of delivering 400mA output current with supply voltages to 18V. Designed to accept differential input from the Hall effect sensors, the device drives the three phases of a brushless DC motor and includes all the commutation logic required for a three phase bidirectional drive. Both delta and wye configurations may be used.

To limit EMI esmission the L6236 operates in a linear mode and controls the rise and fall times of the output stage. In addition the device is designed to limit power dissipation: during recirculation the output stage is switched to an off state reducing dissipation to a very low value and minimizing torque ripple.

A speed control input controls the base current to the lower transistors to limit the motor current and hence control the speed. Any type of speed control system, including F to V and PLL systems, may be used with the L6236 by providing an analog signal at this input. The motor current may be sensed by an external resistor connected to a sensing pin on the device.

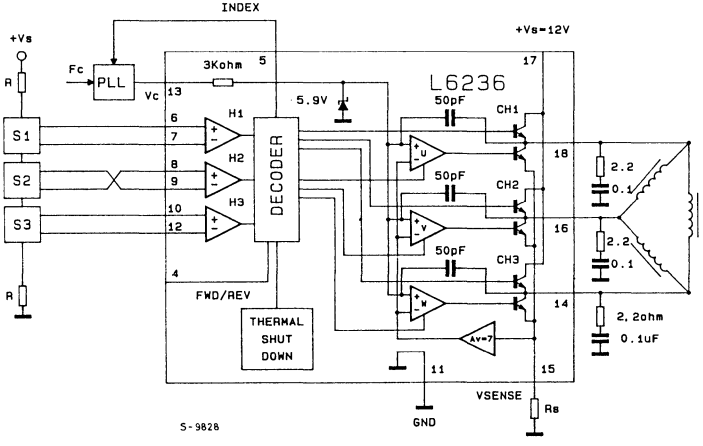
The power stage of the device is designed to eliminate the possibility of simultaneous conduction of the upper and lower power transistors of one output driver, when operating in the right loop.



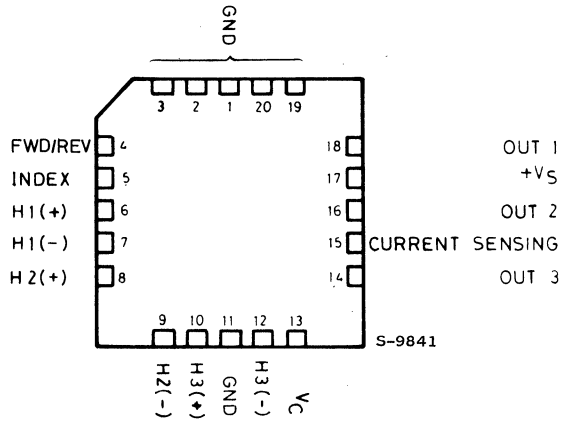
PLCC (15 + 5)

ORDERING NUMBER: L6236

BLOCK DIAGRAM



CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	18	V
I_o	Peak output current each channel		
	– non repetitive (100μs)	1.5	A
	– repetitive (80% on - 20% off; t_{on} = 10ms)	500	mA
	– DC operation	400	mA
V_i	Logic and analogic inputs	$+V_s$	
P_{tot}	Total power dissipation at T_{pins} = 50°C	5	W
T_{op}	Operating temperature range	0 to 70	°C
T_j, T_{stg}	Storage and junction temperature	-40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W
$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	20	°C/W
R_{tt}	Transient thermal resistance (t = 2sec.)	max	30	°C/W

PIN FUNCTIONS

N°	NAME	I/O	FUNCTION
4	FWD/REV	I	Direction Control. When this pin is low, the motor will run in the forward direction. A high will drive the motor in the reverse direction. Direction is defined by the positive of the sensors in the motor.
5	INDEX	O	Signal pulse proportional to the motor speed. In PLL speed control applications, this is the feedback to the PLL. One pulse per electrical rotation. This is an open collector output.
6	H1 (+)	I	Positive input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
7	H1 (-)	I	Negative input of differential amplifier on channel 1. Interfaces with Hall Effect sensor, S1, from motor.
8	H2 (+)	I	Same as pin 3 for channel 2.
9	H2 (-)	I	Same as pin 4 for channel 2.
10	H3 (+)	I	Same as pin 3 for channel 3.
11	GND		Ground connection.
12	H3 (-)	I	Same as pin 4 for channel 3.
13	V_C	I	Speed control input. Connected to output of PLL in PLL speed control applications.
14	OUT3	O	Output motor drive for phase 3.
15	SENSE	I	Current Sensing. Input for load current sense voltage for output stage.
16	OUT2	O	Output motor drive for phase 2.
17	V_S		Motor supply voltage.
18	OUT1	O	Output motor drive for phase 1.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C; V_s = 12V unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		10	12		V
I_s	Quiescent supply current			30	60	mA
HALL AMPLIFIERS						
V_{CM}	Common mode voltage range		0		10	V
V_{io}	Input offset voltage	V_i = 6V		2	10	mV
I_{ib}	Input bias current	V_i = 6V		2	10	μA
I_{io}	Input offset current	V_i = 6V		0.1		μA
SPEED CONTROL INPUT (V_C)						
V_i	Input voltage range		0		5	V
I_{ib}	Input bias current	$V_C < V_{sens}$		1	5	μA
V_{ic}	Input clamping voltage			5.9		V
FWD/REVERSE INPUT						
V_{IH}	Input high voltage		2		V_s	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current				10	μA
I_{IL}	Input low current			-5	-50	μA
HALL LOGIC OUTPUT						
V_{LO}	Low output voltage	I = 5mA			0.8	V
I_L	Leakage current	V_{CE} = 12V			10	μA
OUTPUT POWER STAGE						
V_{sat}	Total saturation voltage	I_o = 0.15A I_o = 0.4A I_o = 1.0A		2.2 2.5 2.7		V
$\dot{V}_{OSR}$	Output voltage slew-rate			100		V/ms
V_{sens}	Sense voltage range		0		0.7	V
THERMAL SHUTDOWN						
T_j	Junction temperature		150			°C
T_H	Hysteresis				30	°C

DESCRIPTION

The L6236 is a three-phase brushless motor driver IC containing all the power stages and commutation logic required for a three-phase bidirectional drive.

Logic signals from the motor's Hall effect sensors are decoded to generate the correct driving sequence according to the truth-table of Fig. 1.

The direction of rotation is controlled by the forward/reverse input (pin 1). When this pin is at a low level the motor rotates in the forward direction.

When one of the push-pull output drivers is activated the upper transistor is always in saturation while the lower transistor is controlled in linear mode to set the desired speed in steady state conditions.

In PLL speed control applications the device provides a signal proportional to the motor speed at pin 2 (it is the buffered H1 input). The output of the PLL is connected to the speed control input on the device at pin 10, V_C.

In addition, a 1V offset is added to the speed demand voltage to match the minimum output on the PLL.

An external resistor, R_s, sense the output stage current. The sensing voltage across this resistor is amplified in the device by a factor of 7 to allow a reduction in the voltage drop in the resistor.

The amplified sensing voltage is then compared with the speed demand signal from the PLL and the resulting error signal sets the amplifier output accordingly.

The output current is related to the speed control voltage by:

$$I_o = (V_C - 1)/7\ R_s$$

The value of the sensing resistor is given by:

$$R_s = (V_X - 1)/(7\ I_{max})$$

where V_X is the full scale voltage of V_C.

In this way the V_C/I_{out} characteristics can be modified. Note that V_X max is clamped at 5.9V.

The most important feature of the L6236 is slew rate control. With this device a typical value of 0.1V/μs is achieved, reducing EMI to a very low value.

In a delta configuration a key feature is three-state operation; when the current is recirculating the corresponding phase driver is switched off and power dissipation is negligible. Current recirculates through the integrated free-wheeling diodes in the acceleration phase and through the motor in steady-state conditions. Torque ripple is also minimized.

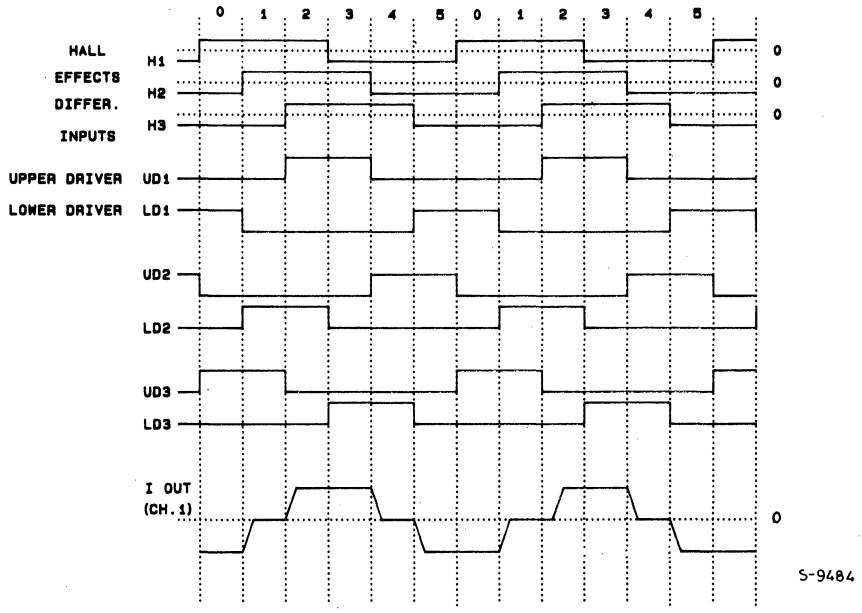
The L6236 can also operate with a brushless motor connected in a star configuration, leaving the center floating.

The Hall inputs are ground compatible comparators and can work with direct active digital Hall signals on three terminals (of the same polarity) and a TTL level on the other three terminals.

Fig. 1 - **TRUTH TABLE FOR FORWARD ROTATION**

HALL EFFECT DIFF. INPUT			UPPER DRIVER STATUS			LOWER DRIVER STATUS		
1 = POSITIVE 0 = NEGATIVE			1 = ON 0 = OFF			1 = ON 0 = OFF		
H1	H2	H3	UD1	UD2	UD3	LD1	LD2	LD3
1	0	0	1	0	0	0	0	1
1	1	0	0	1	0	0	0	1
1	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
0	0	1	0	0	1	0	1	0
0	0	0	1	0	0	0	1	0

Fig. 2 - Timing diagram

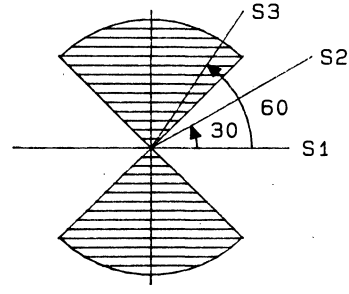


DETERMINING HALL EFFECT SENSOR CODING

The L6236 assumes that the positioning of the Hall Effect sensors in a three-phase brushless DC bipolar motor are at 30 intervals. One can imagine two "windows" on the rotor each of which is 90 wide and 180 apart, see fig. 4. As a window passes over a sensor, the sensor output goes high. The timing diagram, fig. 2, shows the waveforms produced. These waveforms must appear at the Hall Effect Inputs of the L6236. Note that the rotation in fig. 3 must be counter-clockwise for forward rotation of the motor in whatever manner that is defined for the motor.

Fig. 3 is a stylized concept for determining the Hall Effect code pattern and does not reflect the actual direction of rotation of the motor in a physical sense. If a motor is chose whose sensor outputs do not match the L6236 desired input pattern, a signal set conversion must be determined. It is helpful to visualize this by developing a diagram similar to that of fig. 4.

Fig. 3



For example, let us examine the output pattern of a different type of motor (fig. 4). Assuming 90 windows at 180 intervals, then with respect to fig. 3, a similar diagram, fig. 5, results in sensors 60 apart with the windows rotating clockwise. The situation results in a "forward" rotation of the motor.

Since S3 is the first sensor encountered by the window in fig. 5, this should be used for the L6236 Hall Effect Input H1. After 30 of rotation CW, the H2 input of the L6236 must go high. The inverse of S1 from the motor would satisfly this. After an additional 30 of rotation, the H3 input must go high. The S2 sensor is encountered by the window. Thus, S2 is applied to this input, H3. By countinuing around the diagram, one can develop a pattern which matches that for the L6236.

Fig. 4

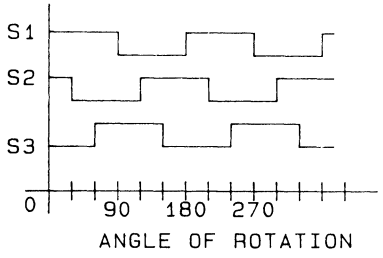
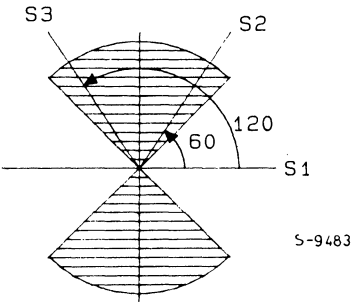


Fig. 5

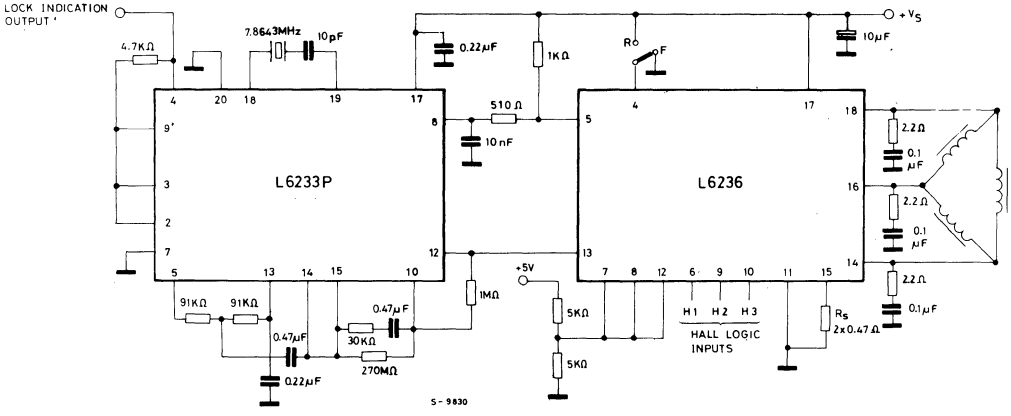


Thus the conversione table for this particular motor is:

Motor Sensors	L6236 inputs
S3	H1
S1	H2
S2	H3

Note, for the inverted signal from S1 actual inverter gate is not necessary with the L6236. Since the L6236 has differential inputs, the negative input pin may be used. Therefore, with TTL compatible Hall Effect sensors, the positive input is connected to a reference point along with the other negative inputs.

Fig. 6 - Application circuit using the L6233 PLL-Controller

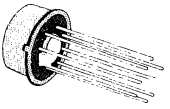


HIGH SPEED OPERATIONAL AMPLIFIER

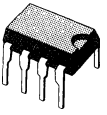
ADVANCE DATA

- SUITABLE FOR VIDEO APPLICATIONS
- SLEW RATE 150 V/us (AV = 20 dB AND I_{set} = 100 µA)
- UNITY GAIN BANDWIDTH (45 MHz TYP)
- LARGE SIGNAL BANDWIDTH (20 MHz TYP)
- LOW NOISE (5 nV/ √Hz)
- LOW OFFSET VOLTAGE
- PROGRAMMABLE OUTPUT PEAK CURRENT
- NO EXTERNAL COMPENSATION FOR AV = 20 dB OR HIGHER

TO-99 (8 Pins)



MINIDIP
(plastic)



ORDER CODES : L6495 (TO99)
L6495 DP (MINIDIP)

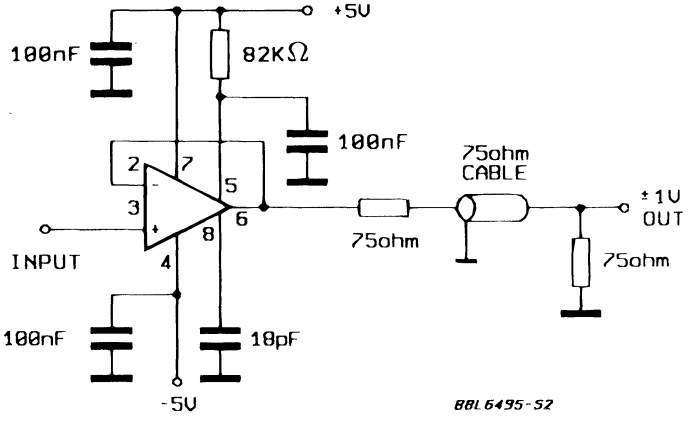
DESCRIPTION

The L6495 is a high performance monolithic operational amplifier with wideband and high slew rate. The frequency compensation is built into the chip for closed loop gain higher than 20 dB.

Large gain bandwidth product and high slew rate make the L6495 ideally suited for wideband signal amplification or switching, in vidéo gain blocks, line driver circuitry, driving capacitive loads and generally for all high frequency applications.

The L6495 is available in both minidip and metal can 8 pin.

BLOCK DIAGRAM



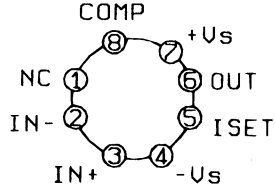
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_s	Supply Voltage		± 10	V
V_{is}	Differential Input Voltage		± 7	V
V_i	Input Voltage		$-V_s - 0.5$ $+V_s + 0.5$	V V
I_o	Output Current		±100	mA
T_{op}	Operating Temperature		0 to 70	°C
P_{tot}	Power Dissipation at T_{amb} = 70 °C	Minidip T0-99	600 500	mW mW
T_j	Junction Temperature		– 55 to 150	°C
T_{stg}	Storage Temperature		– 55 to 125	°C

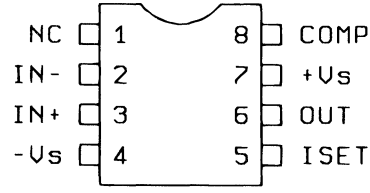
THERMAL DATA

			T0-99	Minidip
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-amb	Max	155 °C/W	120 °C/W

CONNECTION DIAGRAMS



88L6495-C1



88L6495-C2

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C ; V_s = ± 5 V ; I_{set} = 100 µA ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 3	± 5	± 9	V
I_s	Supply Current	NO LOAD		10	12	mA
I_b	Input Bias Current			8	10	µA
R_{in}	Input Resistance	A_V = 20 dB		100		KΩ
C_{in}	Input Capacitance	A_V = 20 dB		5		pF
V_{os}	Offset Voltage			2	5	mV
$\frac{\Delta V_{os}}{\Delta T}$	Average Offset Voltage Drift	0 to 70 °C		10	30	µV/°C
I_{os}	Offset Current				1	µA
VCM	Common Mode Voltage Range			± 3		V
G_v	Open Loop Voltage Gain	ΔV_o = 5 V ; R_L = 2 KΩ		72		dB
B	Large Signal Bandwidth	A_V = 20 dB (*)		20		MHz
GBW	Gain Bandwidth Product	A_V = 0 dB C_{comp} = 18 pF ;	30	45		MHz
e_N	Equivalent Input Noise Voltage	1 KHz to 500 KHz		5		nV/VHz
V_o	Output Voltage Swing	R_L = 2 KΩ		± 4		V
I_o	Output Current		± 20	± 30		mA
R_o	Output Resistance	Open Loop		30		Ω
S_R	Slew Rate	A_V = 20 dB	100	150		V/µs
S_R	Slew Rate	C_{comp} = 18 pF A_V = 0 dB		40		V/µs
CMRR	Common Mode Reject. Ratio		70			dB
SVR + RATIO	Power Supply Rejection (positive supply)		70			dB
SVR – RATIO	Power Supply Rejection (negative supply)		60			dB
t_r	Rise Time	A_V = 20 dB		20		ns

(*) Test circuit of Fig. 4.

Figure 1 : Output Current vs. I_{set}.

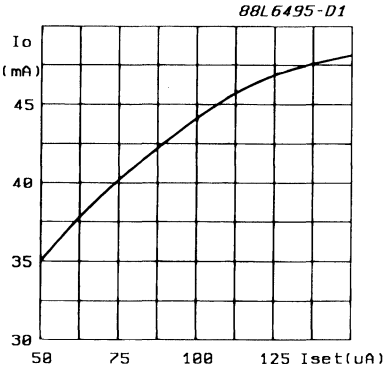


Figure 2 : Non Inverting Amplifier Configuration (AV = 20 dB).

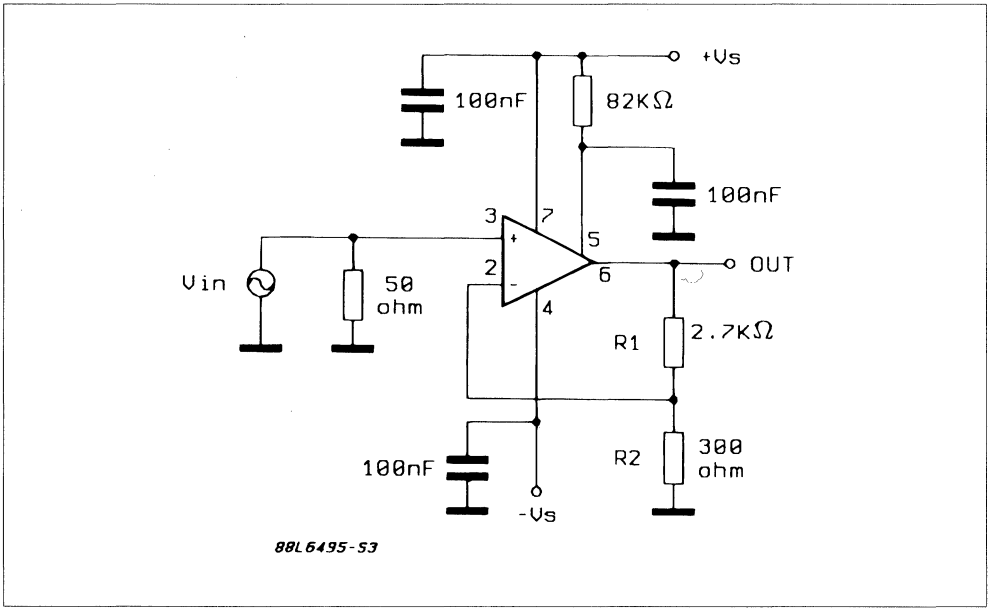
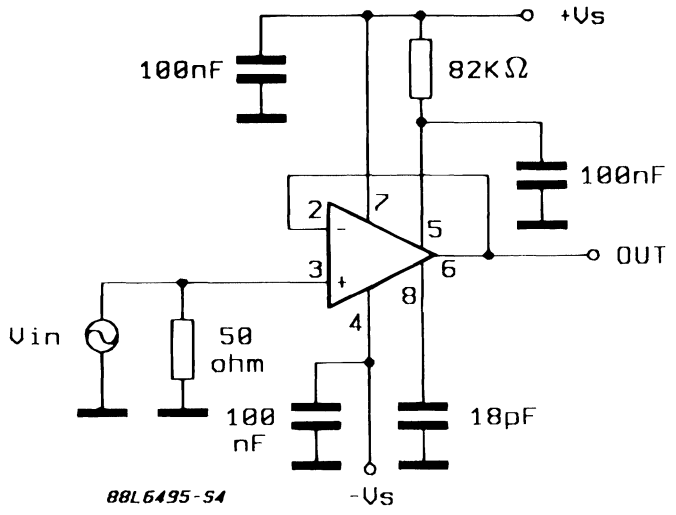


Figure 3 : Buffer Configuration (AV = 0 dB).



An external compensation capacitor at pin 8 is needed if the loop gain of the operational amplifier is less then 8.

Figure 4 : Bandwidth Test Circuit (closed loop gain of the L6495 = 20 dB).

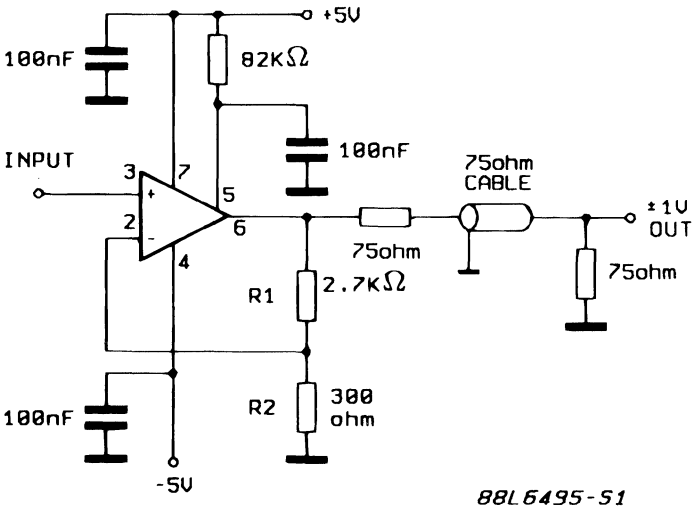
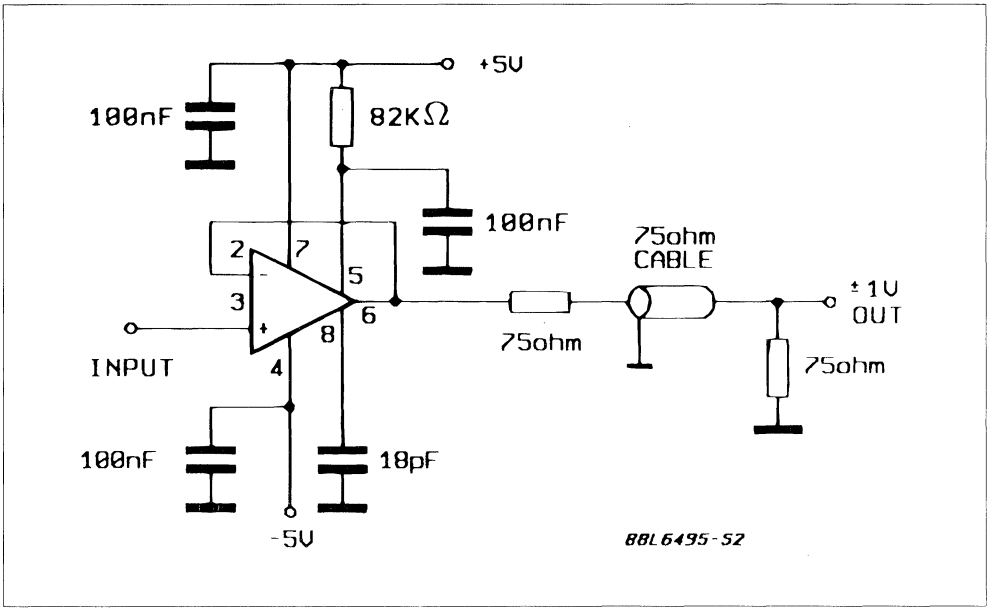


Figure 5 : Bandwidth Test Circuit (closed loop gain of the L6495 = 0 dB).



SGS-THOMSON MICROELECTRONICS

L6503

HAMMER SOLENOID CONTROLLER

PRELIMINARY DATA

- DRIVES FOUR DARLINGTONS WITH UP TO 2.5 mA DRIVE CURRENT
- FEEDBACK LOOP CONTROLS DARLINGTON CURRENT
- PRESETTABLE CONDUCTION TIME
- LATCHED μC-COMPATIBLE INPUTS
- DIAGNOSTIC CIRCUITRY

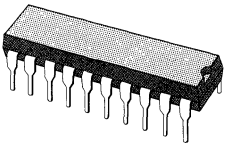
DESCRIPTION

Designed primarily for selenoid driving applications, the L6503 Hammer Solenoid Controller includes all the circuitry needed to control four darlington power devices or a quad darlington array such as the SGS L7180.

The device is controlled by four latched logic inputs, which may be connected directly to a microcomputer chip, plus an analog input which sets the load current. Additionally, the conduction time of the outputs is controlled by a clock input which drives internal timers.

Fault conditions may be detected thanks to diagnostic circuitry which allows the control micro to read (serially) the load current status of the external darlingtons.

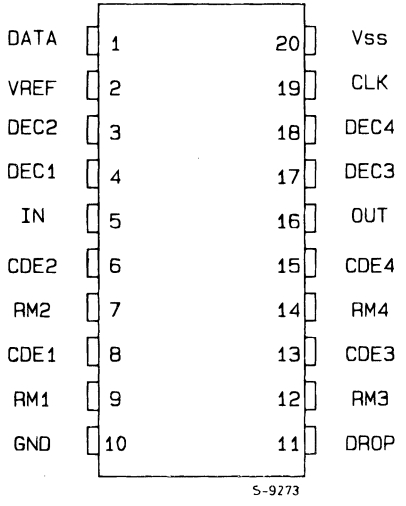
Assembled in a 20-pin DIP package, the L6503 operates on a single 5 V supply and is suitable for computer printers, solenoid valves and similar applications.



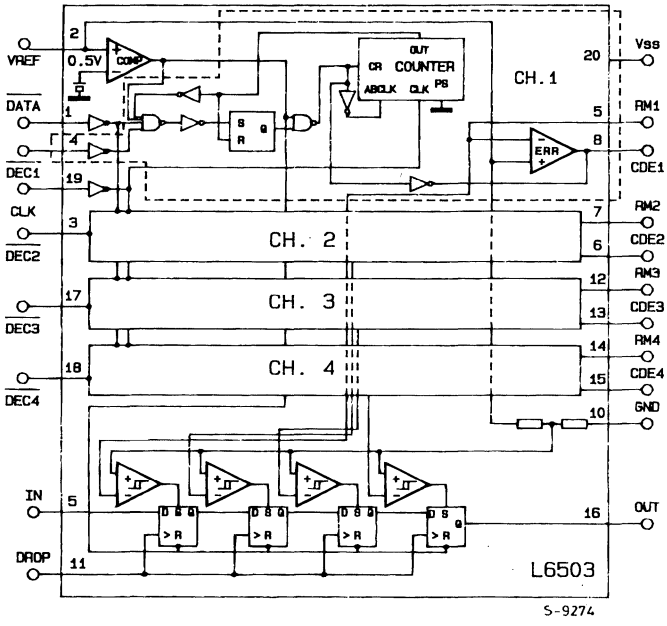
DIP-20 Plastic
(0.4)

ORDER CODE : L6503

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{ss}	Supply Voltage	7	V
I_{CDE}	Output Current	10	mA
V_i	Input Voltage (for analog and logic inputs)	0 to V_{ss} – 0.5	V
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

PIN FUNCTIONS DESCRIPTION

N°	Name	Function
1	$\overline{DATA}$	Latches control command into the four inputs DEC1-DEC4 on the high-low transition.
2	V_{ref}	Analog reference input which sets the load current for all four channels ; when lower than 0.5 V resets the logic circuitry.
3	$\overline{DEC2}$	Data input for channel 2. Data is latched on the high-low transition of the DATA input.
4	$\overline{DEC1}$	Data Input for Channel 1.
5	IN	Input for diagnostic shift register used to cascade several device.
6	CDE2	Channel 2 output (connect to base ofdarlington). Up to 2.5 mA drive.
7	RM2	Feedback input from sensing resistor of channel 2 darlington.
8	CDE1	Channel 1 Output .
9	RM1	Feedback input for channel 1 sense resistor .
10	GND	Ground.
11	DROP	Clock Input for Diagnostic Register.
12	RM3	Feedback input for channel 3 sense resistor.
13	CDE3	Channel 3 Output.
14	RM4	Feedback input for channel 4 sense resistor.
15	CDE4	Channel 4 Output.
16	OUT	Output of Diagnostic Register.
17	$\overline{DEC3}$	Input for Channel 3.
18	$\overline{DEC4}$	Input for Channel 4.
19	CLK	Input for clock signal which sets conduction time for all four channels. $T_{on} = 128/f_{CLK}$.
20	V_{ss}	5 V Supply Input Voltage.

FUNCTIONAL DESCRIPTION

The L6503 Hammer Solenoid Controller is designed to control a quad darlington array, such as the SGS-THOMSON L7180, in solenoid driving applications.

Compatible with 5 V microcomputer and peripheral chips, the L6503 is controlled by four logic inputs - one per channel ($\overline{DEC1} - \overline{DEC4}$) - which are latched by a high-low transition on the DATA input.

When one of the channels is activated the corresponding darlington is driven, with up to 2.5 mA drive current. The conduction period is determined by the frequency applied to the CLK input which clocks the 7-bit timer in each channel. The conduction time is therefore 128/fCLK. Typically the CLK frequency will be of the order of 100KHz but the L6503's internal logic will operate at any clock rate within the range of practical conduction times.

During the conduction period the load current is controlled by feedback from a sense resistor in the darlington's emitter and set by the voltage applied to the V_{ref} input. The current depends on both the values of V_{ref} and the sensing resistor :
$I = V_{ref}/R_{sense}$.

The control microcomputer may verify correct operation of the complete drive subsystem thanks to a diagnostic circuit in the L6503. A four bit PISO shift register in the device monitors the feedback signals from the four output darlingtons and may be read serially after each command to check that the loads were driven.

Typically, this register, clocked by the DROP input, will be read a short time after each drive command has been latched into the device.

The input of this register (IN) is available externally so that multiple devices may be cascaded.

ELECTRICAL CHARACTERISTICS (V_{SS} = 5 V , T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ss}	Supply Voltage	T_j = 0 to 70 °C	4.75	5	5.25	V
I_{ss}	Total Supply Current	I_{CDE} = 2 mA All Channels On		75	90	mA
V_{REF}	Input Voltage Reference		1		2.4	V
V_{REF}	Reset Logic Function		0.3		0.65	V
I_{REF}	Input BIAS Reference Current	V_{REF} = 0 to 2.4 V			– 5	µA
V_i	Input Voltage (pin 1, 3, 4, 5, 11, 17, 18, 19)	V_{iL}			0.4	V
		V_{iH}	2.7			
V_{out}	Output Logic Voltage (pin 16)	V_{OL} I_{OUT} = + 1.6 mA			0.4	V
		V_{OH} I_{OUT} = – 100 µA	2.7			
I_b	Input Bias Current (pin 1, 3, 4, 5, 11, 17, 18, 19)	V_{IL}			– 100	µA
		V_{IH}			± 10	
I_b	Input Bias Current (pin 7, 9, 12, 14)	1 ≤ V_{RM} ≤ 2.4 V			– 100	µA
I_{CDE}	Output Current (pin 6, 8, 13, 15)	V_{OUT} = V_{SS} – 0.5 V	2.5			mA
	Output Voltage Range (pin 6, 8, 13, 15)	V_{OL}			0.2	V
		V_{OH}	V_{ss} – 0.5			
	Error Amplifier Input Offset Voltage	1 V ≤ V_{REF} ≤ 2.4 V			± 10	mV

TIMING SECTION

	Data Ability Time t		160			ns
	Data to CDE Delay Time t1 (1)	V_{RM} = 0 V		0.8	1.5	µs
	Clock to CDE Delay Time t2 (1)	V_{RM} = 0 V		7	10	µs
	Reset Time t3		1.9			µs
	Reset to CDE Delay Time t4 (1)				1.3	µ s
	Clock Frequency				100	KHz
	Low Level Clock State t5 (1)		500			ns
	RM to OUT Delay Time t6 (1)				3	µs
	Drop Frequency				500	KHz
	Low Level Drop State t7		500			ns
	Reset to Output Delay Time t8 (1)				1.3	µs
	Drop to in Delay•Time t9 (1)				1.0	µs

(1) 100% Tested

Figure 1 : Application Diagram.

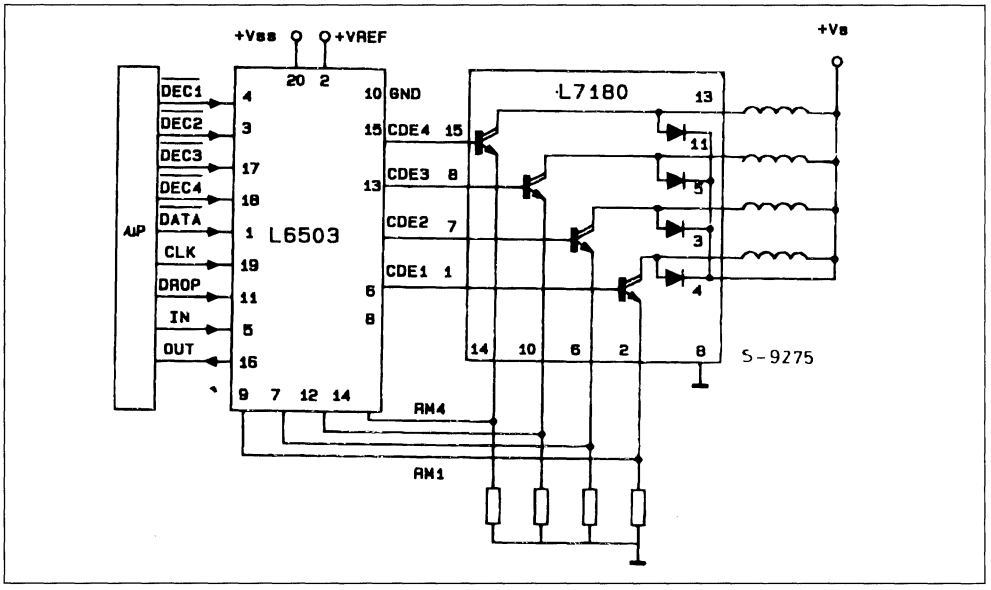
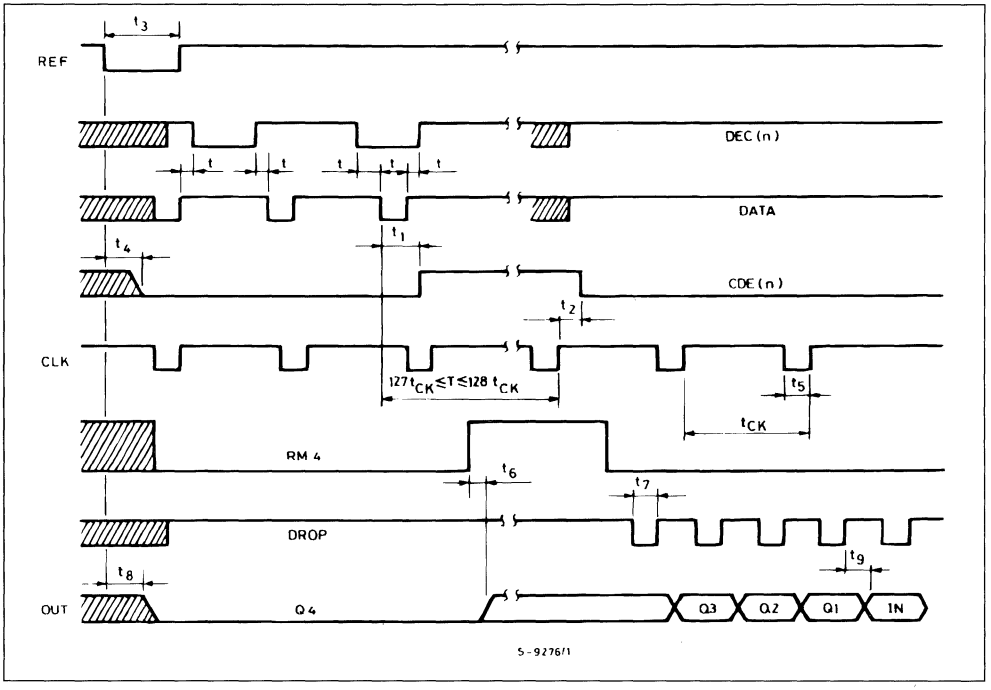


Figure 2 : Timing Diagram.



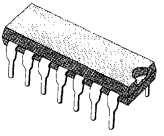
SOLENOID CONTROLLER

PRELIMINARY DATA

- SWITCH MODE CURRENT REGULATION
- TTL COMPATIBLE LOGIC INPUTS
- DRIVES ONE OR TWO EXTERNAL POWER TRANSISTORS
- VERY PRECISE ON-CHIP REFERENCE
- ANALOG CURRENT CONTROL INPUT
- ADJUSTABLE CURRENT RISE AND FALL TIME CONTROL INDEPENDENT OF SOLENOID SUPPLY VOLTAGE
- UNDERVOLTAGE LOCKOUT

DESCRIPTION

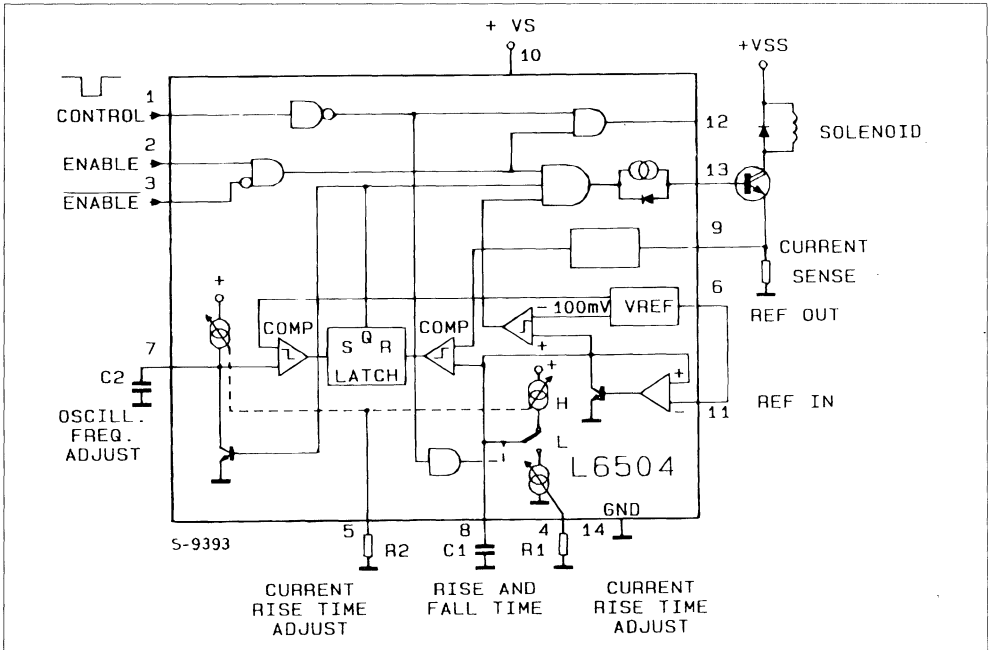
Designed for use with one external power transistor, the L6504 drives the hammer solenoid in daisy-wheel printers and typewrites. The device is controlled by three logic inputs and features switchmode regulation of the load current. A key feature of the device is that the rise and fall time of the load current can be set by external components. Additionally an analog input allows the load current to be set by an external DC voltage. An undervoltage lockout circuit guarantees the output off state for switch on phase.



DIP-14 Plastic
(0.25)

ORDER CODE : L6504

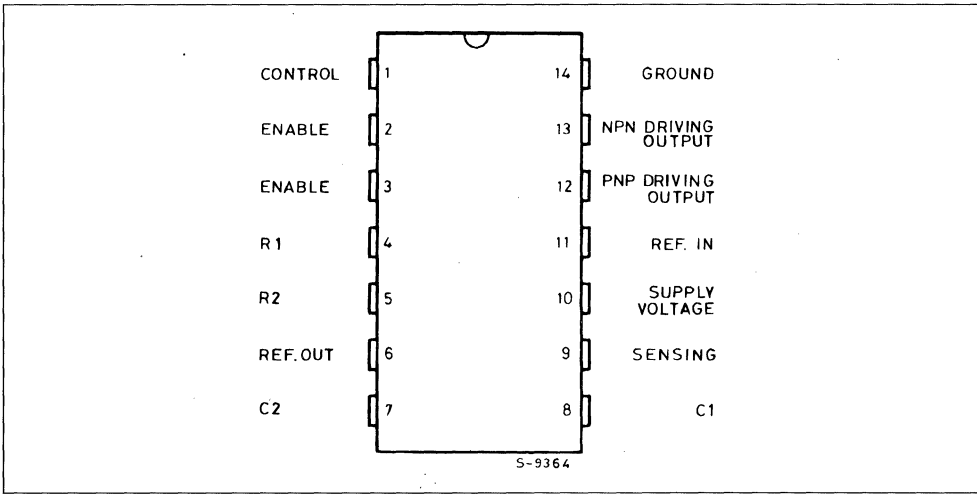
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	10	V
$V_{2,3}$	Enable Input Voltage Range	– 0.3 to 7	V
V_1	Control Input Voltage Range	– 0.3 to 7	V
V_9	Sense Voltage	– 0.3 to 2	V
I_6	Reference Output Current	2	mA
V_{11}	External Reference Voltage	2	V
T_{stg}	Storage Temperature	– 55 to 150	°C
T_j	Junction Temperature	– 55 to 150	°C
T_{op}	Operating Temperature	0 to 85	°C

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

PIN FUNCTION

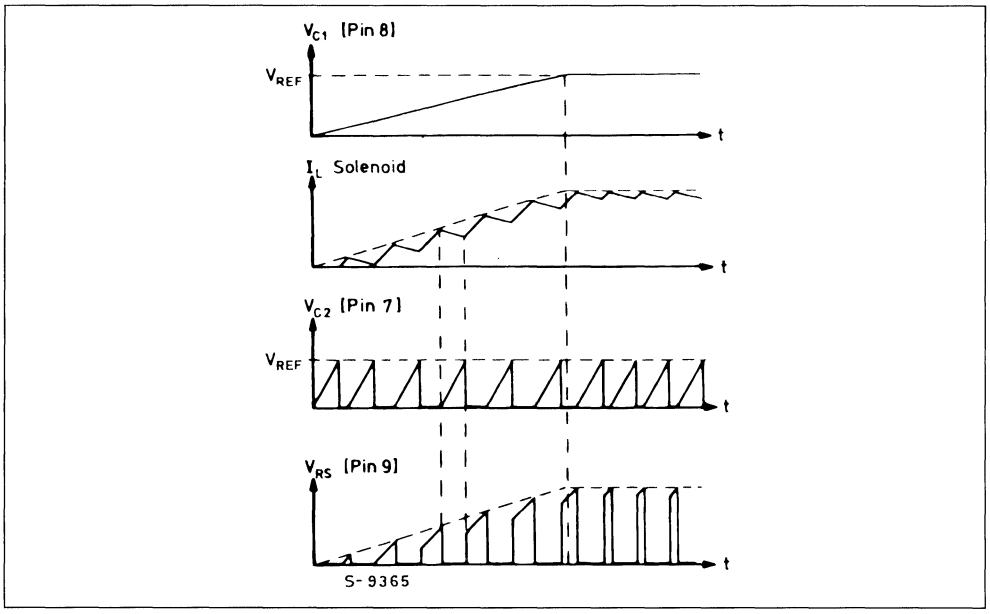
N°	Name	Function
1	CONTROL	TTL Compatible Control Input. A low level activates the output, driving the load. Internal Pull-up Resistor.
2	ENABLE	TTL Compatible Enable Input. A low level disables the output stage.
3	$\overline{\text{ENABLE}}$	TTL Compatible Enable Input. A high level disables the output stage.
4	R1	The value of this resistor (*) sets slope of trailing edge of load current.
5	R2	The value of this resistor (*) sets slope of leading edge of load current.
6	REFERENCE OUT	Output for Internal Reference Voltage.
7	C2	The value of this capacitor sets the duration of power transistor switch off time.
8	C1	The value of this capacitor sets slope of leading and trailing edge of load current.
9	SENSING	Connection for Load Current Sense Resistor. Value sets the maximum load current : $I = V_{ref}/R_s$.
10	SUPPLY VOLTAGE	Supply Voltage Input.
11	REFERENCE IN	Input for External Reference Voltage to Control Load Current by DC-level.
12	PNP DRIVING OUTPUT	Output to Control External PNP-transistor for Fast Current Discharge.
13	NPN DRIVING OUTPUT	Output for Basecharge and Discharge of External Power Transistor.
14	GROUND	Ground

(*) Value between 10 kΩ and 200 kΩ (or open).

ELECTRICAL CHARACTERISTICS

N°	Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
1 .	V_s	Operating Supply Voltage	10		4.5		10	V
2 .	V_{sth}	Supply Voltage Threshold For Output Switch-off	10	V_{CH} = LOW V_E = HIGH	2.96	3.7	4.45	V
3 .	I_s	Quiescent Current	10	Pin1 Highstate		7	12	mA
4 .	V_{CL}	Control Voltage	1	Low State			1.5	V
5 .	V_{CH}	Control Voltage	1	High State	2.3			V
6 .	I_{CL}	Control Input Current	1	V_1 Low State	– 1		0	mA
7 .	I_{CH}	Control Input Current	1	V_1 High State	– 0.6		5	uA
8 .	V_{EL}	Enable Voltage	2/3	Low State			1.5	V
9 .	V_{EH}	Enable Voltage	2/3	High State	2.3			V
10 .	I_{IN}	Input Current	2/3	$V_{2,3}$ Low State	– 10		1	µA
11 .	I_{IN}	Input Current	2/3	$V_{2,3}$ High State	– 1		5	µA
12 .	V_{DL}	Driving Voltage Low	13	R13, 14 = 5 K Low State			0.5	V
13 .	I_D	Driving Current	13	V_{13} = 2 V	6.5	10	16	mA
14 .	V_{SE}	Sense Voltage	9		0		2	V
15 .	V_{ref}	Reference Voltage	6	I_6 = 0. . . 2 mA	1.28	1.33	1.38	V
16 .	I_{ref}	Reference Current	6				2	mA
17 .	V_{RIN}	Reference Input	11		0.3		2	V
18 .	I_{C8}	Charge Current	8	R2 (Pin 5) = 20 K Pin1L	58	65	72	µA
19.	I_{D8}	Discharge Current	8	R1 (Pin 4) = 20 K Pin1H	28	32.5	37	µA
20 .	I_{SD}	Source Current	12	V_{12} = 2 V	0.5	1	1.6	mA
21 .	V_{sats}	Source Saturation Voltage	12	Isource = 0.5 mA			1.2	V
22 .	V_{sats}	Sink Saturation Voltage	12	Isink = 2 mA			0.4	V
23 .	V_{V-I}	VI-Converter Voltage	4 / 5	10 K < R1, 2 < 200 K R1 = R2	1.26	1.32	1.4	V
24 .	t_r	Recirculation Time of Load Current	7	C2 = 1.5 ns R2 = 20 Kohm	27	30	33	µs
25 .	t_D	Current Sense Delay Time	9		0.3	1	2.5	µs

Figure 1 : Timing Diagram Start Phase.



APPLICATION INFORMATION

Figure 2 : Free Running Load Current Leading and Trailing Edge.

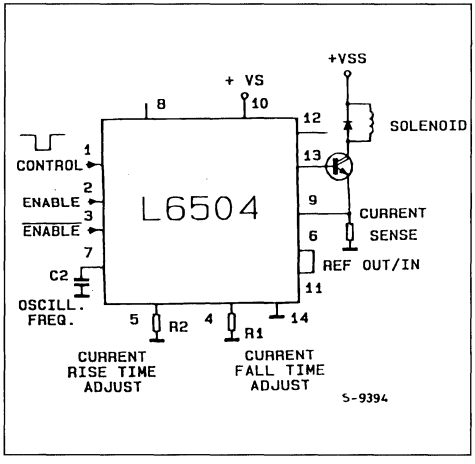


Figure 3.

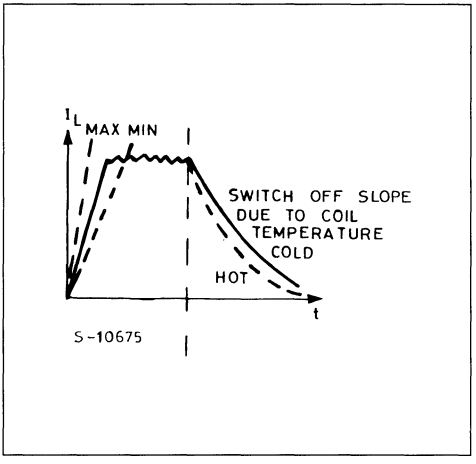


Figure 4 : Slew Rate of Loading Edge Controlled.

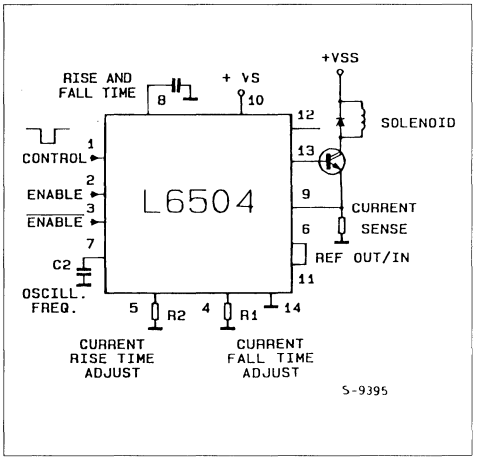


Figure 5.

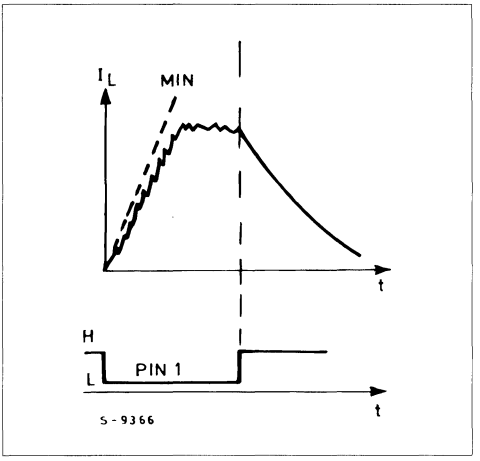


Figure 6 : Slew Rate Leading and Trailing Edge Controlled.

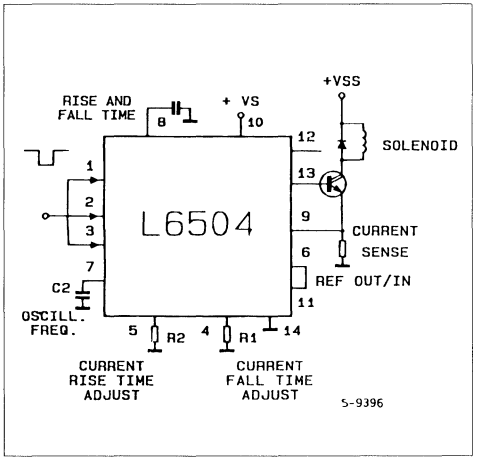


Figure 7.

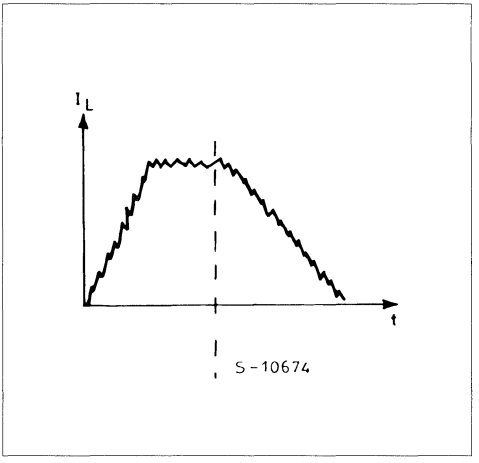


Figure 8 : Free Running Leading Edge Fast Current Slope at Trailing Edge.

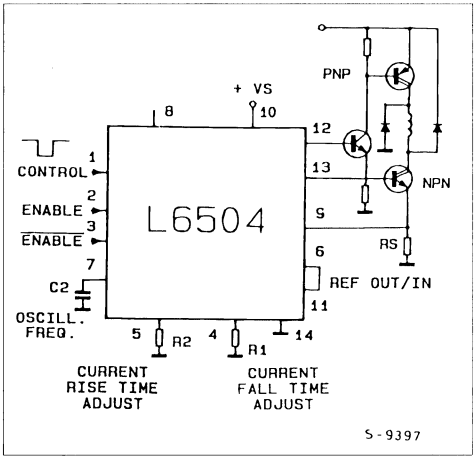
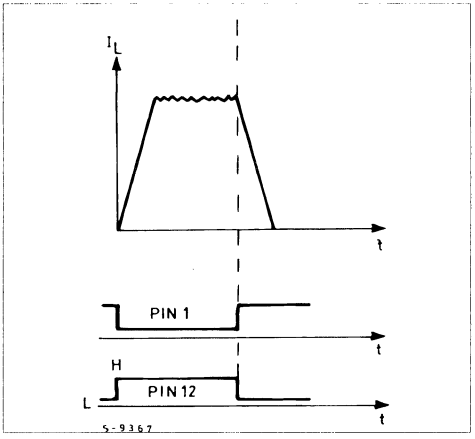


Figure 9.



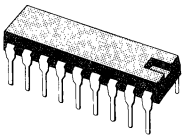
CURRENT CONTROLLER FOR STEPPING MOTORS

PRELIMINARY DATA

DESCRIPTION

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and similar devices. When used in conjunction with the L293, L298, L7150, or L7180, the chip set forms a constant current drive for and inductive load and performs all the interface function from the control logic thru the power stage.

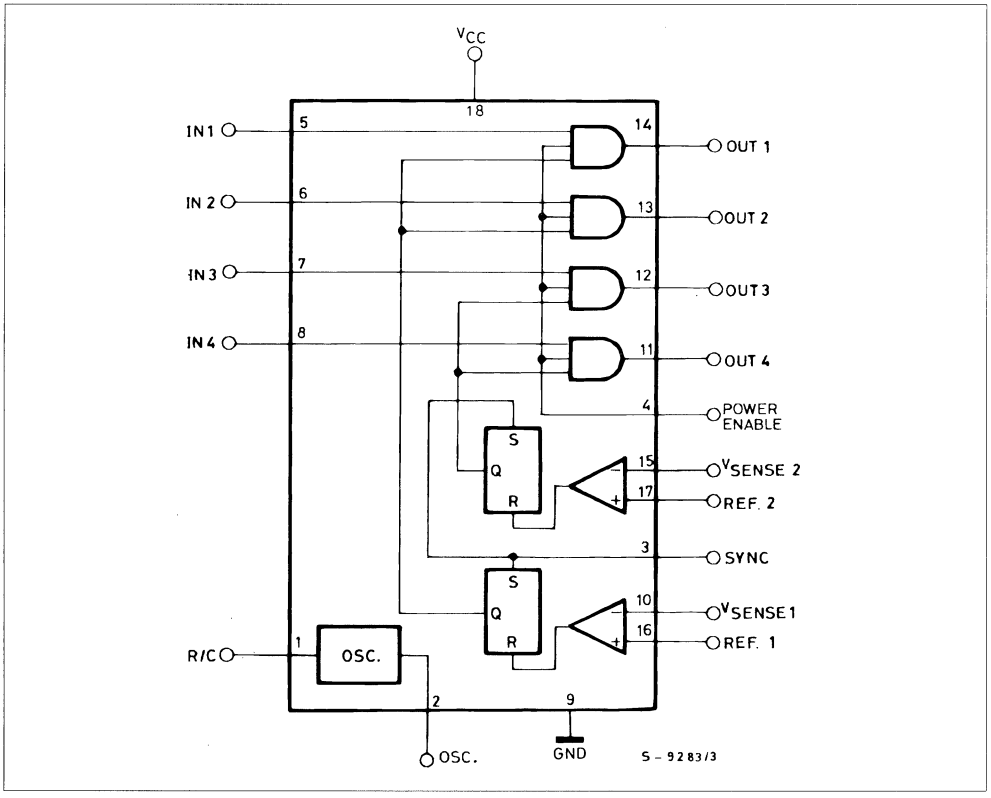
Two or more devices may be synchronized using the sync pin. In this mode of operation the oscillator in the master chip sets the operating frequency in all chips.



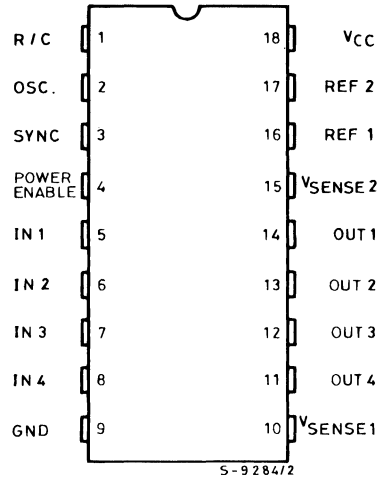
DIP-18 Plastic

ORDER CODE : L6506

BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	10	V
V_I	Input Signals	7	V
P_{tot}	Total Power Dissipation (T_{amb} = 70 °C)	1	W
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_{amb} = 25 °C ; unless otherwise noted)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5		7	V
I_{CC}	Quiescent Supply Current	V_{CC} = 7 V			25	mA

COMPARATOR SECTION

V_{IN}	Input Voltage Range	V_{sense} Inputs	– 0.3		3	V
V_{IO}	Input Offset Voltage	V_{IN} = 1.4 V			± 5.0	mV
I_{IO}	Input Offset Current				± 200	nA
I_{IB}	Input Bias Current				1	µA
	Response Time	V_{REF} = 1.4 V V_{SENS} = 0 to 5 V		0.8	1.5	µs

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
COMPARATOR SECTION PERFORMANCE (over operating temperature range)						
V_{IO}	Input Offset Voltage	V_{IN} = 1.4 V			± 20	mV
I_{IO}	Input Offset Current				± 500	nA
LOGIC SECTION(over operating temperature range) - (TTL compatible inputs & outputs)						
V_{IH}	Input High Voltage		2.0		V_s	V
V_{IL}	Input Low Voltage				0.8	V
V_{OH}	Output High Voltage	V_{CC} = 4.75 V I_{OH} = 400 µA	2	3.5		V
V_{OL}	Ouptut Low Voltage	V_{CC} = 4.75 V I_{OH} = 4.0 mA		0.25	0.4	V
I_{OH}	Ouput Source Current Outputs 1 - 4	V_{CC} = 4.75 V	2.75			mA
OSCILLATOR						
f_{osc}	Frequency Range		5		70	KHz
V_{thL}	Lower Threshold Voltage			0.33 V_{CC}		V
V_{thH}	Higher Threshold Voltage			0.66 V_{CC}		V
R_i	Internal Discharge Resistor		0.7	1	1.3	KΩ

CIRCUIT OPERATION

The L6506 is intended for use with dual bridge drivers, such as the L298, quad darlington arrays, such as the L7180, or discrete power transistors to drive stepper motors and other similar loads. The main function of the device is to sense and control the current in each of the load windings.

A common on-chip oscillator drives the dual chopper and sets the operating frequency for the pulse width modulated drive. The RC network on pin 1 sets the operating frequency which is given by the equation :

$$f = \frac{1}{0.69\ RC} \quad \text{for } R > 10\ K$$

The oscillator provides pulses to set the two flip-flops which in turn cause the outputs to activate the drive. When the current in the load winding reaches the programmed peak value, the voltage across the sense resistor (R_{sense}) is equal to V_{ref} and the corresponding comparator resets its flip-flop interrupting the drive current until the next oscillator pulse occurs. The peak current in each winding is programmed by selecting the value of the sense resistor and V_{ref}. Since separate inputs are provided for each chopper, each of the loads may be programmed independently allowing the device to be used to implement microstepping of the motor. Lower threshold of L6506's oscillator is 1/3 V_{CC}. Upper threshold is 2/3 V_{CC} and internal discharge resistor is 1 KΩ ±30 %.

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground.

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can be found by looking at the figure 1 and are :

$$T2 = 0.69\ C1\ \frac{R1\ R_{IN}}{R1 + R_{IN}} \quad (1)$$

$$T1 = 0.69\ R1\ C1 \quad (2)$$

$$DC = \frac{T2}{T1 + T2} \quad (3)$$

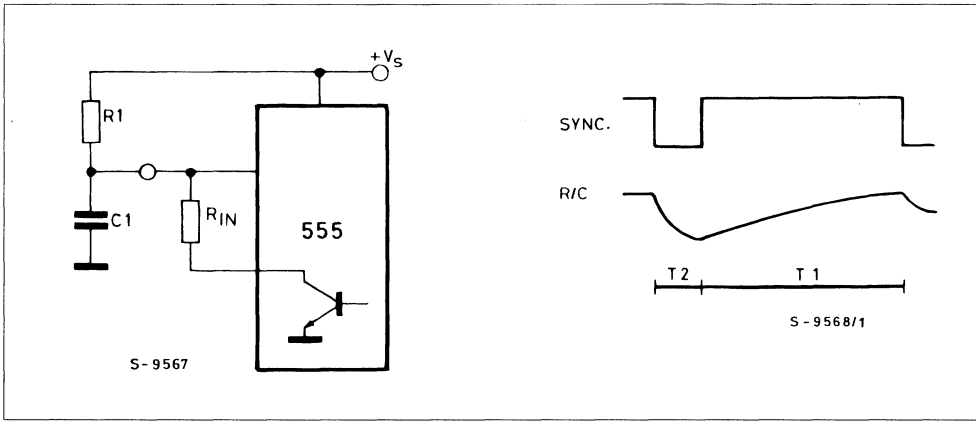
By substituting equations 1 and 2 into equation 3 and solving for the value of R1 the following equations for the external components can be derived :

$$R1 = \left(\frac{1}{DC} - 2\right) R_{IN} \quad (4)$$

$$C1 = \frac{T1}{0.69\ R1} \quad (5)$$

Looking at equation 1 it can easily be seen that the minimum pulse width of T2 will occur when the value of R1 is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 4 the minimum value for R1 of 700Ω (1 KΩ – 30 %) should be used to guarantee the required pulse width.

Figure 1 : Oscillator Circuit and Waveforms.



APPLICATIONS INFORMATION

The circuits shown in figures 2 and 3 use the L6506 to implement constant current drives for stepper motors. Figure 2 shows the L6506 used with the L298 to drive a 2 phase bipolar motor. Figure 3 shows the L6506 used with the L7180 to drive a 4 phase unipolar motor. The peak current can be calculated using the equation :

$$I_{peak} = \frac{V_{ref}}{R_{sense}}$$

The circuit of Fig.2 can be used in applications requiring different peak and hold current values by modifying in the reference voltage.

The L6506 may be used to implement either full step or half step drives. In the case of 2 phase bipolar stepper motor applications, if a half step drive is used, the bridge requires an additional input to disable the power stage during the half step. If used in conjunction with the L298 the enable inputs may be used for this purpose.

For quad darlington array in 4 phase unipolar motor applications half step may be implemented using the 4 phase inputs.

The L6506 may also be used to implement microstepping of either bipolar or unipolar motors.

Figure 2 : Application Circuit Bipolar Stepper Motor Driver.

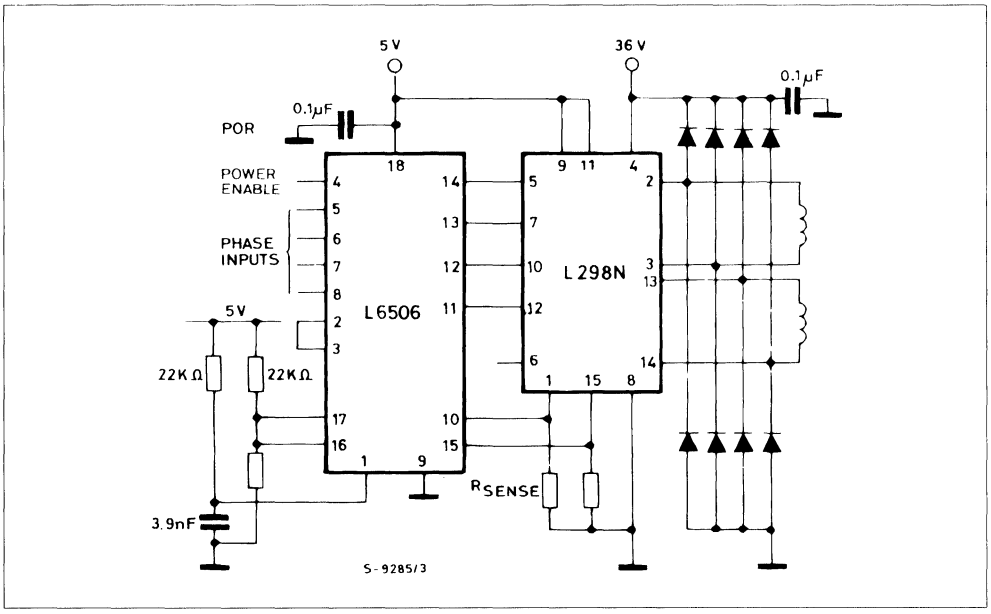
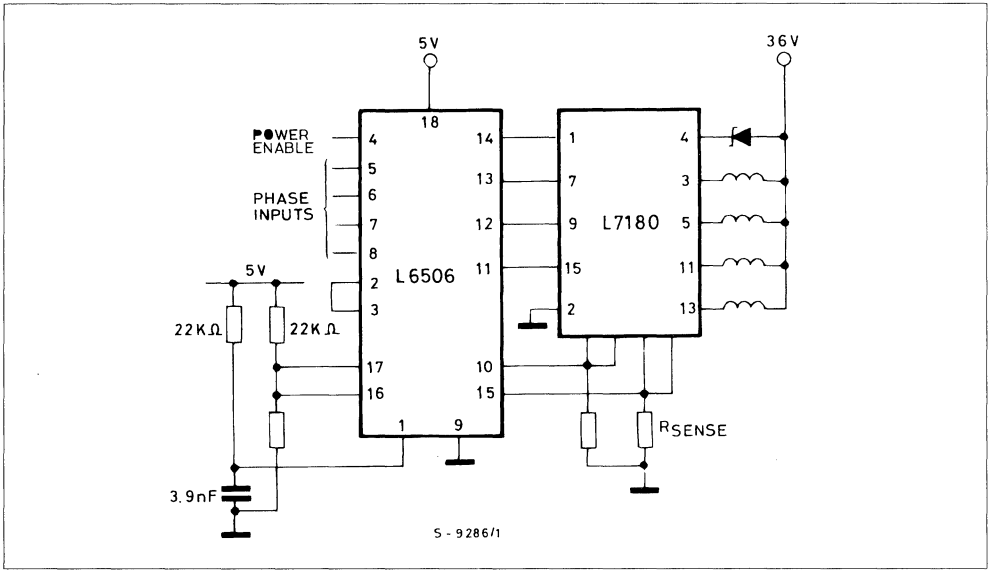


Figure 3 : Application Circuit Unipolar Stepper Motor.

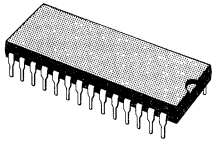


2–CHANNEL FLOPPY DISK READ/ WRITE CIRCUITS

- TWO GAIN VERSIONS (A AND B)
- COMPATIBLE WITH 8", 5.25" AND 3.5" DRIVES.
- INTERNAL WRITE AND ERASE CURRENT SOURCES, EXTERNALLY SET
- INTERNAL CENTER TAP VOLTAGE SOURCE
- CONTROL SIGNALS ARE TTL COMPATIBLE
- TTL SELECTABLE WRITE CURRENT BOOST
- OPERATES ON + 12 V AND + 5 V POWER SUPPLIES

DESCRIPTION

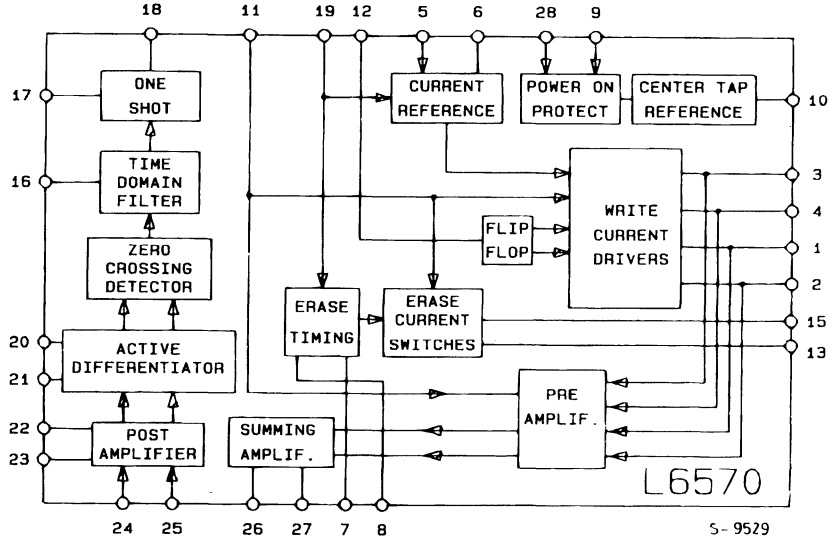
The L6570A/ B are integrated circuits which perform the functions of generating write signals and amplifying and processing read signals required for a double sided floppy disk drive. The L6570A features a gain of 85 min and the L6570B of 300 min. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility.



DIP–28 Plastic

ORDER CODES : L6570A
L6570B

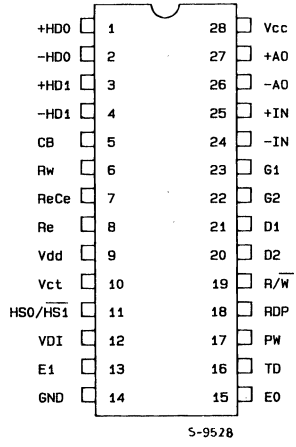
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_{CC}	5V Supply Voltage	7	V
V_{DD}	12V Supply Voltage	14	V
T_{stg}	Storage Temperature	– 65 to 150	°C
T_{amb}	Ambient Operating Temperature	0 to + 70	°C
T_j	Junction Operating Temperature	0 to + 130	°C
V_I	Logic Input Voltage	– 0.5 to 7.0	V
P_{tot}	Power Dissipation	500	mW

CONNECTION DIAGRAM (top view)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (unless otherwise specified, 4.75V ≤ V_{CC} ≤ 5.25V ; 11.4V ≤ V_{DD} ≤ 12,6V ; 0 °C ≤ T_{amb} ≤ 70 °C ; R_W = 430 Ω ; R_{ED} = 62 KΩ ; C_E = 0.012 µF ; R_{EH} = 62 KΩ ; R_{EC} =220Ω)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
POWER SUPPLY CURRENTS						
I_{CC}	5V Supply Current	Read Mode Write Mode			35 38	mA mA
I_{DD}	12V Supply Current	Read Mode **L6570A** **L6570B**			26 35	mA mA
		Write Mode (exclude Write and Erase currents) **L6570A** **L6570B**			24 35	mA mA
LOGIC SIGNALS-READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$), CURRENT BOOST (CB)						
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IL} = 0.4V			– 0.4	mA
V_{IH}	Input High Voltage		2.0			V
I_{IH}	Input High Current	V_{IH} = 2.4V			20	µA
LOGIC SIGNALS-WRITE DATA INPUT (WDI), **HEAD SELECT** (HS0/HS1)						
$V_{T}+$	Threshold Voltage, Positive-going		1.4		1.9	V
$V_{T}-$	Threshold Voltage, Negative-going		0.6		1.1	V
$V_{T}+$, $V_{T}-$	Hysteresis		0.4			V
I_{IH}	Input High Current	V_{IH} = 2.4V			20	µA
I_{IL}	Input Low Current	V_{IL} = 0.4V			– 0.4	mA
CENTER TAP VOLTAGE REFERENCE						
V_{CT}	Output Voltage	I_{WC} + I_E = 3 mA to 60 mA	V_{DD}–1.5		V_{DD}–0.5	V
V_{CC}	Turn-Off Threshold		4.0			V
V_{DD}	Turn-Off Threshold		9.6			V
V_{CT}	Disabled Voltage				1.0	V
ERASE OUTPUTS (E1, E0)						
	Unselected Head Leakage	V_{EO}, V_{E1} = 12.6V			100	µA
V_{E1}, V_{EO}	Output on Voltage	I_E = 50 mA			0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
WRITE CURRENT						
	Unselected Head Leakage	V_{E1}, V_{E0} = 12.6V			25	µA
	Write Current Range	R_W = 820 Ω to180 Ω	3		10	mA
	Current Reference Accuracy	I_{WC} = 2.3/R_W V_{CB} (current boost) = 0.5V	–5		+5	%
	Write Current Unbalanced	I_{WC} = 3 mA to 10 mA			1.0	%
	Differential Head Voltage Swing	$\Delta I_{WC} \leq 5$ %	12.8			V_{pk}
	Current Boost	V_{CB} = 2.4V	1.25 I_{WC}		1.35 I_{WC}	
ERASE TIMING						
	Erase Delay Range	R_{ED} = 39 KΩ to 82 KΩ C_E = 0.0015 µF to 0.043 µF	0.1		1.0	ms
	Erase Delay Accuracy $\frac{\Delta T_{ED}}{T_{ED}}$ x100 %	T_{ED} = 0.69 R_{ED} C_E R_{ED} = 39 KΩ to 82 KΩ C_E = 0.0015 µF to 0.043 µF	– 15		+ 15	%
	Erase Hold Range	R_{EH} + R_{ED} = 78 KΩ to 164 KΩ C_E = 0.0015 µF to 0.043 µF	0.2		2.0	ms
	Erase Hold Accuracy $\frac{\Delta T_{ED}}{T_{ED}}$ x 100 %	T_{EH} = 0.69 (R_{ED} + R_{ED}) C_E R_{EH} + R_{ED} = 78 KΩ to 164 KΩ C_E = 0.0015 µF to 0.043 µF	– 15		+ 15	%

ELECTRICAL CHARACTERISTICS (Unless otherwise specified : V_{IN} (Preamplifier) =10mV_{pp} sine wave, DC coupled to center tap. Summing amplifier load = 2 KΩ line-line, AC coupled. V_{IN} (Postamplifier)= 0.2 V_{pp} sine wave, AC coupled ; R_G = open ; Data pulse load = 1 KΩ to V_{CC} ; C_D = 240 pF ; C_{TD} = 100 pF ; R_{TD} = 7.5 KΩ ; C_{PW} = 47 pF ; R_{PW} = 7.5 KΩ).

READ MODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PREAMPLIFIER-SUMMING AMPLIFIER						
	Diff Voltage Gain	Freq. = 250 KHz **L6570A** **L6570B**	85 300		115 400	V/V
	Bandwidth (– 3 dB)		3			MHz
	Gain Flatness	Freq. = DC to 1.5 MHz			± 1.0	dB
	Diff. Input Impedance	Freq. = 250 KHz	20			KΩ
	Max. Diff. Output Voltage Swing	V_{IN} = 250 KHz Sine Wave THD ≤ 5 % **L6570A** **L6570B**	2.5 4.0			V_{pp}
	Small Signal Difference Output Resistance	$I_O \leq 1.0$ mA $_{pp}$			75	Ω
	Common Mode Rejection Ratio	V_{IN} = 300 mV_{pp} @ 500 KHz Inputs Shorted **L6570A** **L6570B**	50 40			dB

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PREAMPLIFIER-SUMMING AMPLIFIER						
	Power Supply Rejection Ratio	ΔV_{DD} = 300 mV_{pp} @ 500 KHz Inputs Shorted to V_{CT}	50			dB
	Channel Isolation	Unselected Channel V_{IN} =100 mV_{pp} @ 500 KHz. Selected Channel Input Connected to V_{CT}	40			dB
	Equivalent Input Noise	Power BW = 10 kHz to 1 MHz Inputs Shorted to V_{CT}			10	μV_{rms}
V_{CT}	Center Tap Voltage			1.5		V
POSTAMPLIFIER-ACTIVE DIFFERENTIATOR						
	AO, Diff. Voltage Gain + IN, - IN to D1, D2	Freq. = 250 KHz	8.5		11.5	V/V
	Bandwidth (– 3dB) + IN, - IN to D1, D2	C_D = 0.1 µF, R_D = 2.5 KΩ	3			MHz
	Gain Flatness + IN, - IN to D1, D2	Freq. = DC to 1.5 MHz C_D = 0.1 µF, R_D = 2.5 KΩ			± 1.0	dB
	Max. Diff. Output Voltage Swing	V_{IN} = 250 KHz Sine Wave, AC Coupled. ≤ 5 % THD in Voltage across C_D	5.0			V_{pp}
	Max. Diff. Input Voltage	V_{IN} = 250 KHz Sine Wave, AC Coupled. ≤ 5 % THD in Voltage across C_D, R_G = 1.5 KΩ	2.5			V_{pp}
	Diff. Input Impedance		10			KΩ
	Gain Control Accuracy $\frac{\Delta A_R}{A_R}$ x 100 %	$A_R = A_O R_G/(8 \times 10^3 + R_G)$ R_G = 2 KΩ	– 25		+ 25	%
	Threshold Differential Input Voltage	Min. diff. input voltage at post amp. that results in a change of state at RDP V_{IN} = 250 KHz square wave, C_D = 0.1 µF R_D = 500 Ω, T_R, T_F ≤ 0.2 µs. No overshoot ; Data pulse from each V_{IN} transition			3.7	mV_{pp}
	Peak Differential Network Current		1.0			mA

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TIME DOMAIN FILTER						
	Delay Accuracy $\frac{\Delta T_{TD}}{T_{TD}}$ x 100 %	$T_{TD} = 0.58\ R_{TD} \cdot (C_{TD} + 10^{-11}) +$ 150 ns. R_{TD} = 5 KΩ to 10 KΩ C_{TD} = 56 pF V_{IN} = 50 mV_{pp}@ 250 KHz sq. wave T_R, $T_F \leq$ 20 ns, AC coupled. Delay measured from 50 % input amplitude to 1.5 V data pulse	– 15		+ 15	%
	Delay Range	$T_{TD} = 0.58\ R_{TD} = (C_{TC} + 10^{-11}) +$ 150 ns. R_{TD} = 5 KΩ to 10 KΩ C_{TD} = 56 pF to 240 pF R_D = 500 Ω C_D = 0.1 µF.	240		2370	ns
DATA PULSE						
	Width Accuracy $\frac{\Delta T_{PW}}{T_{PW}}$ x 100 %	$T_{PW} = 0.58\ R_{PW}$ x (C_{PW} + 8 x 10^{-12}) + 20 ns R_{PW} = 5 KΩ to 10 KΩ $C_{PW} \geq$ 36 pF with measured at 1.5V amplitudes	– 20		+ 20	%
	Active Level Output Voltage	I_{OH} = 400 µA	2.7			V
	Inactive Level Output Leakage	I_{OL} = 4 mA			0.5	V
	Pulse Width	$T_{PW} = 0.58\ R_{PW}$ x (C_{PW} + 8 x 10^{-12}) + 20 ns R_{PW} = 5 KΩ to 10 KΩ C_{PW} = 36 pF to 200 pF	145		1225	ns

TEST SCHEMATICS

Figure 1 : Preamplifier Characteristics.

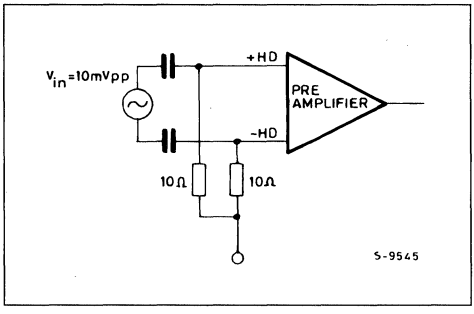
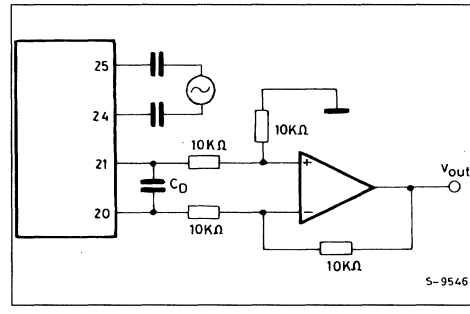


Figure 2 : Postamplifier Differential Output Voltage Swing and Voltage Gain.



TEST SCHEMATICS (Continued)

Figure 3 : Postamplifier Threshold Differential Input Voltage.

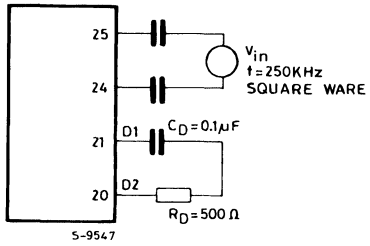
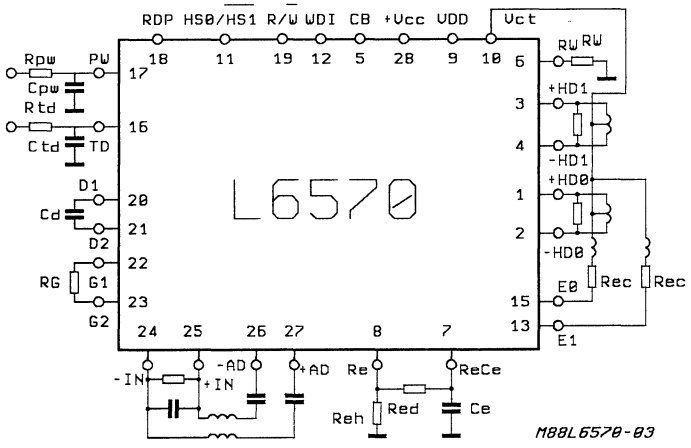


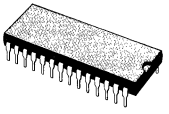
Figure 4 : Complete Test Circuit.



MEMORY CARD INTERFACE

ADVANCE DATA

- Single Power Supply operation
- Internal Clock Generator or External Clock Input
- Adjustable Precision of PVS Output Voltage (2 %)
- 100 mV/step of the Writing Output Voltage
- I/O, Reset and Clock Outputs Protection Against Short Circuit to GND and to V_{pvs}.



DIP 28

ORDER CODE : L6603

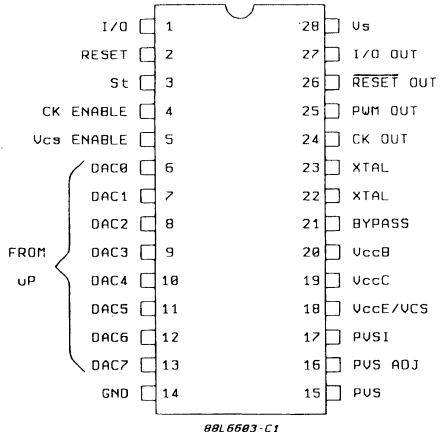
PLCC 28

ORDER CODE : L6604

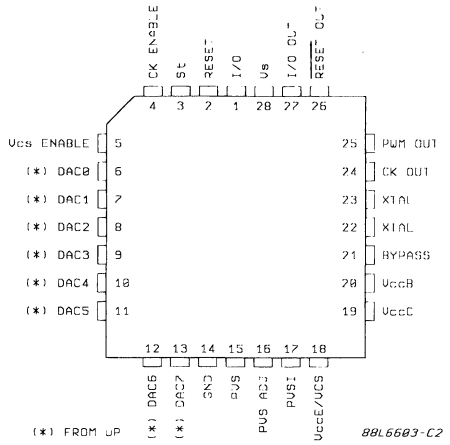
DESCRIPTION

The L6603 and L6604 are integrated circuits for application as interface between different types of memory card and a microprocessor which excanges data with cards. Its operate with a single power supply.

CONNECTION DIAGRAMS

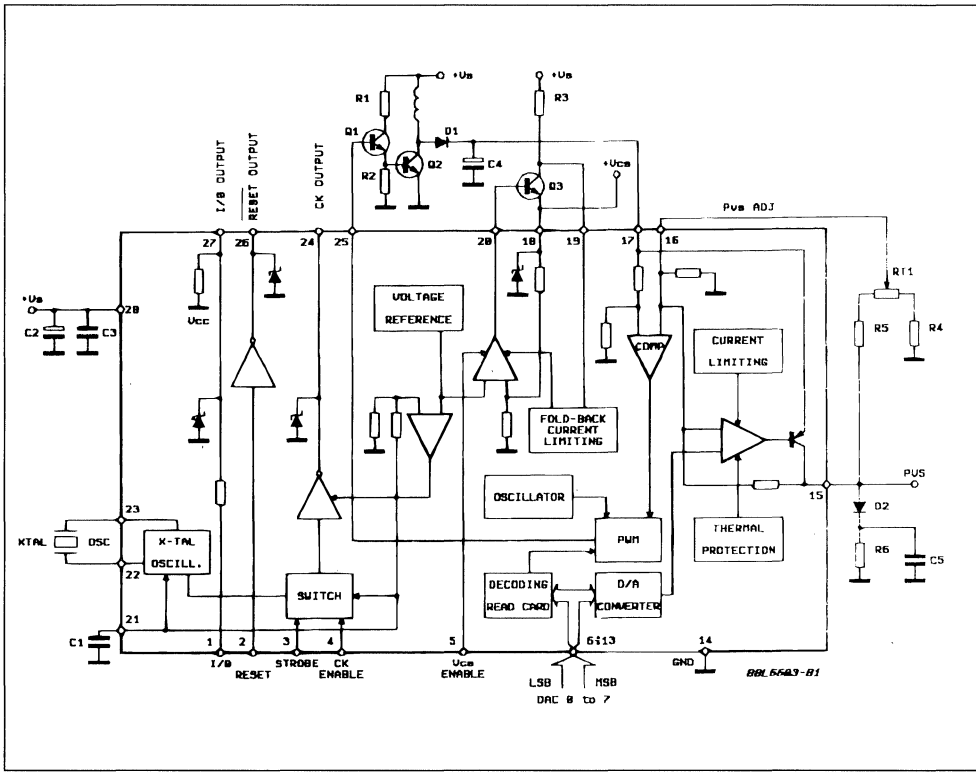


DIP 28



PLCC 28

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_S	Supply Voltage	10	V
T_{op}	Operating Temperature Range	– 20 to 70	°C
T_{stg}	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA (*)

			DIP 28	PLCC 28	
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	100	°C/W

(*) With all the pins soldered to printed circuit with minimized copper area.

PIN FUNCTIONS

Pin	Name	Function
1	I/O	Input of the Bidirectional Data Line
2	RESET	Control Input for Reset of Memory Card FA Function
3	St	Strobe for Card with Memory (TTL compatible)
4	CK ENABLE	Commutation for µP Cards CK ENABLE = 1 (internal clock)
5	VCS ENABLE	Control Input for VCS Supply Voltage
6 to 13	DACO to DAC7	Control Inputs for Programmation of V_{PVS} Supply (see operation of programming supply V_{PVS})
14	GND	Ground
15	V_{PVS}	Programmable Supply for Memory Card (no use with decoupling capacitor) Note 7 (to the credit card)
16	V_{PVS} Adj	Adjustment Input for 2 % Precision V_{PVS} Output
17	PVS I	Input for V_{PVS} Regulator
18 19 20	V_{CS} V_{CC} E C B	Inputs for Connection of Power Transistor (V_{CC} regulator) (decoupling capacitor on pin 18 > 100 nF if necessary) Note 8 (pin 18 to the credit card)
21	BYPASS	Output Voltage of Regulator for Clock Circuits (decoupling capacitor > 150 nF). Note 9
22 23	XTAL XTAL	Inputs for X-tal Connection. Note 10
24	CK OUT	Output for Clock Signal (TTL levels). Note 11 (to the credit card)
25	PWM OUT	Output for DC/DC Converter
26	$\overline{\text{RESET}}$/OUT	Reset Output. Note 11 (to the credit card)
27	I/O Out	Output I/O. Note 11 (to the credit card)
28	V_S	General Power Supply

Note 1 For inputs V_{vss} enable, Reset, I/0, St, CK enable DAC (0 - 7).
Note 2 For inputs DAC (0 - 7)
Note 3 For input CK enable
Note 4 For input Reset
Note 5 For input V_{vcs} enable
Note 6 For input I/0
Note 7 Typical internal thermal protection & current limiting system
Note 8 Current limiting with "fold back system"

$$I_{lim}\ max\ (A) = \frac{0.75\ V}{Rlim}$$

Note 9 Internal current limiting system
Note 10 Input for external clock (fig. 3)
Note 11 Output protected against short-circuit to ground and to & V_{pvs}

ELECTRICAL CHARACTERISTICS (V_S = 8.5 V ; T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Note
V_{IH}	Input High Voltage		2			V	1
V_{IL}	Input Low Voltage				0.8	V	1
I_{IH}	Input High Current				250	µA	2
					500	µA	3
					100	µA	4
					400	µA	5
					– 200	µA	6
I_{IL}	Input Low Current				– 150	µA	2
					– 300	µA	3
					+ 10	µA	4
					– 200	µA	5
					– 300	µA	6
I_{SW}	Supply Current Writing Mode (pin 28)	$V_{PVS} = V_{PVSW}$ max	tbd			mA	
I_{SR}	Supply Current Reading Mode (pin 28)	$V_{PVS} = V_{PVSR}$	tbd			mA	
V_{CS}	Output Voltage Range	V_S = 7 to 10 V ; I_{CS} = 0 to – 200 mA ; T_{amb} = – 20 to 70 °C ;	4.8	5	5.2	V	
$\frac{\Delta V_{CS}}{\Delta V_{CS}}$	Load Regulation	I_{CS} = 0 to – 200 mA		0.18		%	
$\frac{\Delta V_{CS}}{\Delta V_S}$	Line Regulation	V_S = 7 to 10 V ;		– 50		dB	
$\frac{\Delta V_{CS}}{\Delta T}$	Temperature Coeff. of Output Voltage V_{CS}	T_{amb} = – 20 to 70 °C		65		dB	
t_{off1}	Fall Time of V_{CS}	Fig. 1 CL = 30 pF		5	25	µs	
t_{off2}	Fall Time of V_{PVS}	Fig. 1 CL = 30 pF ; ΔV_{PVS} = 0.1 V		40	100	µs	
$I_{CS\ max}$	Operating Curr. Limit	V_{CS} = – 4 % ; R_{lim} = 3 ohm	– 220			mA	
I_{CS1}	Short Circuit Current limit			– 70	– 100	mA	
$V_{PVSWMAX}$	Maximum Programming Voltage (writing mode memory)	V_S = 7 to 10 V ; I_{PVS} = 0 to – 50 mA ;	24.5	25.5	26.5	V	
$V_{PVSWMIN}$	Minimum Programming Voltage (writing mode memory)	V_S = 7 to 10 V ; I_{PVS} = 0 to – 50 mA ;	4.9	5.1	5.3	V	
V_{PVSR}	Output Voltage Range of PVSP (reading mode memory)	V_S = 7 to 10 V ; I_{PVS} = 0 to – 20 mA ;	4.8	5	5.2	V	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Note
$\frac{\Delta V_{PVS}}{V_{PVS}}$	Load Regulation	I_{PVS} = 0 to – 50 mA ;		0.8		%	
$\frac{\Delta V_S}{\Delta V_{PVS}}$	Line Regulation	I_{VPS} = 0 mA ; V_S = 7 to 10 V		50		dB	
$\frac{\Delta V_{PVS}}{\Delta_T}$	Temperature coeff. of Ouptut Voltage V_{PVS}	I_{PVS} = 0 mA ; T_{amb} = – 20 to 70 °C		74		dB	
I_{PVSMAX}	Short Circuit Current Limit		– 50	– 65	– 80	mA	
V_{PVS} ADJ – V_{CS}	Differential Volt. between V_{PVS} (reading mode) & V_{CS}		– 5		5	%	
t_{pLH1}	Turn ON Time of V_{CS}	Fig. 1 CL = 30 pF ;		12	50	µs	
t_{pLH2}	Turn ON Time of V_{PVS}	Fig. 1 CL = 30 pF ; ΔV_{PVS} = 0.1 V		25	100	µs	
t_{on1}	Rise Time of V_{CS}	Fig. 1 CL = 30 pF ;		10	50	µs	
t_{on2}	Rise Time of V_{PVS}	Fig. 1 CL = 30 pF; ΔV_{PVS} = 0.1 V		30	100	µs	

ELECTRICAL CHARACTERISTICS (V_S = 8.5 V ; T_{amb} = 25 °C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Note
V_{OH1}	High Output Voltage (pin 26)	(PIN 26) V_{CS} min I_{OH} = – 200/µA	4.2	4.8		V	
V_{OL1}	Low Output Voltage (pin 26)	(PIN 26) V_{IH} = 2 V ; I_{OL} = + 200/µA		0.15	0.4	V	
V_{SC1}	Max Output Voltage during Short-circuit between V_{PVS} and Pin 26				V_{CS} + 0.3	V	
I_{SC2}	Short-circuit Curr. Limit (pin 26)				– 0.5	mA	
V_{OH2}	High Output Voltage (pin 27)	V_{CS} min ; I_{OH} = – 500/µA V_{IH} max = 2 V	1.9			V	
V_{OL2}	Low Output Voltage (pin 27)	V_{CS} max ; I_{OL} = + 200/µA V_{IH} min = 0.8 V			0.9	V	
V_{SC2}	Max Output Voltage during Short-circuit between V_{PVS} and Pin 27				V_{CS} + 0.3	V	
I_{SC3}	Short-circuit Curr. Limit (pin 27)	I/O = 4.2 V			– 30	mA	
V_{OH3}	High Output Voltage (pin 24)	I_{OH} = – 200/µA	3.5	4.1		V	
V_{OH4}	High Output Voltage (pin 24)	I_{OH} = – 10/µA	4.1	4.2		V	
V_{OL3}	Low Output Voltage (pin 24)	I_{OL} = + 200/µA		0.1	0.4	V	
V_{SC3}	Max Output Voltage during Short-circuit between Pin 24 & V_{PVS} Output				V_{CS} + 0.3	V	
I_{SC4}	Short-Circuit Curr. Limit (pin 24)				– 35	mA	
t_{on}	Rise Time of Clock Output (pin 24)	Fig. 2 f_{XTAL} = 4.91 MHz ; CL = 30 pF		15		ns	
t_{off}	Fall Time of Clock Output (pin 24)	Fig. 2 f_{XTAL} = 4.91 MHz ; CL = 30 pF		18		ns	
	Duty Cycle (T1/T)	f_{XTAL} = 4.91 MHz ; CL = 30 pF	40		60	%	

OPERATION OF PROGRAMMING SUPPLY V_{PVS}

The output voltage V_{pvs} can be programmed from 5 V to 25.5 V by steps of 0.1 V and can be expressed as follows :

$$V_{pvs} = \frac{\text{code DAC 0-7}}{10}$$

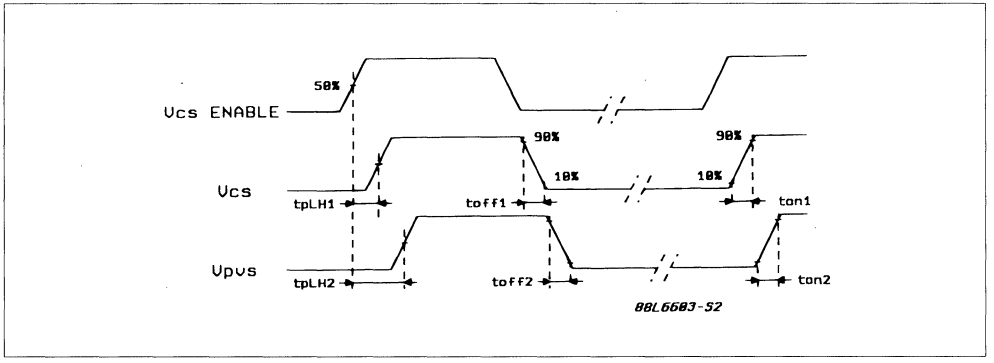
Two operating modes are possible

Reading mode (code DAC = 50) : V_{pvs} = 5 V ;

Writing mode (code 51 to 255) : V_{pvs} = 5.1 to 25.5 V

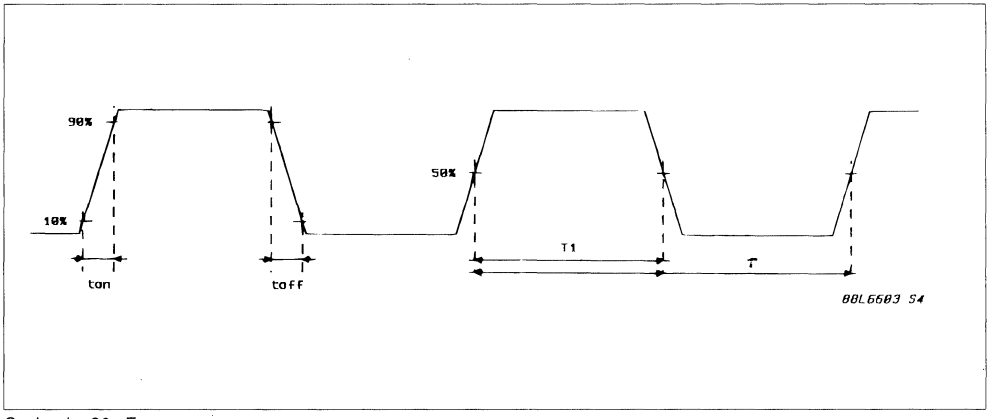
In this case, the voltage drop between output of converter DC/DC (PVSI) and V_{pvs} is constant and is tipically to 3 V.

Figure 1 : V_{CS} and V_{PVS} Delay Times Versus V_{CS} Enable.



C_{tot} load = 30 pF.

Figure 2 : Clock Output Waveform.



C_{tot} load = 30 pF.

Figure 3 : Input for External Clock.

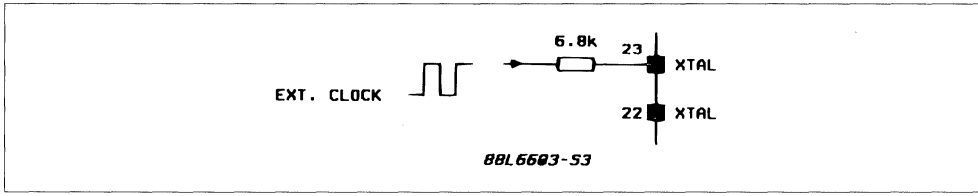
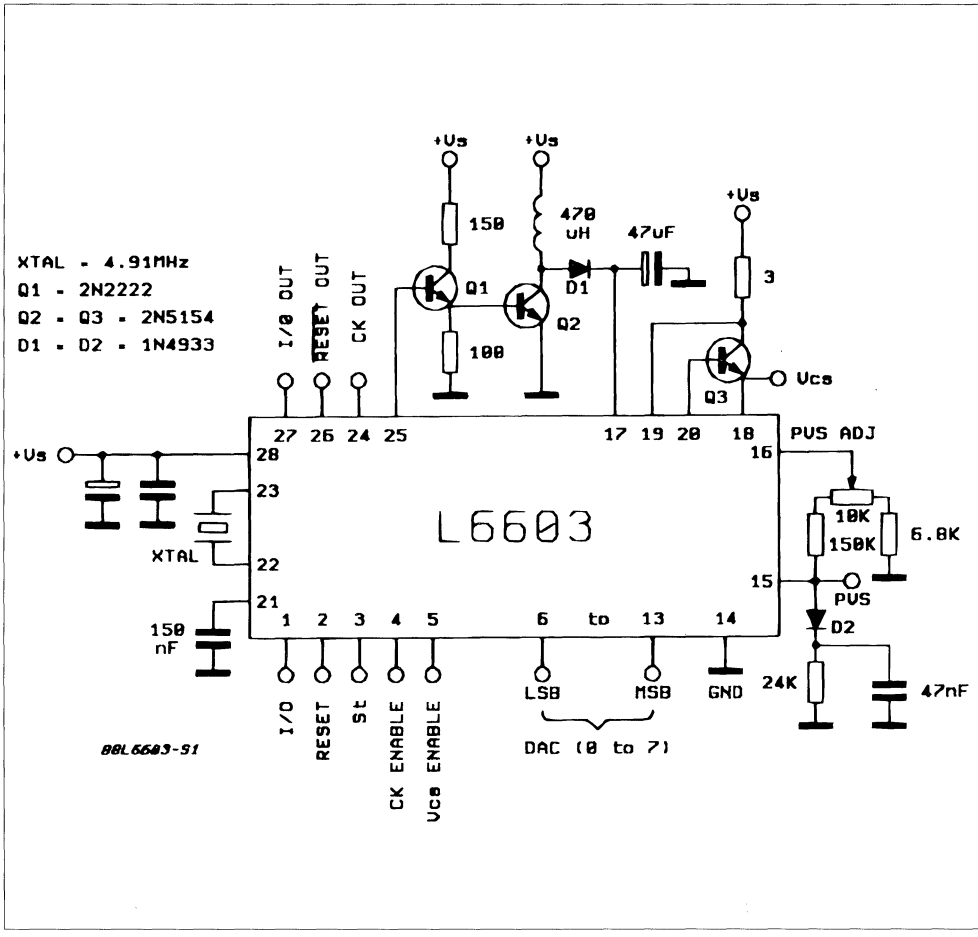


Figure 4 : Application Circuit.



SGS-THOMSON MICROELECTRONICS

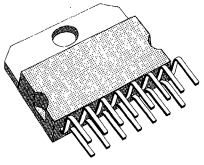
L7150
L7152

50 V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5 A, 50 V, 100 % DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5 V AND 6-15 V LOGIC FAMILIES

The L7150 has 350 input resistors and is compatible with TTL, DTL, LSTTL and 5 V CMOS logic. The L7152 has 3 KΩ input resistors for use with 6-15 V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



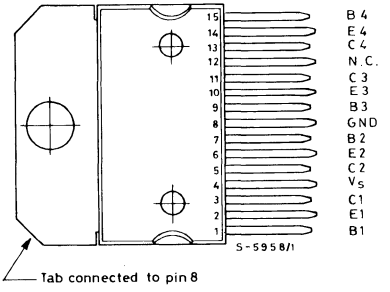
Multiwatt-15

ORDER CODES : L7150
L7152

DESCRIPTION

The L7150 and L7152 are 1.5 A quad darlington arrays mounted in the 15-lead Myltiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads and all three terminals are isolated.

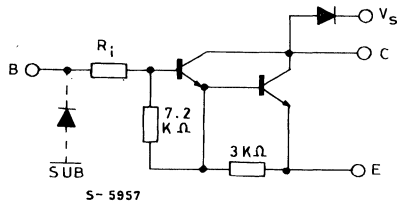
CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	50	V
I_o	Output Current	1.75	A
V_I	Input Voltage	30	V
I_B	Input Current	25	mA
P_{tot}	Power Dissipation (T_{case} = 75 °C)	25	W
T_{amb}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



L7150 : R_{IN} = 350Ω
L7152 : R_{IN} = 3KΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V T_{amb} = 70°C V_{CE} = 50 V			100 500	µA µA	1
$V_{CER\ (sus)}$	Collector-emitter Sustaining Voltage*	I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE\ (sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA I_C = 750 mA I_B = 935 µA I_C = 1 A I_B = 1.25 mA I_C = 1.25 A I_B = 2 mA			**1.15** **1.3** **1.4** **1.5**	V V V V	3
$I_{i(on)}$	Input Current	for **L7150** V_i = 2.4 V for **L7150** V_i = 3.75 V for **L7152** V_i = 5 V for **L7152** V_i = 12 V	**1.4** **3.3** **0.6** **0.7**		4.3 9.6 1.8 5.2	mA mA mA mA	4
$V_{i(on)}$	Input Voltage	for **L7150** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A for **L7152** V_{CE} = 2 V I_C = 1 A V_{CE} = 2 V I_C = 1.5 A			 2 2.5 6.5 10	 V V V V	5
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

(*) $t_{(sus)}$ = 10 µs.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

TEST CIRCUIT

Figure 1.

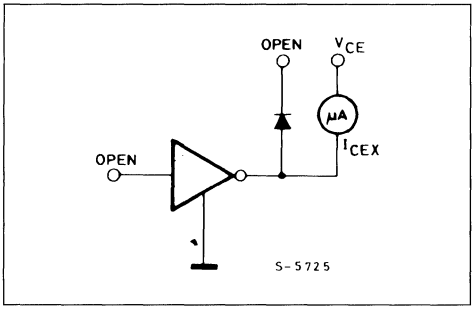


Figure 2.

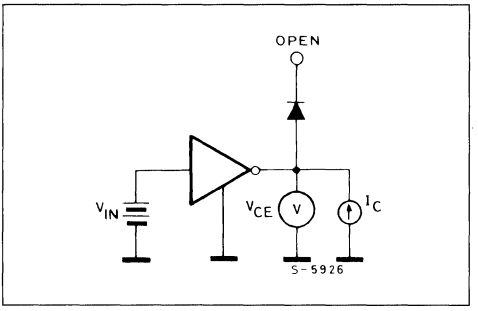


Figure 3.

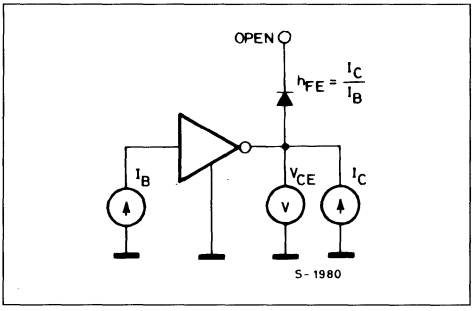


Figure 4.

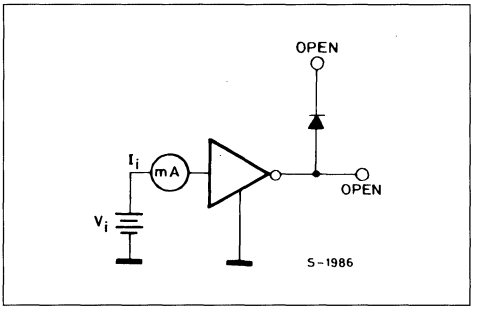
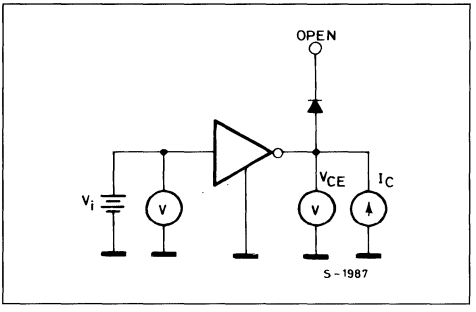


Figure 5.

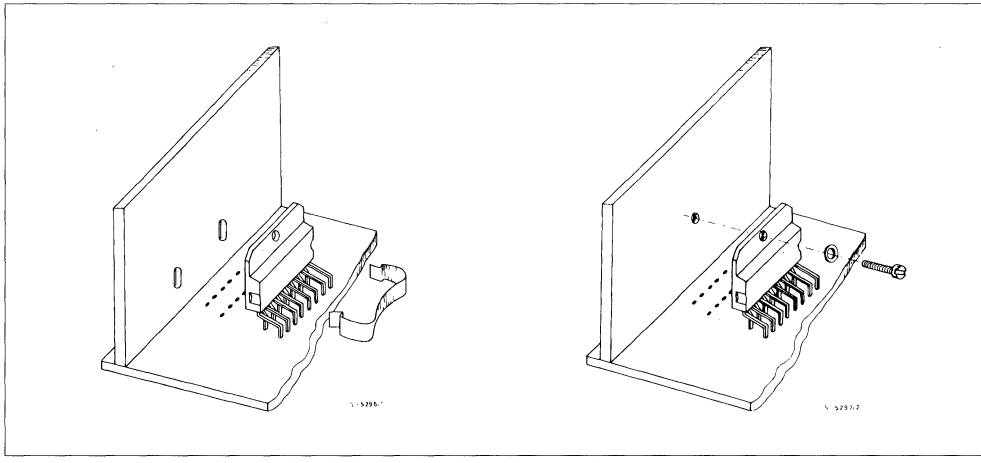


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 6 : Mounting Example.

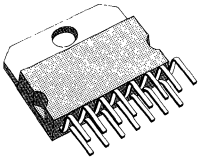


80 V QUAD DARLINGTON SWITCHES

- FOUR NPN DARLINGTONS WITH ISOLATED CONNECTIONS
- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- MULTIWATT PACKAGE ALLOWS OPERATION AT 1.5 A, 80 V, 100 % DUTY CYCLE, ALL FOUR DEVICES ON
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR 5 V AND 6-15 V LOGIC FAMILIES

The L7180 has 350 Ω input resistors and is compatible with TTL, DTL, LSTTL and 5 V CMOS logic. The L7182 has 3 KΩ input resistors for use with 6-15 V CMOS and PMOS logic.

These devices are suitable for driving a wide range of inductive and non-inductive loads including DC motors, stepper motors, solenoids, relays, lamps, multiplexed LEDs and heaters.



Multiwatt 15

ORDER CODES : L7180
L7182

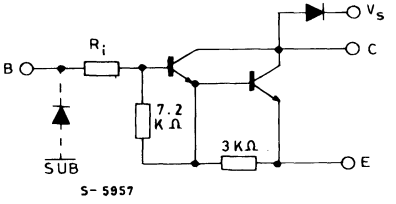
DESCRIPTION

The L7180 and L7182 are 1.5 A quad darlington arrays mounted in the 15-lead Multiwatt® plastic package. Each darlington is equipped with a suppression diode for inductive loads, and all three terminals are isolated.

ABSOLUTE MAXIMUM RATINGS

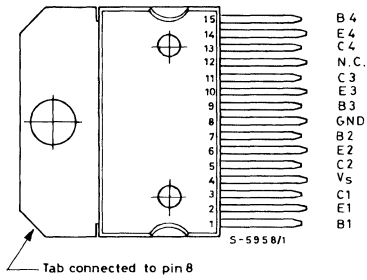
Symbol	Parameter	Test Conditions	Unit
V_{CEX}	Output Voltage	80	V
I_o	Output Current	1.75	A
V_i	Input Voltage	60	V
I_B	Input Current	25	mA
P_{tot}	Power Dissipation (T_{case} = 75 °C)	25	W
T_{amb}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

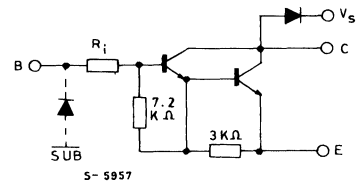
SCHEMATIC DIAGRAM



L7180 : R_{IN} = 350 Ω
L7182 : R_{IN} = 3 KΩ

CONNECTION AND SCHEMATIC DIAGRAMS (top view)





L7180 : R_{IN} = 350 Ω
L7182 : R_{IN} = 3 KΩ

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	35	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 80 V				100	µA	1
		V_{CE} = 80 V	T_{amb} = 70 °C			500	µA	
$V_{CER(sus)}$	Collector-emitter Sustaining Voltage(*)	I_C = 50 mA	V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA	I_B = 625 µA			**1.15**	V	3
		I_C = 750 mA	I_B = 935 µA			**1.3**	V	
		I_C = 1 A	I_B = 1.25 mA			**1.4**	V	
		I_C = 1.5 A	I_B = 2.25 mA			**1.6**	V	
$I_{i(on)}$	Input Current	For **L7180**	V_i = 2.4 V	**1.4**		4.3	mA	4
		For **L7180**	V_i = 3.75 V	**3.3**		9.6	mA	
		For **L7182**	V_i = 5 V	**0.6**		1.8	mA	
		For **L7182**	V_i = 12 V	**1.7**		5.2	mA	
$V_{i(on)}$	Input Voltage	For **L7180**						5
		V_{CE} = 2 V	I_C = 1 A			2	V	
		V_{CE} = 2 V	I_C = 1.5 A			2.5	V	
		For **L7182**						
		V_{CE} = 2 V	I_C = 1 A			6.5	V	
		V_{CE} = 2 V	I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o				1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o				1.5	µs	

(*) $t_{(sus)}$ = 10 µs.
Guaranteed by design ; not tested 100 %.

TEST CIRCUITS

Figure 1.

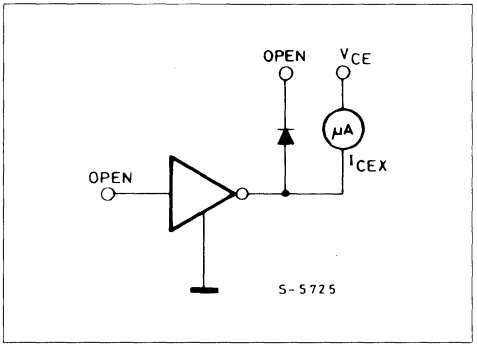


Figure 2.

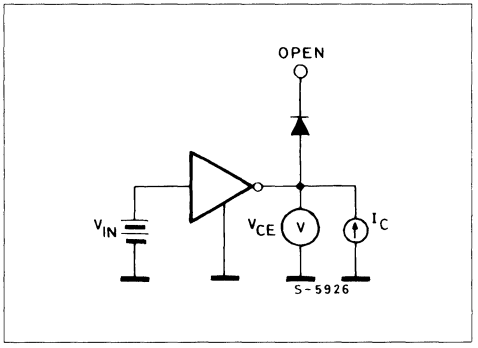


Figure 3.

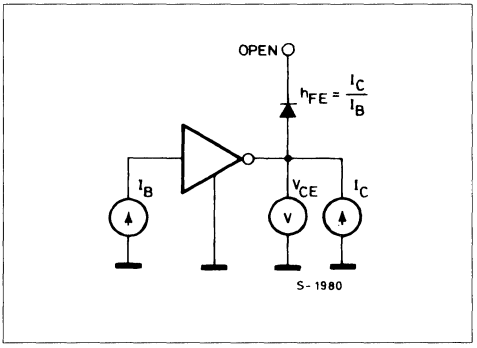


Figure 4.

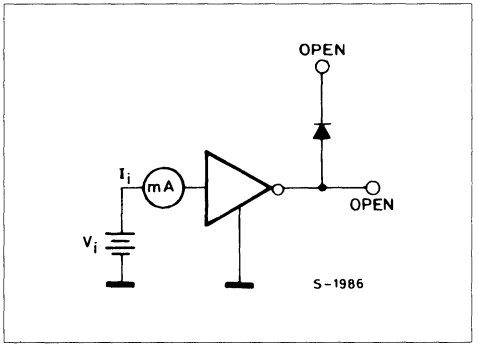
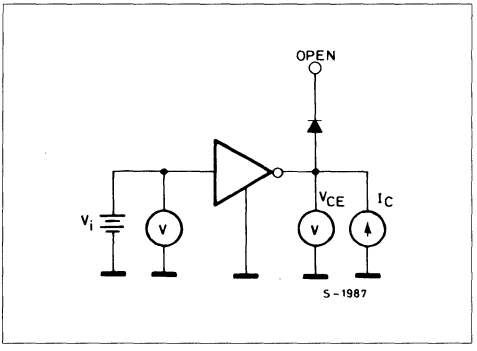


Figure 5.

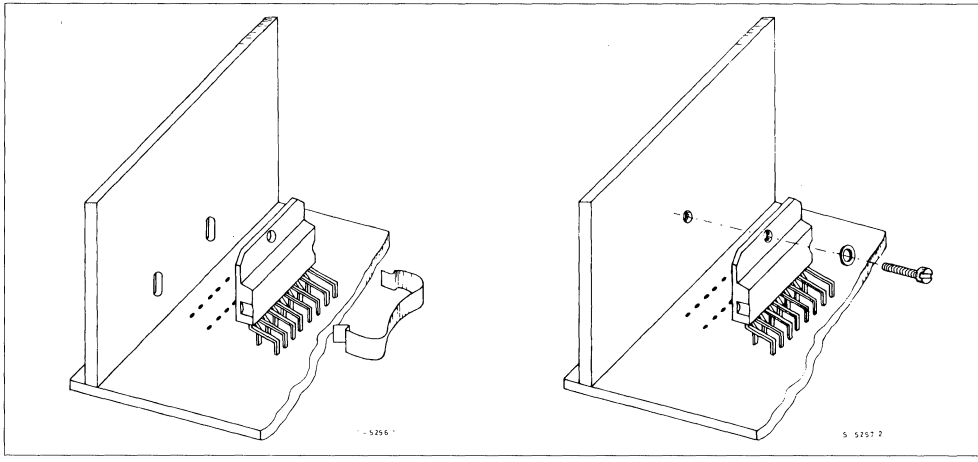


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 6 : Mounting Example.



SGS-THOMSON MICROELECTRONICS

M5450
M5451

LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

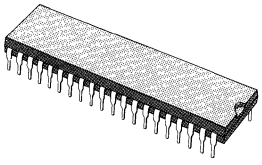
Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

The M5450 and M5451 are pin-to-pin replacements of the NS MM 5450 and MM 5451.



DIP-40 Plastic

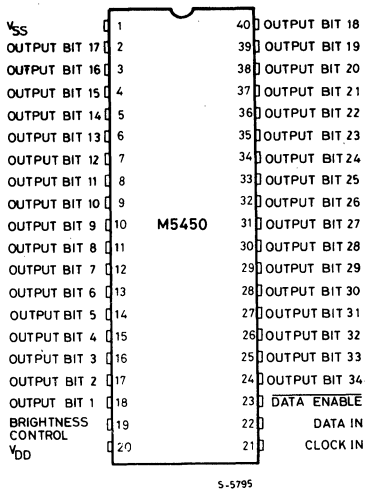
ORDERING NUMBERS: M5450 B7
M5451 B7

ABSOLUTE MAXIMUM RATINGS

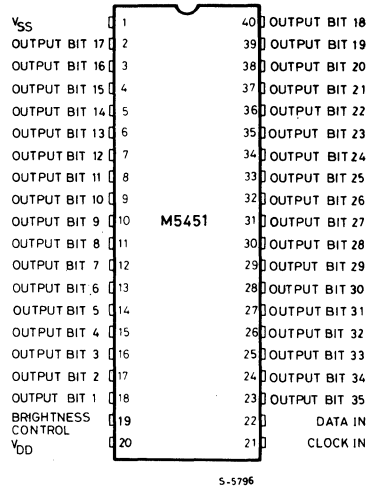
V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1W
		at 85°C	560 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAMS



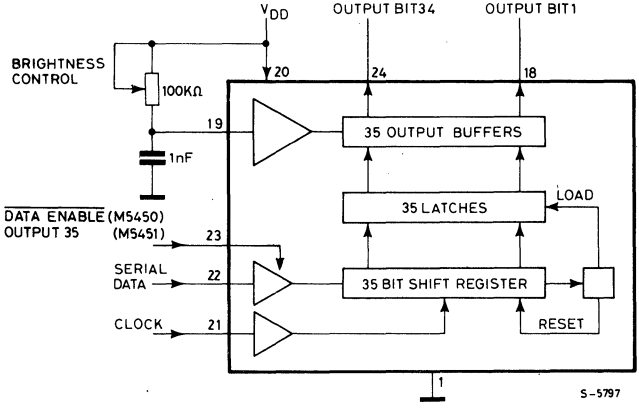
S-5795



S-5796

BLOCK DIAGRAM

Fig. 1



S-5797

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
VI	Input Voltage Logical "0" Level Logical "1" Level	± 10 µA input bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.
A block diagram is shown in figure 1. For the M5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the M5450.

FUNCTIONAL DESCRIPTION (continued)

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.
Figure 3 shows the timing relationship between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + (V_{DD} \cdot 7\ \text{mA})\ ]\ (124\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
124°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

Fig. 2 - Input Data Format

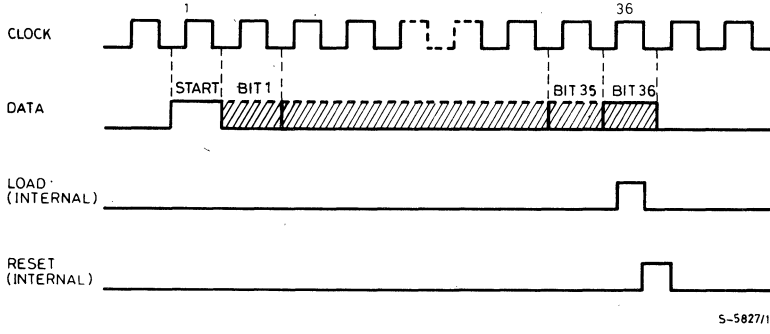


Fig. 3

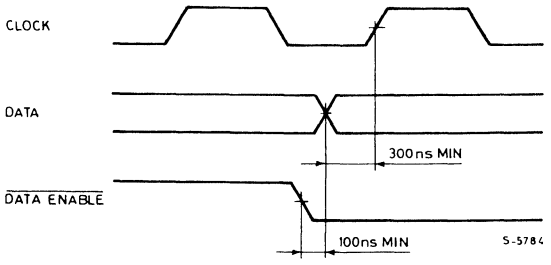


Fig. 4

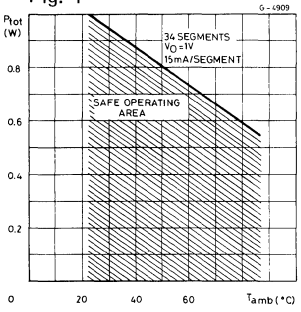


Fig. 5

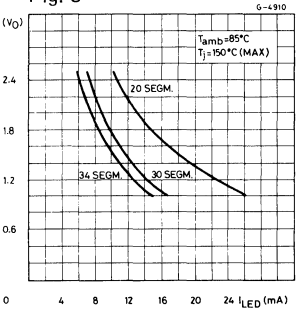
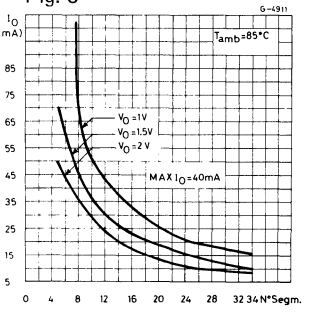
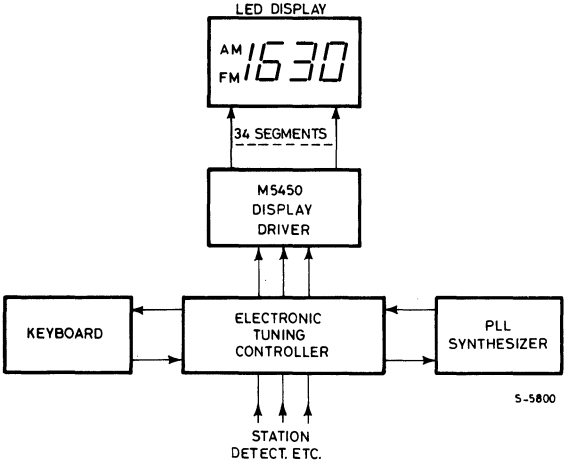


Fig. 6



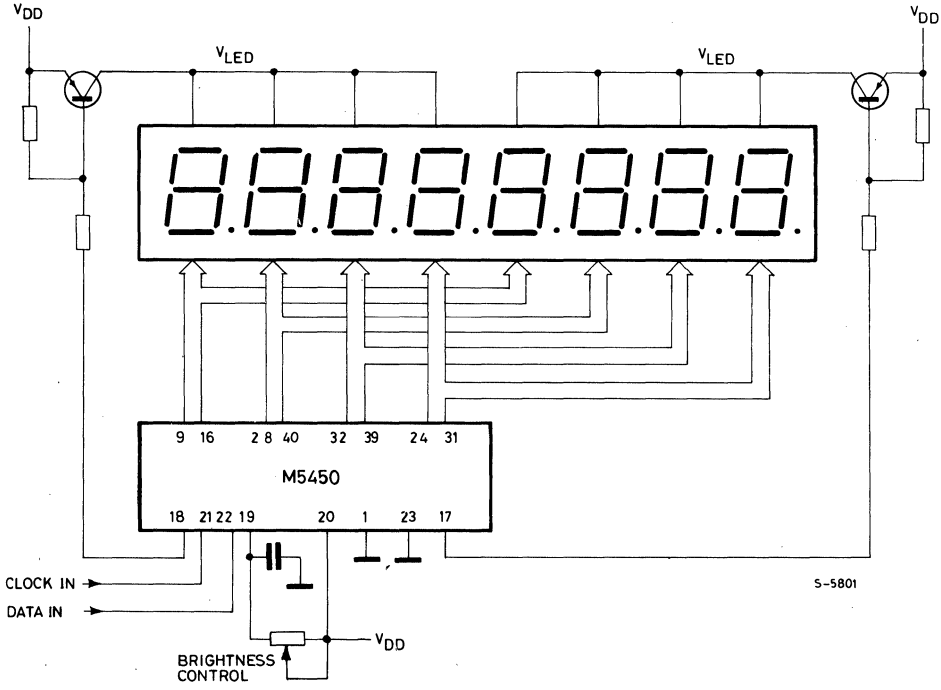
TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system



TYPICAL APPLICATIONS (continued)

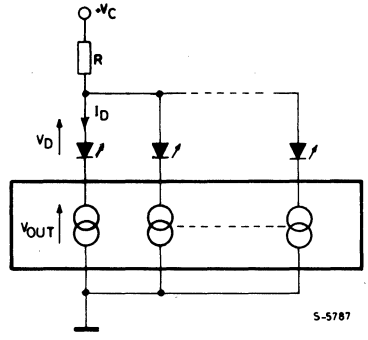
Duplexing 8 Digits with One M5450



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

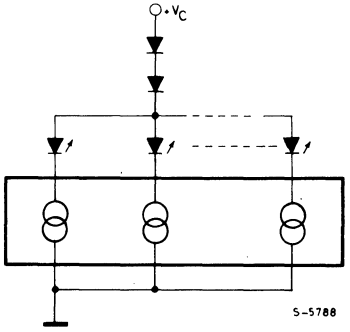


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

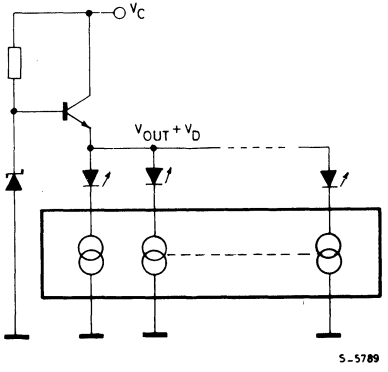
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

M5480

LED DISPLAY DRIVER

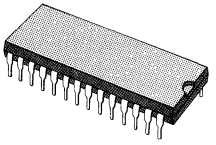
- 3½ DIGIT LED DRIVER (23 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3½ digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5480 is a pin-to-pin replacement of the NS MM 5480.



DIP-28 Plastic

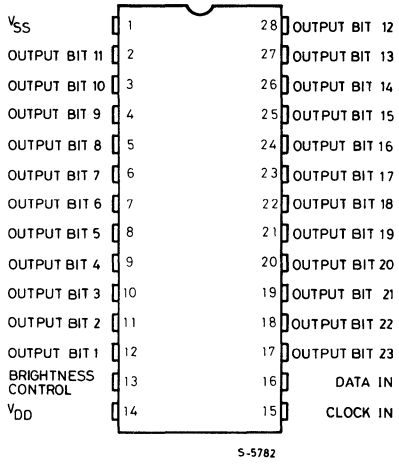
ORDERING NUMBER: M5480 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	940 mW
		at 85°C	490 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

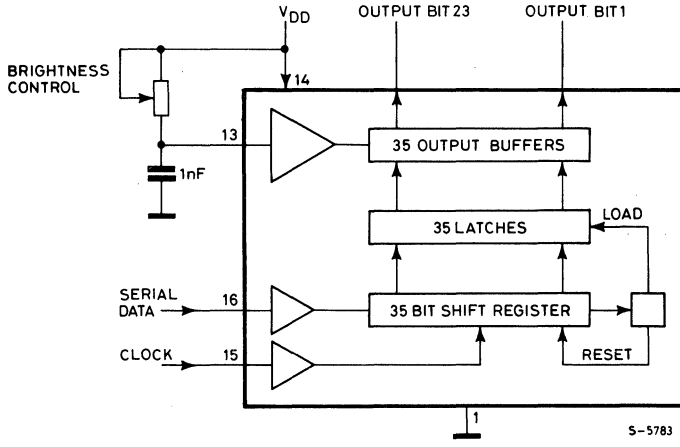
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 µA Input Bias $4.75 \leqslant V_{DD} \leqslant 5.25$ $V_{DD} > 5.25$	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage			13.2	18	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate $3^1/_2$ digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (132\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
132°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

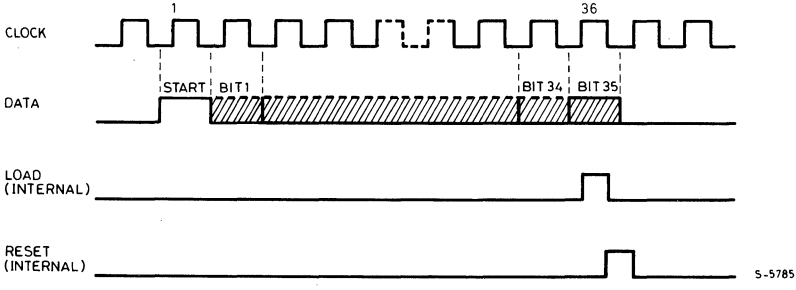


Fig. 3

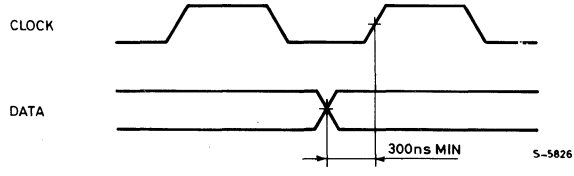
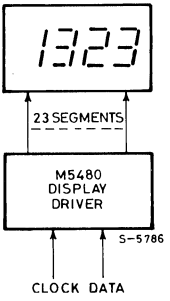


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

TYPICAL APPLICATION

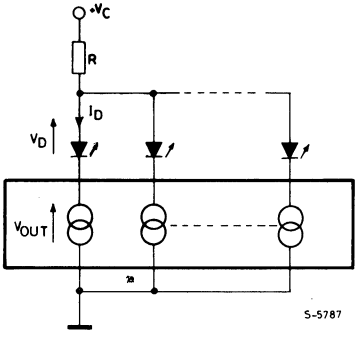
BASIC $3^1/_2$ Digit interface.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

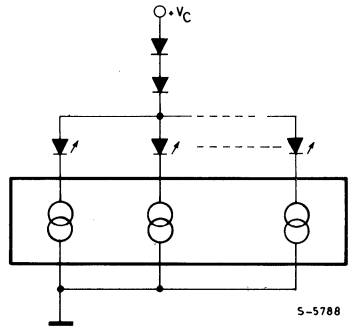


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\ MAX} - V_{OUT\ MIN}}{N_{MAX} \cdot I_D}$$

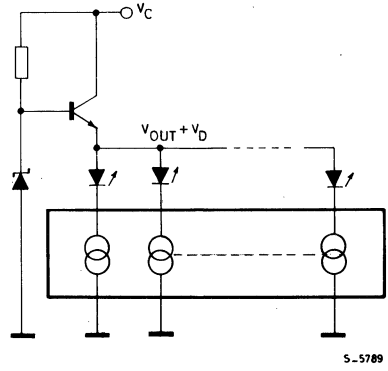
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

M5481

LED DISPLAY DRIVER

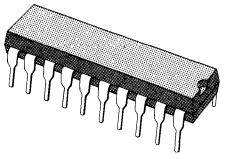
- 2 DIGIT LED DRIVER (14 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5481 is a pin-to-pin replacement of the NS MM 5481.



DIP-20 Plastic
(0.25)

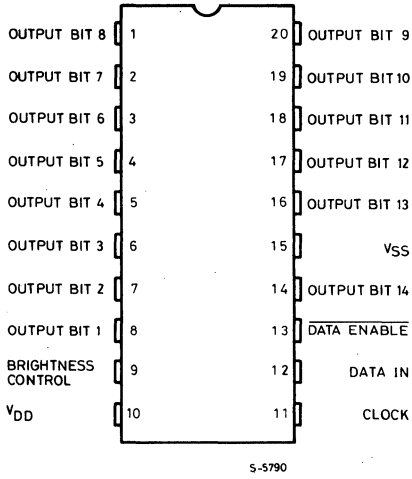
ORDERING NUMBER: M5481 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

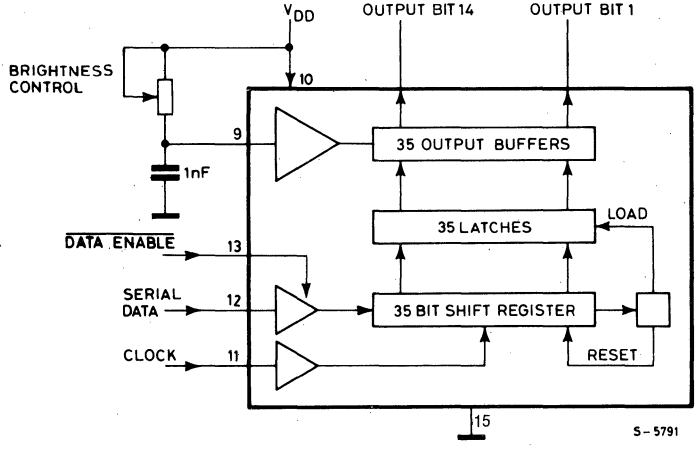
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculates as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non--multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
These is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (80\ °C/W) + T_{amb}$$

where:

T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

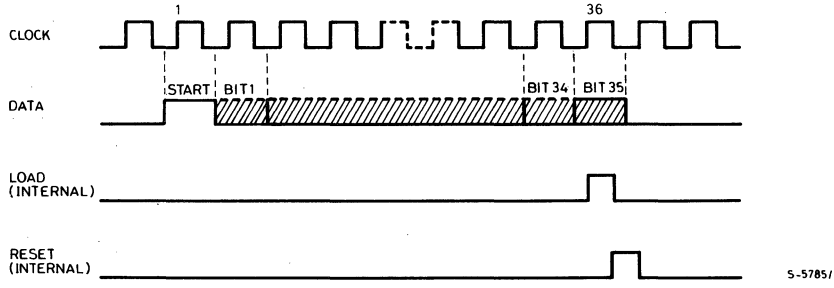


Fig. 3

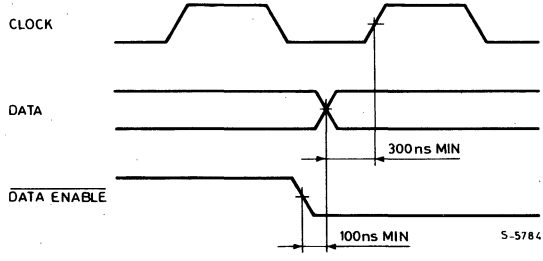
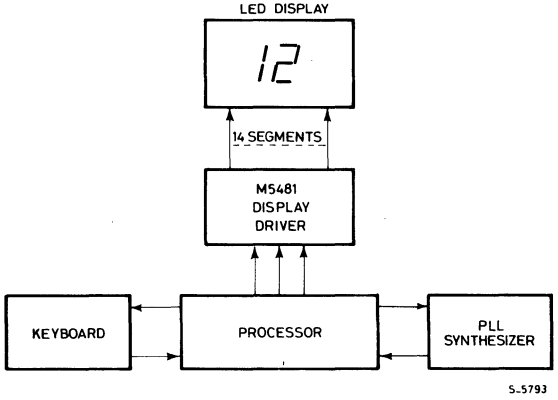


Fig. 4 - Serial Data Bus/Outputs Correspondence

5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

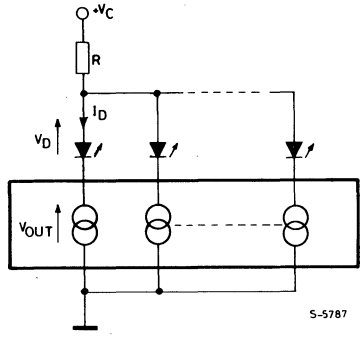
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

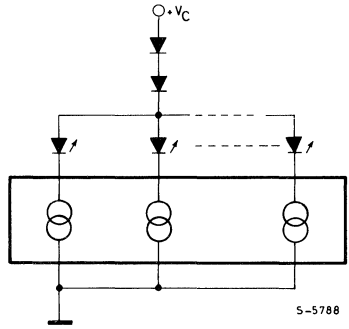


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\ MAX} - V_{O\ MIN}}{N_{MAX} \cdot I_D}$$

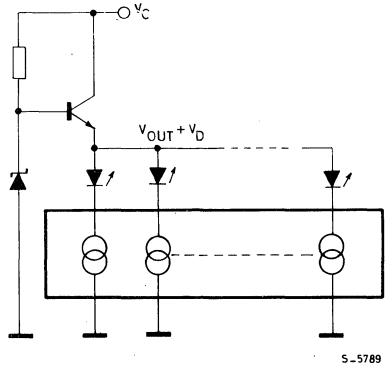
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

M5482

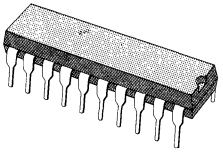
LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (15 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.



DIP-20 Plastic (0.25)

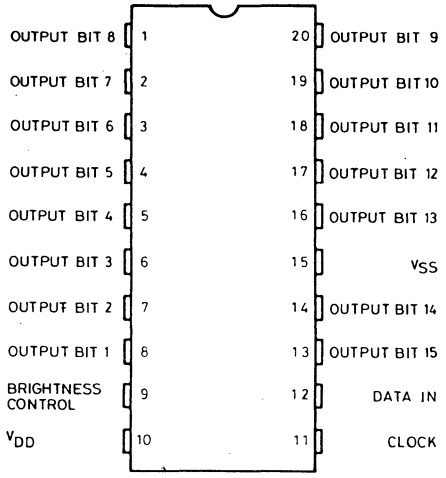
ORDERING NUMBER: M5482 B7

ABSOLUTE MAXIMUM RATINGS

V_{DD}	Supply voltage	-0.3 to 15	V
V_I	Input voltage	-0.3 to 15	V
$V_{O\,(off)}$	Off state output voltage	15	V
I_O	Output sink current	40	mA
P_{tot}	Total package power dissipation	at 25°C	1.5W
		at 85°C	800 mW
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-25 to 85	°C
T_{stg}	Storage temperature range	-65 to 150	°C

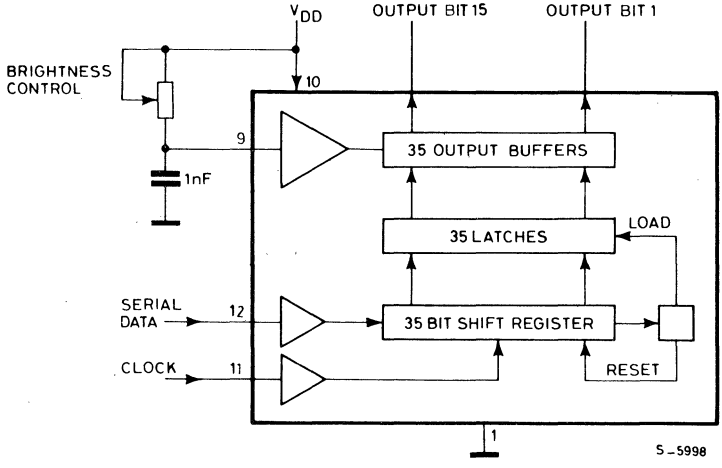
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM



BLOCK DIAGRAM

Fig. 1



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD}= 4.75V to 13.2V, V_{SS}= 0V, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD}= 13.2V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	± 10 μA Input Bias 4.75 ⩽ V_{DD} ⩽ 5.25 V_{DD} > 5.25	 -0.3 2.2 V_{DD}-2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 μA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0 μA Brightness In. = 100 μA Brightness In. = 750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ mA\ ]\ (80\ °C/W) + T_{amb}$$

where:
T_j = junction temperature (150°C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80°C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Fig. 2 - Input Data Format

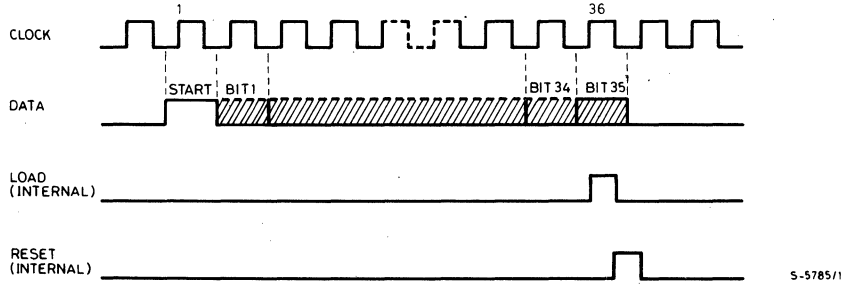


Fig. 3

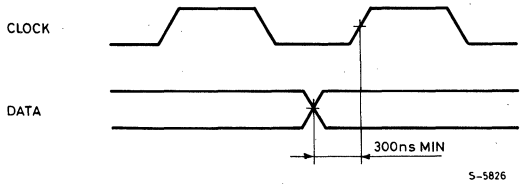
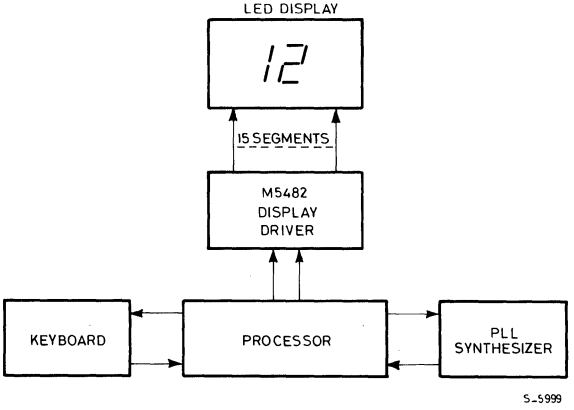


Fig. 4 - Serial Data Bus/Outputs Correspondence

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

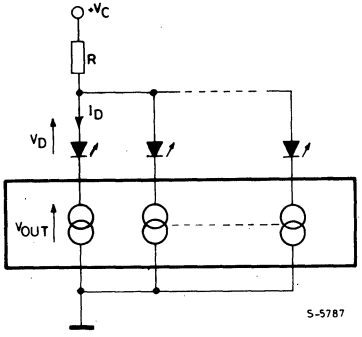
BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

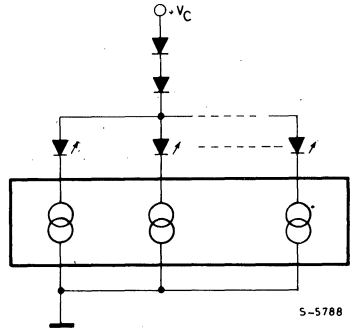


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

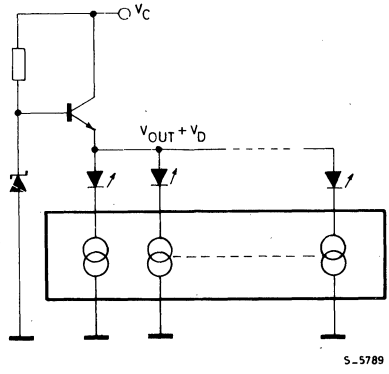
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



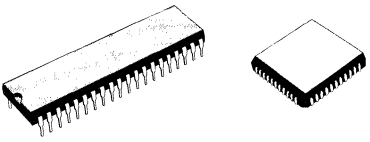
In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON MICROELECTRONICS

M8438A

SERIAL INPUT LCD DRIVER

- DRIVES UP TO 32 LCD SEGMENTS
- DATA TRANSFER: FIXED ENABLE MODE FOR DIP-40, ENABLE AND LATCH-MODE FOR 44PLCC
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- CASCADABLE
- REQUIRES ONLY 3 CONTROL LINES
- ON CHIP OSCILLATOR
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- −40 TO 85°C TEMPERATURE RANGE



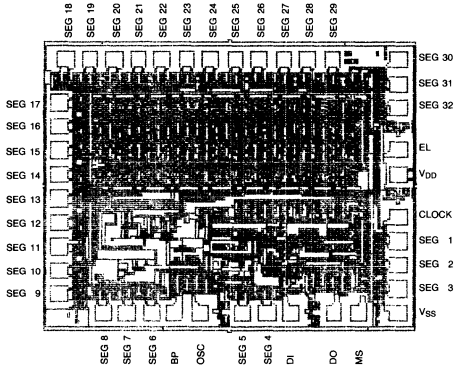
B
DIP-40 Plastic

C
44 PLCC Plastic Chip Carrier

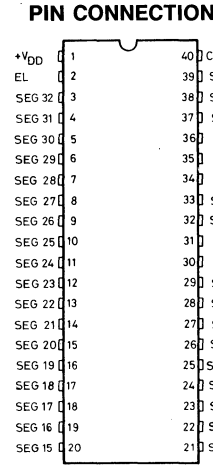
ORDERING NUMBERS: M8438A DIE 1
M8438A B6
M8438A C6

DESCRIPTION

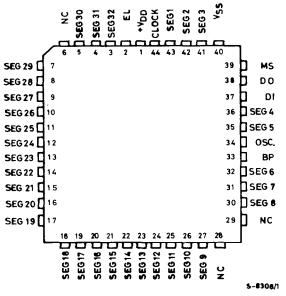
The M8438A is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8438A can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8438A is available in DIE form and assembled in 40 pin dual-in line plastic or 44 PLCC packages.



PIN CONNECTIONS

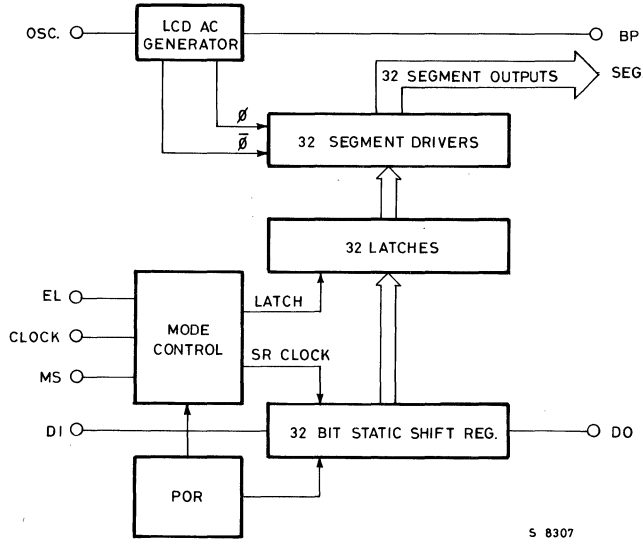


S-8309



S-8308/1

BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
MS :Mode select input (not available in 40 Pin DIL)
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	µA
I_Q	Quiescent Current		V_{DD} = 10V		10	µA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level			0	.2V_{DD}	V
I_{IN}	Input Current				±5	µA
C_I	Input Capacitance				5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level		Driven mode		.1V_{DD}	V
I_{IN}	Input Current		Driven mode		±10	µA
R_{ON}	Segment Output Impedance		I_{IL} = 10µA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100µA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100µA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

The circuit can operate in two different data transfer modes: Enable mode and latch mode. One of either mode can be chosen with the mode select input MS. An internal pull up device is provided between this input and VDD. Enable mode is selected if MS is left open or connected to VDD.
Latch mode is selected if MS is connected to VSS.
The input MS is not available, if the device is assembled in the 40 pin package, and is internally fixed to operate in ENABLE MODE.

ENABLE MODE

Fig. 3 shows a timing diagram of the enable mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted when the enable/latch control EL is high. When EL is low it causes the shift register clock to be inhibited and the content of the shift register to be loaded into the latches that control the segment drivers.

LATCH MODE

Fig. 4 shows a timing diagram of the latch mode. Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

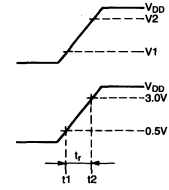
POWER-ON LOGIC

A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V



b) Rise time
t_r min = 10 μs
t_r max = 1 s

c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of enable mode: set-up and hold time

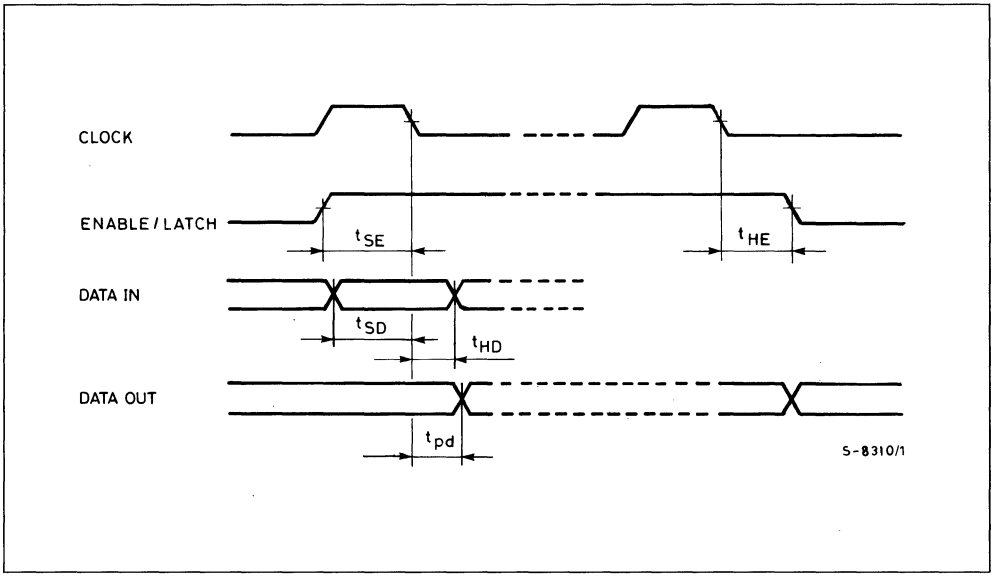


Fig. 2 - Timing diagram of latch mode: set-up and hold time

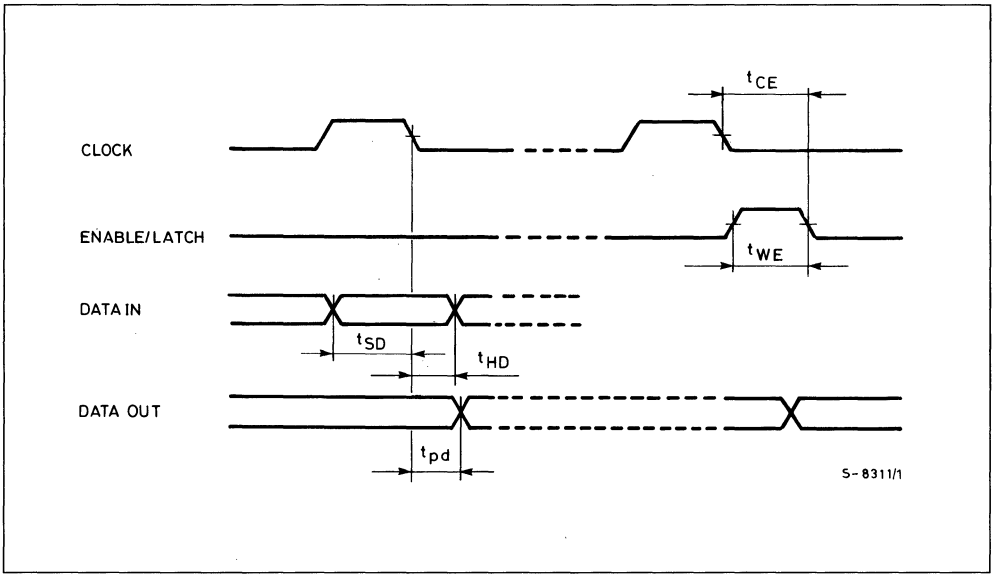


Fig. 3 - Timing diagram of enable mode: Serial load into SR and parallel transfer to LCD

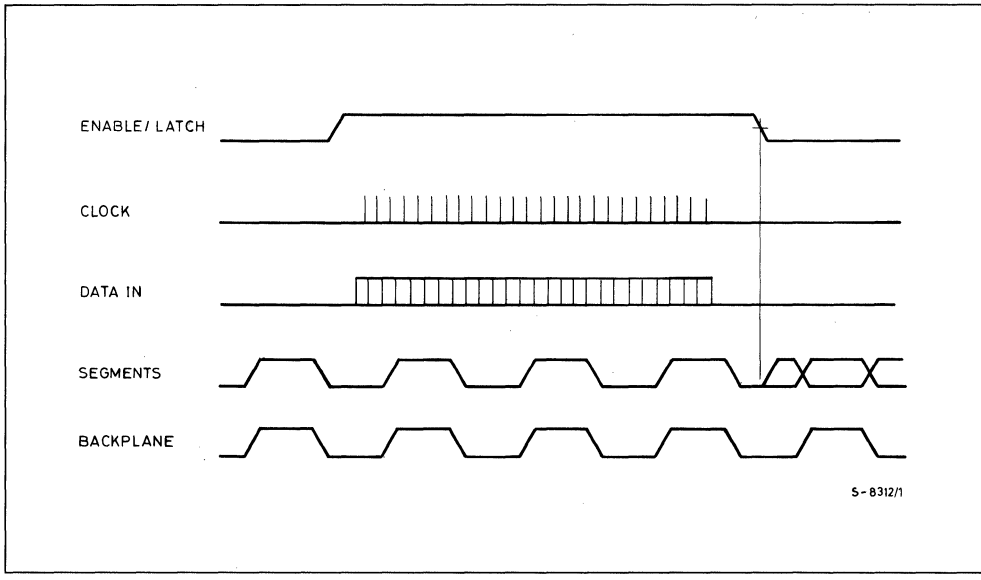


Fig. 4 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

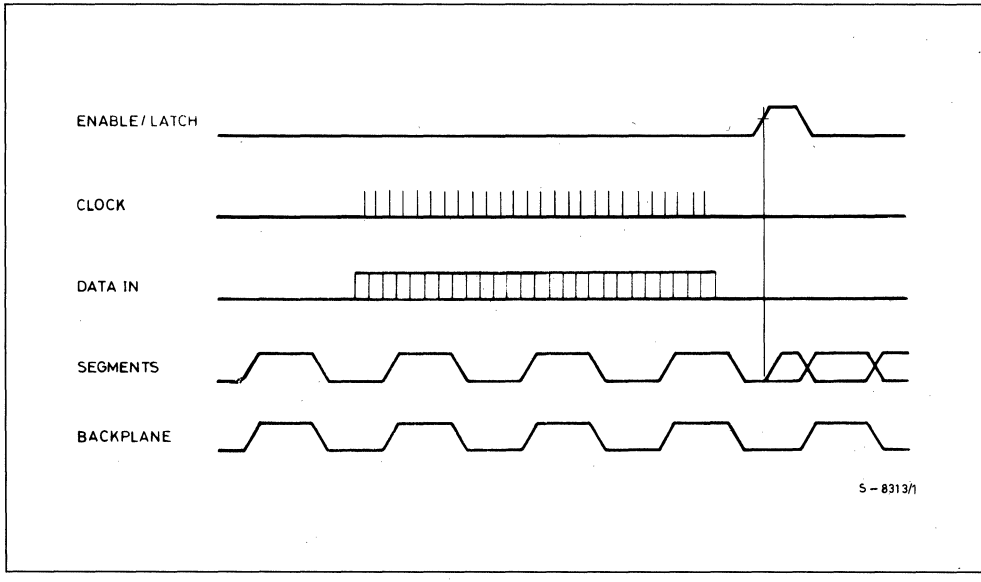


Fig. 5 - Cascade configuration, self oscillating

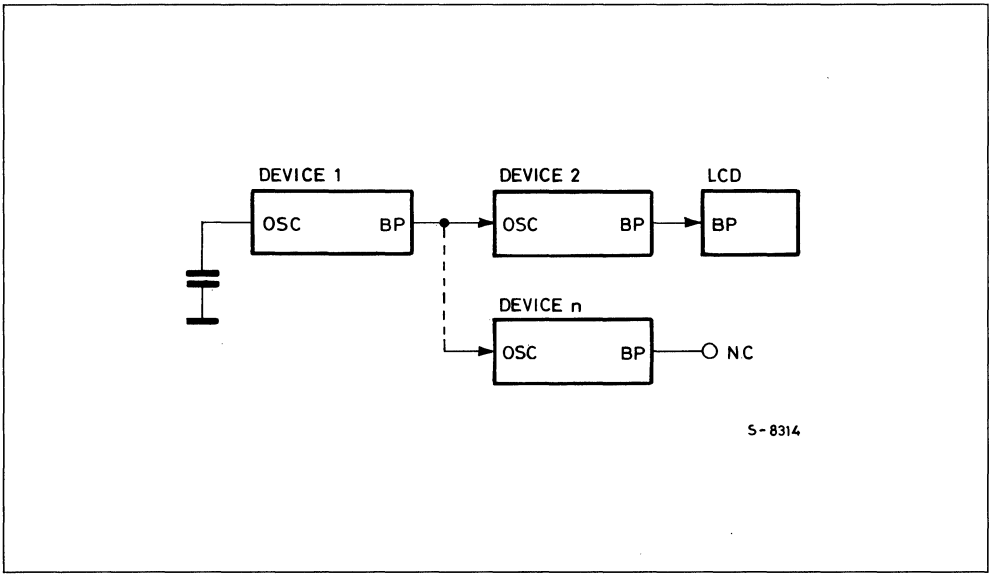
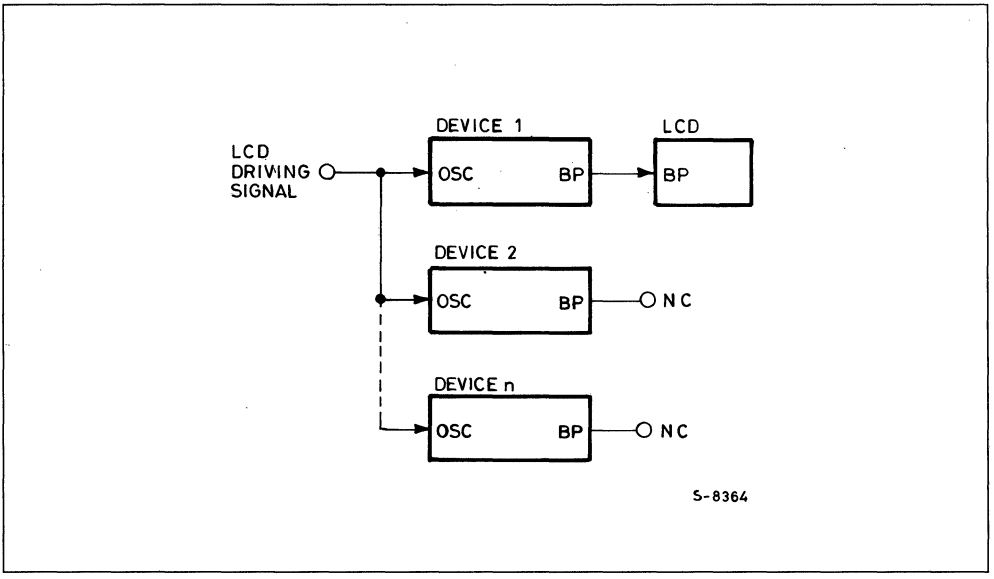
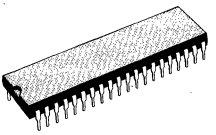


Fig. 6 - Cascade configuration, drive by external signal



SERIAL INPUT LCD DRIVER

- DRIVES UP TO 32 LCD SEGMENTS
- DATA TRANSFER: LATCH MODE
- INPUTS ARE CMOS, NMOS AND TTL COMPATIBLE
- CASCADABLE
- REQUIRES ONLY 3 CONTROL LINES
- ON CHIP OSCILLATOR
- CMOS TECHNOLOGY FOR WIDE SUPPLY VOLTAGE RANGE
- −40 TO 85°C TEMPERATURE RANGE

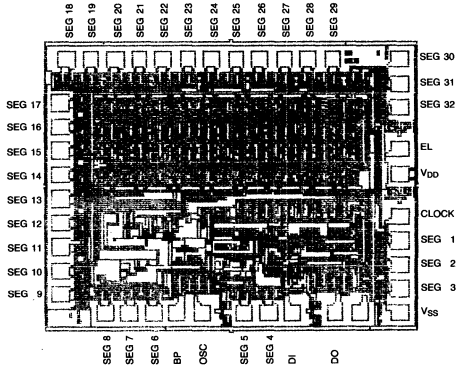


Plastic DIP-40

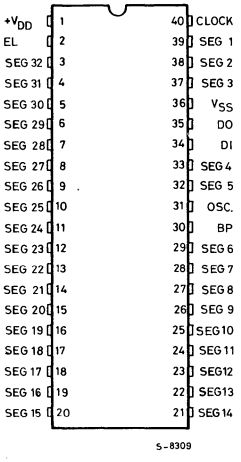
ORDERING NUMBERS: M8439 B6
M8439 DIE 1

DESCRIPTION

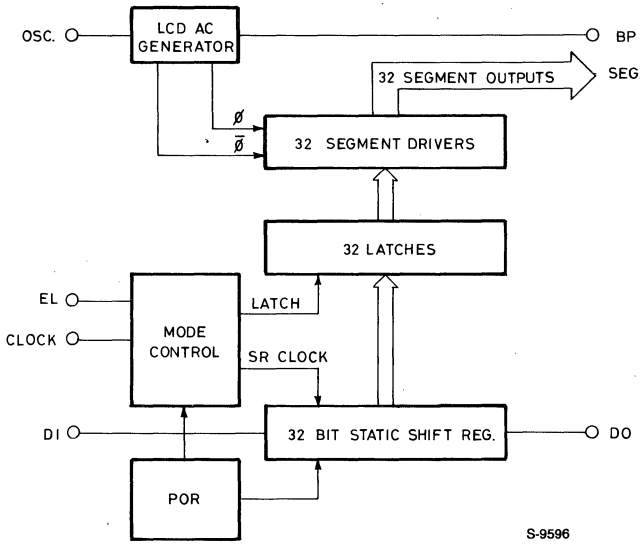
The M8439 is a CMOS integrated circuit that drives an LCD display, usually under microprocessor control. The part acts as a smart peripheral that drives up to 32 LCD segments. It needs only three control lines due to its serial input construction. It latches the data to be displayed and relieves the microprocessor from the task of generating the required waveforms.
The M8439 can drive any standard or custom parallel drive LCD whether it be field effect or dynamic scattering. Several drivers can be cascaded, if more than 32 segments are to be driven. The AC frequency of the LCD waveforms can be supplied by the user or can be generated by attaching a capacitor to the OSC input which determines the frequency of an internal oscillator.
The M8439 is available in DIE form and assembled in 40 pin dual-in line plastic.



PIN CONNECTION



BLOCK DIAGRAM



OSC :Oscillator (capacitor or drive signal)
EL :Enable/Latch control input
DI :Serial data input
DO :Serial data output
BP :Backplane output
SEG :Segment output signal

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
(VDD-VSS)	Supply voltage	−0.3 to +12	V
V_I	Input voltage	VSS−0.3 to VDD+0.3	V
V_O	Output voltage	VSS−0.3 to VDD+0.3	V
P_D	Power dissipation	250	mW
T_{stg}	Storage temperature	−55 to +125	°C
T_A	Operating temperature	−40 to +85	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C and V_{DD} = 5V unless otherwise noted)

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage			3	10	V
I_{DD}	Supply Current		Oscillator f < 15kHz		60	µA
I_Q	Quiescent Current		V_{DD} = 10V		10	µA
V_{IH}	Input High Level	CLOCK DI EL		.5V_{DD}	V_{DD}	V
V_{IL}	Input Low Level	CLOCK DI EL		0	.2V_{DD}	V
I_{IN}	Input Current	CLOCK DI EL			±5	µA
C_I	Input Capacitance	CLOCK DI EL			5	pF
V_{IH}	Input High Level	OSC	Driven mode	.9V_{DD}		V
V_{IL}	Input Low Level	OSC	Driven mode		.1V_{DD}	V
I_{IN}	Input Current	OSC	Driven mode		±10	µA
R_{ON}	Segment Output Impedance		I_{IL} = 10µA		40	kΩ
R_{ON}	Backplane Output Impedance		I_L = 100µA		3	kΩ
V_{OFF}	Output Offset Voltage		C_L = 250pF between each SEG output and BP		±50	mV
R_{ON}	Data Output Impedance		I_L = 100µA		3	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{TR}	Transition Time OSC	Driven mode		500	ns
t_{SD}	Data Set-up Time	Fig. 1 and 2	150		ns
t_{HD}	Data Hold Time	Fig. 1 and 2	50		ns
t_{SE}	EL Set-up Time	Fig. 1	100		ns
t_{HE}	EL Hold Time	Fig. 1	100		ns
t_{WE}	EL Pulse Width	Fig. 2	175		ns
t_{CE}	Clock to EL Time	Fig. 2	250		ns
t_{pd}	DO Propagation Delay	Fig. 1, 2; C_L = 55pF		500	ns
f	Clock Rate	V_{DD} = 10 50% duty cycle;	DC	1.5	MHz

FUNCTIONAL DESCRIPTION

LCD-AC-GENERATOR

This block generates a 50% duty cycle signal for the backplane output. The circuit can be used in two different modes: oscillator or driven.

OSCILLATOR MODE:

In this mode the backplane frequency is determined by the internal RC oscillator together with an 8-stage frequency divider. For generating the backplane output signal of 50% duty cycle the oscillator frequency is divided by 256. The RC oscillator requires an external capacitor to be connected between input OSC and VSS. A value of 18pF gives a backplane frequency of 80Hz ± 30% at VDD = 5V. The variation of the backplane frequency over the entire temperature and supply voltage range is ± 50%.

DRIVEN MODE:

In this mode the signal at the backplane output BP is in phase with an external driving signal applied to input OSC. This mode is used to synchronize the LCD drive of two or more cascaded driver circuits.

FUNCTIONAL DESCRIPTION (continued)

DETECTION LOGIC

The circuit is able to distinguish between the conditions for oscillator or driven mode. If the circuit is to be in the oscillator mode, the OSC pin has a capacitor connected to it. The oscillator will start as soon as the supply voltage exceeds a certain minimim value. The signal at pin OSC swings within a range from $0.3V_{DD}$ to $0.7V_{DD}$. If the circuit is to be in the driven mode, the OSC pin has to be forced to logic levels by an external source. The transition time between the logic levels must be short, so that the circuit does not react on the voltage level in between. In the driven mode the 8-stage frequency divider is by-passed.

SEGMENT OUTPUTS

A logic 0 at the data input DI causes a segment output signal to be in phase with the backplane signal and turns the segment off. A logic 1 causes a segment output to be in opposite phase to the backplane signal and turns the segment on.

MICROPROCESSOR INTERFACE

Fig. 2 shows a timing diagram.
Data is serially shifted in and out of the shift register on the negative transition of the clock.
Serial entry into the shift register is permitted independently of the enable/latch control EL. When EL is high it causes a parallel load of the content in the shift register into the latches. It is acceptable to tie the EL line high. Then the latches are transparent and only two lines, clock and data input, would then be needed for data transfer.

POWER-ON LOGIC

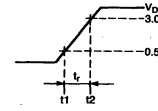
A power on reset pulse is generated internally when the supply voltage is being turned on. The generation of the reset pulse is level dependent and will occur even on a slowly rising supply voltage.
The power on reset pulse resets all shift register stages and the latches that control the segment drivers. Therefore all segment outputs are initially in phase with the backplane output. This causes the display to be blanked and no arbitrary data to show up. This condition is maintained until data is shifted into the register and loaded into the latches.

CONDITIONS FOR POWER-ON RESET FUNCTION

The POR circuit triggers on the rising slope of the positive supply voltage V_{DD}. A reset pulse will be generated, if conditions a) through d) are given:

a) Level
Rising slope from V1 to V2
V1 max = 0.5V
V2 min = 3.0V

b) Rise time
t_r min = 10 μs
t_r max = 1 s



c) Rise function
The function of V_{DD} between t1 und t2 may be nonlinear, but should not show a maximum and should not exceed 0.25 V/μs.

d) Recovery time
The minimum time between turn-off and turn-on of V_{DD} is 1s.

CASCADE CONFIGURATION

Several LCD drivers can be cascaded if a liquid crystal display with more than 32 segments is to be connected.
The phase correlation between all segment outputs is achieved by using the second (and any other) device in the driven mode.
Two different cascade configurations can be chosen depending whether the LCD frequency is to be determined by the internal RC oscillator or by an external signal.
Figure 3 shows the connection scheme for a self oscillating configuration, figure 4 shows the connection of an externally controlled one.

Fig. 1 - Timing diagram of latch mode: set-up and hold time

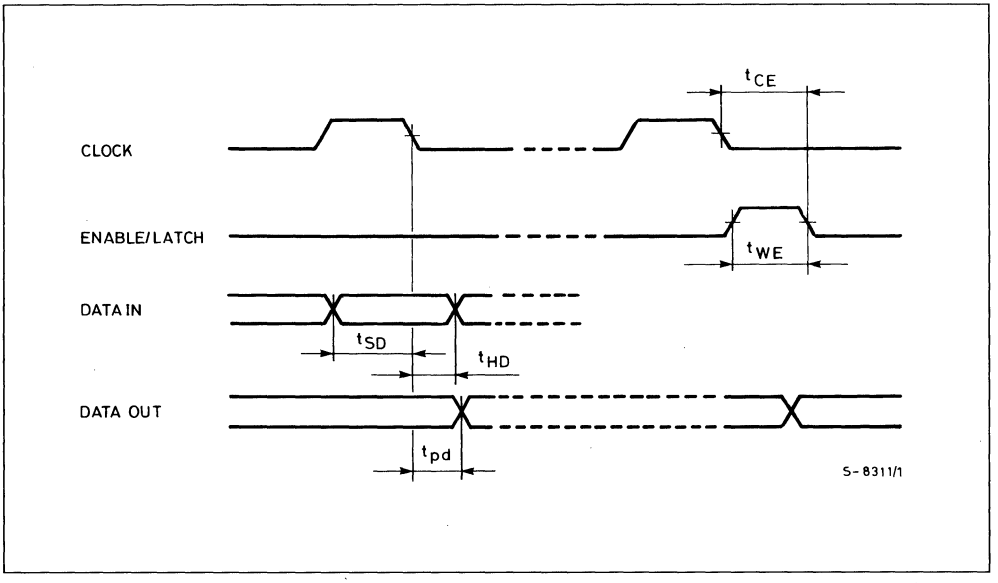


Fig. 2 - Timing diagram of latch mode: Serial load into SR and parallel transfer to LCD

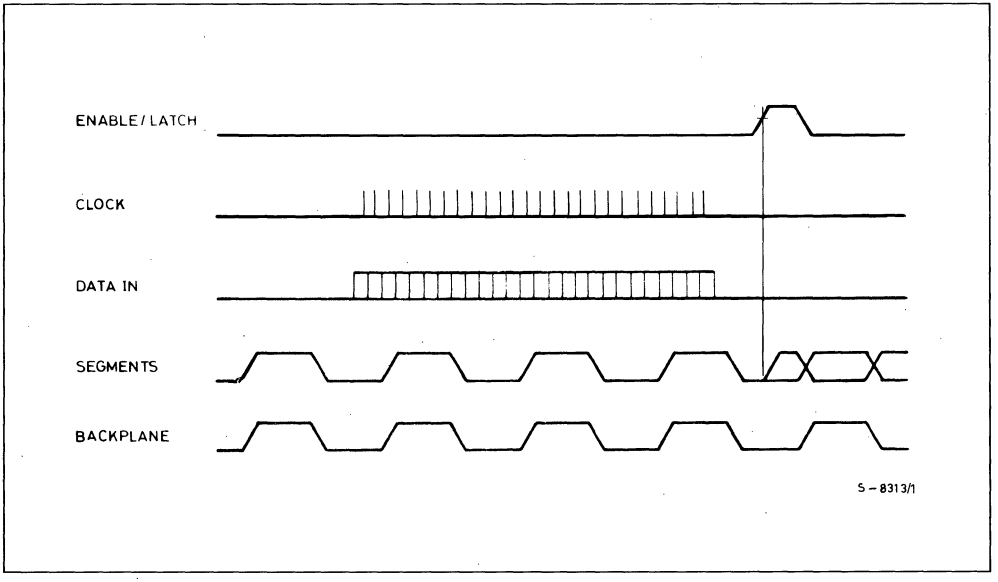


Fig. 3 - Cascade configuration, self oscillating

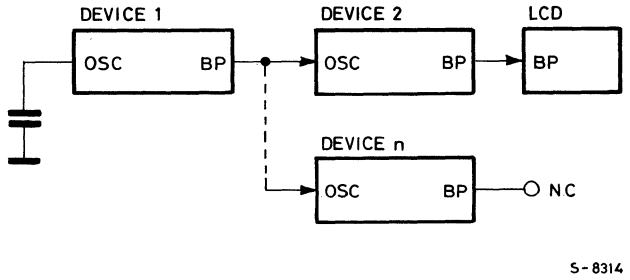
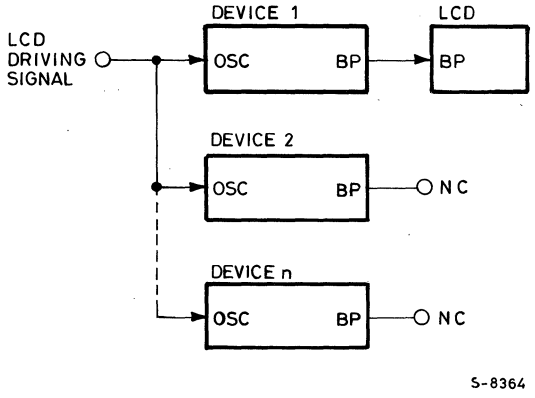


Fig. 4 - Cascade configuration, driven by external signal



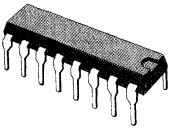
REMOTE CONTROL ENCODER/DECODER CIRCUITS

- M145026 ENCODER
- M145027/M145028 DECODERS
- MAY BE ADDRESSED IN EITHER BINARY OR TRINARY
- TRINARY ADDRESSING MAXIMIZES NUMBER OF CODES
- INTERFACES WITH RF, ULTRASONIC, OR INFRARED TRANSMISSION MEDIAS
- DOUBLE TRANSMISSIONS FOR ERROR CHECKING
- 4.5V TO 18V OPERATION
- ON-CHIP R/C OSCILLATOR, NO CRYSTAL REQUIRED
- HIGH EXTERNAL COMPONENT TOLERANCE, CAN USE 5% COMPONENTS
- STANDARD CMOS B-SERIES INPUT AND OUTPUT CHARACTERISTICS
- APPLICATIONS INCLUDE GARAGE DOOR OPENERS, REMOTE CONTROLLED TOYS, SECURITY MONITORING, ANTITHEFT SYSTEMS, LOW END DATA TRANSMISSIONS, WIRE LESS TELEPHONES

The M145026 encodes nine bits of information and serially transmits this information upon receipt of a transmit enable, $\overline{TE}$, (active low) signal. Nine inputs may be encoded with trinary data (0, 1, open) to allow 3^9 (19,683) different codes.

Two decoders are presently available. Both use the same transmitter - the M145026. The decoders will receive the 9-bit word and will interpret some of the bits as address codes and some as data. The M145028 treats all nine bits as address. If no errors are received, the M145027 outputs the four data bits when the transmitter sends address codes that match that of the receiver. A valid transmission output goes high on both decoders when they recognize an address that matches that of the decoder. Other receivers can be produced with different address/data ratios.

All the devices are available in 16 lead plastic package.

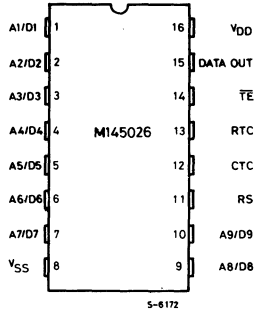


DIP-16 Plastic
(0.25)

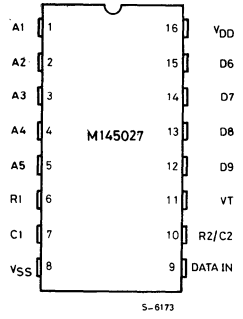
ORDER CODE: M145026 B1
M145027 B1
M145028 B1

CONNECTION DIAGRAMS

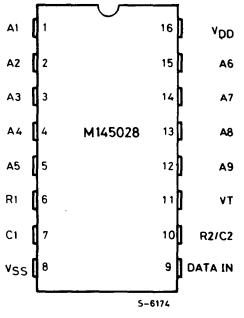
Encoder



Decoder



Decoder



ABSOLUTE MAXIMUM RATINGS

V_{DD}	DC Supply Voltage	-0.5 to +18	V
V_I	Input Voltage, All Inputs	-0.5 to V_{DD} +0.5	V
I_I	DC Current Drain Per Pin	10	mA
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_{op}	Operating Temperature Range	-40 to +85	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_{amb} = 25°C)

	Parameter	V_{DD}	Min	Typ	Max	Unit
t_{TLH} t_{THL}	Output Rise and Fall Time	5 10 15	– – –	100 50 40	200 100 80	ns
t_{TLH} t_{THL}	Data In Rise and Fall Time (M145027, M145028)	5 10 15	– – –	– – –	15 15 15	µs
f_{CL}	Encoder Clock Frequency	5 10 15	0 0 0	– – –	2 5 5	MHz
f_{CL}	Maximum Decoder Frequency (Referenced to Encoder Clock) (See Figure 9)	5 10 15	– – –	– – –	240 410 450	kHz
t_{WL}	$\overline{TE}$ Pulse Width	5 10 15	65 30 20	– – –	– – –	ns
	System Propagation Delay ($\overline{TE}$ to Valid Transmission)	–	–	182	–	Clock Cycles
	Tolerance on Timing Components (ΔRTC + ΔCTC + ΔR1 + ΔC1) (ΔR2 + ΔC2)	 – –	 – –	 – –	 ±25 ±25	%

ELECTRICAL CHARACTERISTICS

Parameter		V_{DD}	-40°C		25°C			+85°C		Unit
		V	Min	Max	Min	Typ	Max	Min	Max	
V_{OL}	Output Voltage V_I = V_{DD} or 0 "0" Level	5	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
V_{OH}	V_I = 0 or V_{DD} "1" Level	5	4.95	–	4.95	5	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
V_{IL}	Input Voltage (V_O = 4.5 or 0.5V) "0" Level	5	–	1.5	–	2.25	1.5	–	1.5	V
	(V_O = 0.9 or 1V)	10	–	3	–	4.50	3	–	3	
	(V_O = 13.5 or 1.5V)	15	–	4	–	6.25	4	–	4	
V_{IH}	(V_O = 0.5 or 4.5V) "1" Level	5	3.5	–	3.5	2.75	–	3.5	–	V
	(V_O = 1.0 or 9V)	10	7	–	7	5.50	–	7	–	
	(V_O = 1.5 or 13.5V)	15	11	–	11	8.25	–	11	–	
I_{OH}	Output Drive Current (V_{OH} = 2.5V) Source	5	-2.5	–	-2.1	-4.2	–	-1.7	–	mA
	(V_{OH} = 4.6V)	5	-0.52	–	-0.44	-0.88	–	-0.36	–	
	(V_{OH} = 9.5V)	10	-1.3	–	-1.1	-2.25	–	-0.9	–	
	(V_{OH} = 13.5V)	15	-3.6	–	-3	-8.8	–	-2.4	–	
I_{OL}	(V_{OL} = 0.4V) Sink	5	0.52	–	0.44	0.88	–	0.36	–	mA
	(V_{OL} = 0.5V)	10	1.3	–	1.1	2.25	–	0.9	–	
	(V_{OL} = 1.5V)	15	3.6	–	3	8.8	–	2.4	–	
I_I	Input Current $\overline{TE}$ (M145026, Pullup Device)	5	–	–	3	4	7	–	–	µA
		10	–	–	16	20	26	–	–	
		15	–	–	35	45	55	–	–	
I_I	Input Current RS (M145026) Data In (M145027, M145028)	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
I_I	Input Current A1/D1–A9/D9 (M145026)	5	–	–	–	±55	±80	–	–	µA
	A1–A5 (M145027)	10	–	–	–	±300	±340	–	–	
	A1–A9 (M145028)	15	–	–	–	±650	±725	–	–	
C_I	Input Capacitance (V_I = 0)	–	–	–	–	5	7.5	–	–	pF
I_{DD}	Quiescent Current - M145026	5	–	–	–	0.0050	0.10	–	–	µA
		10	–	–	–	0.0100	0.20	–	–	
		15	–	–	–	0.0150	0.30	–	–	
I_{DD}	Quiescent Current M145027, M145028	5	–	–	–	30	50	–	–	µA
		10	–	–	–	60	100	–	–	
		15	–	–	–	90	150	–	–	
I_T	Total Supply Current M145026 (f_{CL}= 20 kHz)	5	–	–	–	100	200	–	–	µA
		10	–	–	–	200	400	–	–	
		15	–	–	–	300	600	–	–	
I_T	Total Supply Current M145027, M145028 (f_{CL}= 20 kHz)	5	–	–	–	200	400	–	–	µA
		10	–	–	–	400	800	–	–	
		15	–	–	–	600	1200	–	–	

OPERATING CHARACTERISTICS

M145026

The encoder will serially transmit nine bits of trinary data as defined by the state of the A1/D1-A9/D9 input pins. These pins can be in either of three states (0, 1, open) allowing $3^9 = 19683$ possible codes. The transmit sequence will be initiated by a low level of the $\overline{TE}$ input pin. Each time the $\overline{TE}$ input is forced low the encoder will output two identical data words. This redundant information is used by the receiver to reduce errors. If the $\overline{TE}$ input is kept low, the encoder will continuously transmit the data words. The transmitted words are self-completing (two words will be transmitted for each $\overline{TE}$ pulse).
Each transmitted data bit is encoded into two data pulses. A logic zero will be encoded as two consecutive short pulses, a logic one by two consecutive long pulses, and an open as a long pulse followed by a short pulse. The input state is determined by using a weak output device to try to force each input first low, then high. If only a high state results from the two tests, the input is assumed to be hard wired to V_{DD}. If only a low state is obtained, the input is assumed to be hard wired to V_{SS}. If both a high and a low can be forced at an input, it is assumed to be open and is encoded as such.
The transmit sequence is enabled by a logic zero on the $\overline{TE}$ input. This input has an internal pullup device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high the encoder is completely disabled, the oscillator is inhibited and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started, and an internal reset is generated to initialize the transmit sequence. Each input is then sequentially selected and a determination is made as to input logic state. This information is serially transmitted via the Data Out output pin.

M145027

The decoder will receive the serial data from the encoder, check it for errors and output data if valid. The transmitted data consisting of two identical data words is examined bit by bit as it is received. The first five bits are assumed to be address bits and must be encoded to match the address inputs at the receiver. If the address bits match, the next four (data) bits are stored and compared to the last valid data stored. If this data matches, the VT pin will go high on the 2nd rising edge of the 9th bit of the first word. Between the two data words no signal is sent for three data bit times. As the second encoded word is received, the address must again match, and if it does, the data bits are checked against the previously stored data bits. If the two words of data (four bits each) match, the data is transferred to the output data latches and will remain until new data replaces it. At the same time, the Valid Transmission output pin is brought high and will remain high until an error is received or until no input signal is received for four data bit times.
Although the address information is encoded in trinary fashion, the data information must be either a one or a zero. A trinary (open) will be decoded as a logic one.

M145028

This receiver operates in the same manner as the M145027 except that nine address bits are used and no data output is available. The Valid Transmission output is used to indicate that a valid signal has been received.
Although address information normally is encoded in trinary, the designer should be aware that, for the M145028, the ninth address bit (A9) must be either a one or a zero. This part, therefore, can accept only $2 \times 3^8 = 13{,}122$ different codes. A trinary (open) A9 will be interpreted as a logic 1. However if the transmitter sends a trinary (or logic 1) and the receiver address is a logic 1 (or trinary) respectively, the valid transmission output will be shortened to the R1 x C1 time constant.

DOUBLE TRANSMISSION DECODING

Although the encoder sends two words for error checking, a decoder does not necessarily wait for two transmitted words to be received before issuing a valid transmission output. Refer to the flowcharts in Figure 7 and 8.

Fig. 1 - Encoder block diagram M145026

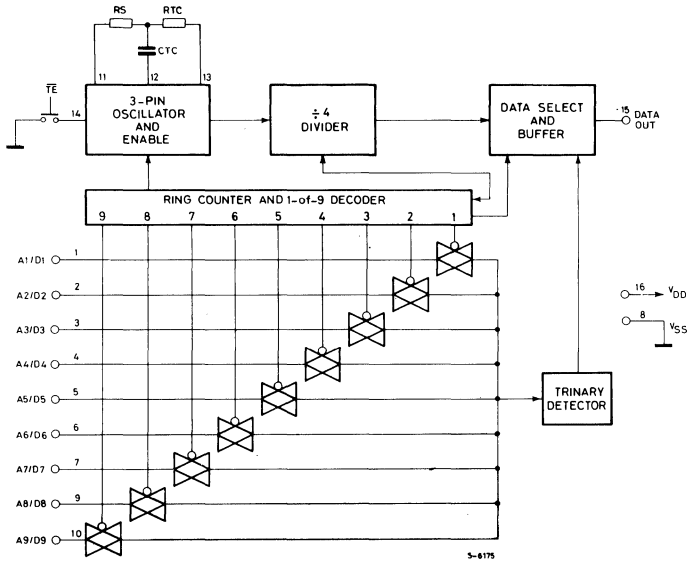


Fig. 2 - Decoder block diagram M145027

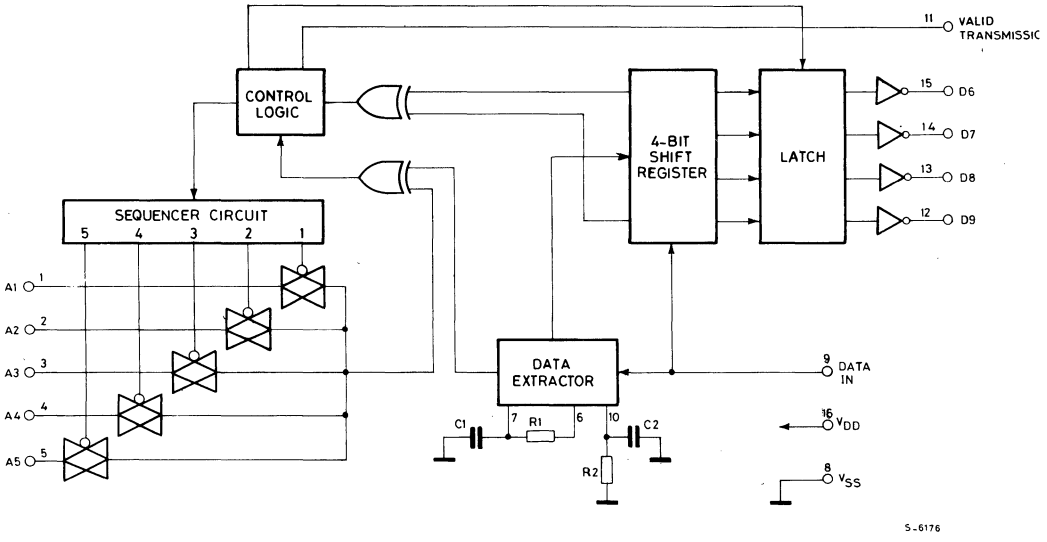
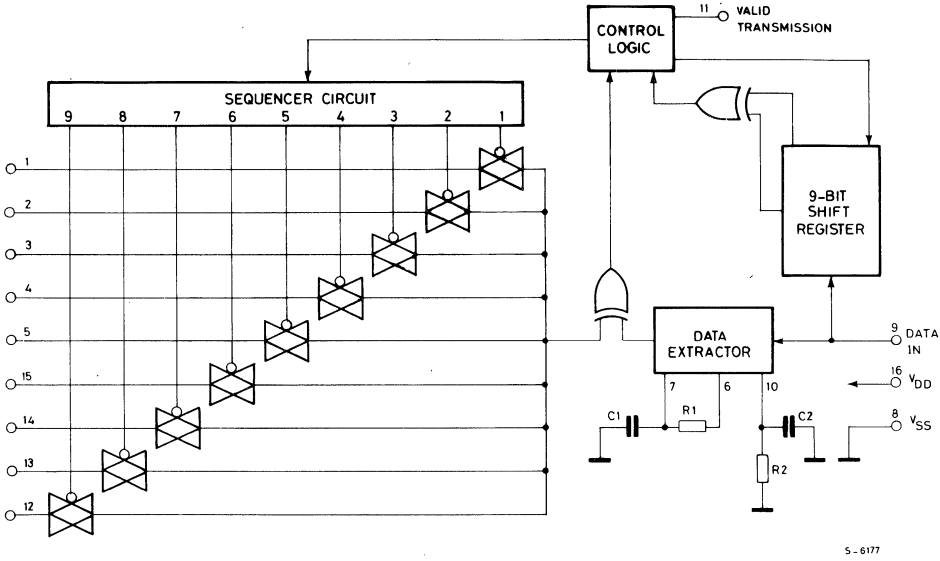


Fig. 3 - Decoder block diagram M145028



PIN DESCRIPTION

M145026 ENCODER

A1/D1-A9/D9
These inputs will be encoded and the data serially output from the encoder.

V_{SS}
The most negative supply (usually ground).

RS, CTC, RTC
These pins are part of the oscillator section of the encoder. If an external signal source is used instead of the internal oscillator it should be connected to the RS input and the RTC and CTC pins should be left open.

$\overline{TE}$
This Transmit-Enable (active low) input will initiate transmission when forced low. A pullup device will keep this input high normally.

Data Out
This is the output of the encoder that will present the serially encoded signals.

V_{DD}
The most positive supply.

M145027/M145028 DECODERS

A1-A5 (M145027) / A1-A9 (M145028)
These are the address inputs that must match the encoder inputs A1/D1-A5/D5 in the case of M145027 or A1/D1-A0/D9 in the case of M145028, in order for the decoder to output data.

D6-D9 (M145027)
These outputs will give the information that is presented to the encoder inputs A6/D6-A9/D9.
Note: Only binary data will be acknowledged, a trinary open will be decoded as logic one.

R1, C1
These pins accept a resistor and capacitor that are used to determine whether a narrow pulse or a wide pulse has been encoded. The time constant R1 x C1 should be set to 1.72 transmit clock periods. R1C1 = 3.95 RTC x CTC.

R2/C2
This pin accepts a resistor to V_{SS} and a capacitor to V_{SS} that are used to detect both the end of an encoded word and the end of transmission. The time constant R2 x C2 should be 33.5 transmit clock periods (four data bit periods). This time constant is used to determine that the Data In input has remained low for four data bit times (end of transmission). A separate comparator looks at a voltage equivalent two data bit times (0.4 R2C2) to detect the dead time between transmitted words.
R2C2 = 77 x RTC x CTC.

Valid Transmission, VT
This output will go high when the following conditions are satisfied:

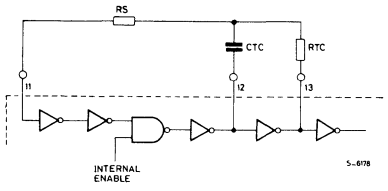
1. the transmitted address matches the receiver address, and
2. the transmitted data matches the last valid data received (M145028 only).

VT will remain high until either a mismatch is received, or no input signal is received for four data data bit times.

V_{DD}
The most positive supply

V_{SS}
The most negative supply (usually ground).

Figure 4 - Encoder Oscillator Information



This oscillator will operate at a frequency determined by the external RC network; i.e..

$$f \cong \frac{1}{2.3 \times RTC \times CTC} \quad (Hz)$$

for $1\ kHz \leqslant f \leqslant 400\ kHz$

where: CTC = CTC + C layout + 12 pF

$RS \approx 2\ RTC$
$RS \geqslant 20\ k$
$RTC \geqslant 10\ k$
$400\ pF < CTC < \mu F$

The value for RS should be chosen to be about 2 times RTC. This range will ensure that current through RS is insignificant compared to current through RTC. The upper limit for RS must ensure that RS x 5 pF (input capacitance) is small compared to RTC x CTC.

For frequencies outside the indicated range, the formula will be less accurate. The actual oscillation range of this circuit is from less than 1 Hz to over 1 MHz.

Figure 5 - Encoder/Decoder Timing Diagram

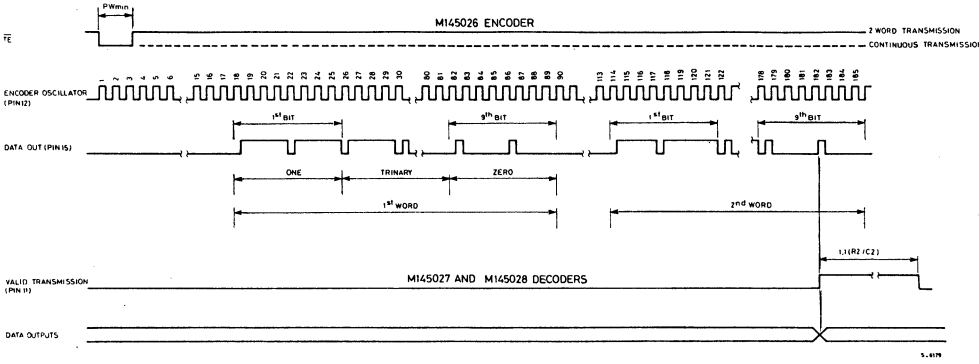
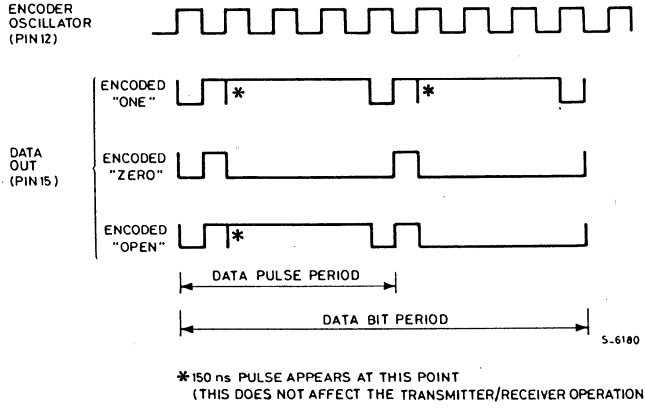


Figure 6 - Encoder Data Waveforms (M145026)



*150 ns PULSE APPEARS AT THIS POINT
(THIS DOES NOT AFFECT THE TRANSMITTER/RECEIVER OPERATION)

Figure 7 - M145027 Flowchart

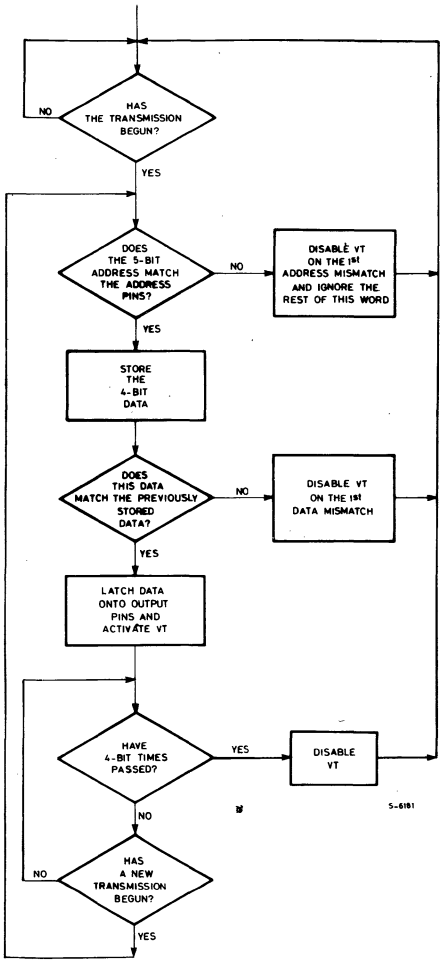


Figure 8 - M145028 Flowchart

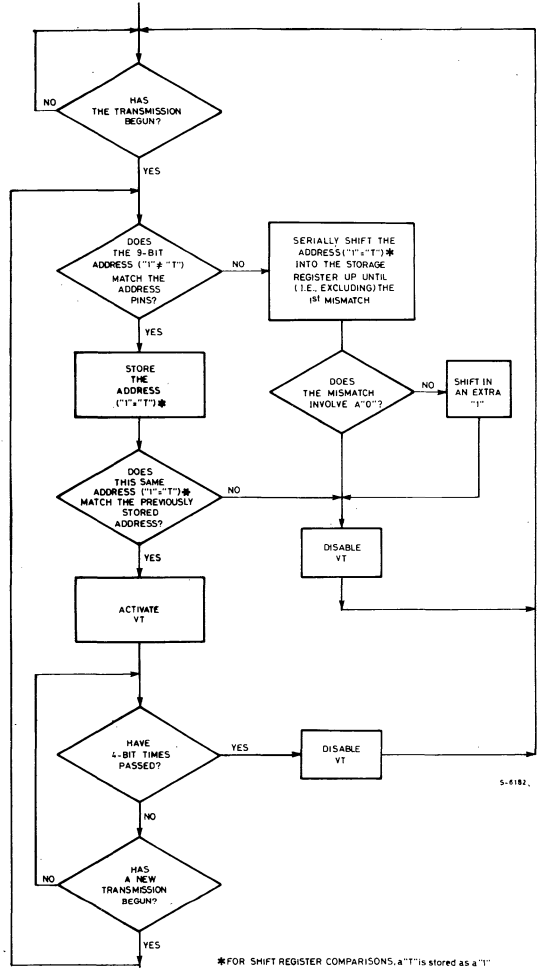


Figure 9 - M145027/M145028 (f_{max} vs. C_{layout})

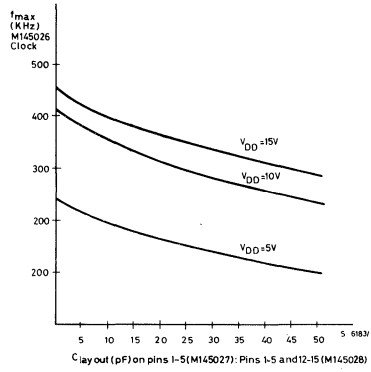
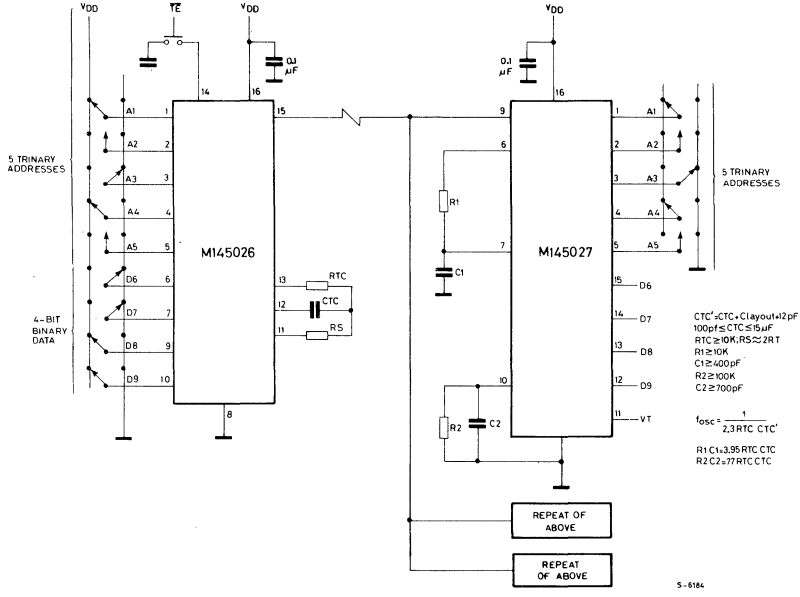


Figure 10 - Typical Application



Example R/C Values
(All Resistors and Capacitors are ± 5%)

(CTC' = CTC + 20 pF)

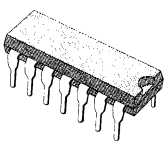
f_{osc}(kHz)	RTC	CTC'	RS	R1	C1	R2	C2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

SGS-THOMSON MICROELECTRONICS

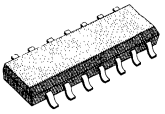
MC1488

RS232C QUAD LINE DRIVER

- CURRENT LIMITED OUTPUT ± 10 mA TYP.
- POWER-OFF SOURCE IMPEDANCE 300 ΩMIN.
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE TTL AND μP COMPATIBLE



DIP-14 (0.25)
(Plastic and Ceramic)



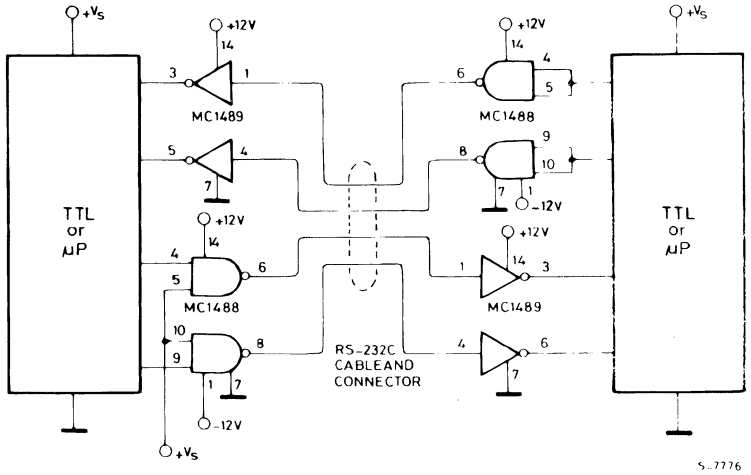
SO-14J

ORDER CODES : MC1488P (Plastic DIP)
MC1488L (Ceramic DIP)
MC1488D (SO-14)

DESCRIPTION

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C.

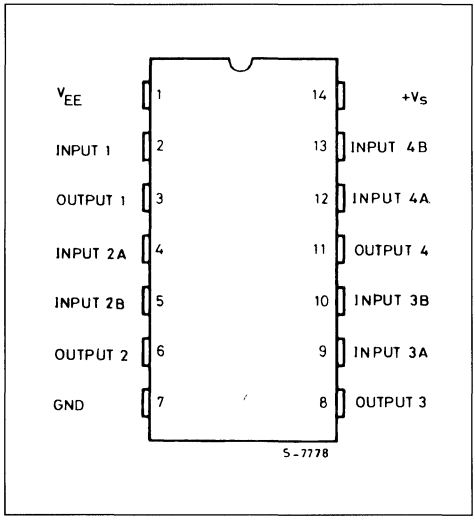
TYPICAL APPLICATION : RS232C Data Transmission.



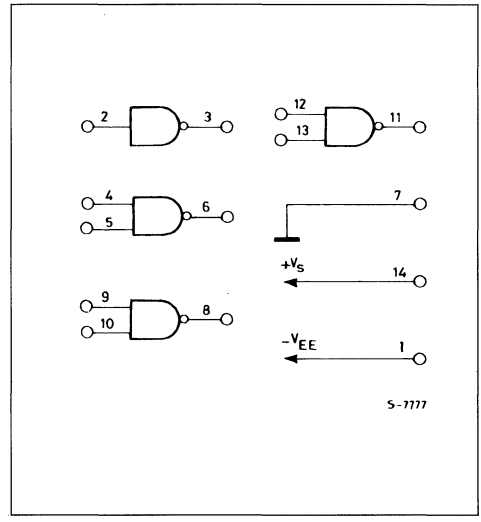
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	15	V
V_{EE}	Power Supply Voltage	− 15	V
V_{IR}	Input Voltage Range	$-15 \leq V_{IR} \leq 7$	V
V_O	Output Signal Voltage	± 15	V
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	− 65 to 150	°C

CONNECTION DIAGRAMS (top views)



LOGIC DIAGRAM



THERMAL DATA

			Plastic DIP - 14	Ceramic DIP - 14	SO - 14
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	200 °C/W	165 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (V_S = 9 ±10 % V, V_{EE} = − 9 ±10 % V, T_{amb} = 0 to 75 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{IL}	Input Current	Low Logic State (V_{IL} = 0V)		1	1.6	mA	1
I_{IH}	Input Current	High Logic State (V_{IH} = 5V)			10	µA	1
V_{OH}	Output Voltage	High Logic State R_L = 3KΩ V_{IL} = 0.8V, V_S = 9V, V_{EE} = −9V V_{IL} = 0.8V, V_S = 13.2V, V_{EE} = −13.2V	 6 9	 7 10.5		 V V	 2 2
V_{OL}	Output Voltage	Low Logic State R_L = 3 KΩ V_{IH} = 1.9V, V_{EE} = −9V, V_S = 9V V_{IH} = 1.9V, V_{EE} = −13.2V, V_S = 13.2V	 − 6 − 9	 − 7 − 10.5		 V V	 2 2
I_{OS+} *	Positive Output Short - circuit Current		6	10	12	mA	3
I_{OS-} *	Negative Output Short-circuit Current		− 6	− 10	− 12	mA	3
R_O	Output Resistance	$V_S = V_{EE}$ = 0 |Vo| = ± 2V	300			Ω	4
I_S	Positive Supply Current (R_i = ∞)	V_{IH} = 1.9 V V_S = 9 V V_{IL} = 0.8 V V_S = 9 V V_{IH} = 1.9 V V_S = 12 V V_{IL} = 0.8 V V_S = 12 V V_{IH} = 1.9 V V_S = 15 V V_{IL} = 0.8 V V_S = 15 V		15 4.5 19 5.5	20 6 25 7 34 12	mA	5
I_{EE}	Negative Supply Current (R_L = ∞)	V_{IH} = 1.9 V V_{EE} = − 9 V V_{IL} = 0.8 V V_{EE} = − 9 V V_{IH} = 1.9 V V_{EE} = − 12 V V_{IL} = 0.8 V V_{EE} = − 12 V V_{IH} = 1.9 V V_{EE} = − 15 V V_{IL} = 0.8 V V_{EE} = − 15 V		− 13 − 18 	− 17 − 15 − 23 − 15 − 34 − 2.5	mA µA mA µA mA mA	5
P_c	Power Consumption	V_S = 9 V V_{EE} = − 9 V V_S = 12 V V_{EE} = − 12 V			333 567	mW	

SWITCHING CHARACTERISTICS (V_S = ± 9 ±1 % V, V_{EE} = − 9 ± 1 % V, T_{amb} = 25 °C)

t_{PLH}	Propagation Delay Time	Z_i = 3 KΩ and 15 pF		275	350	ns	6
t_{THL}	Fall Time	Z_i = 3 KΩ and 15 pF		45	75	ns	6
t_{PHL}	Propagation Delay Time	Z_i = 3 KΩ and 15 pF		110	175	ns	6
t_{TLH}	Rise Time	Z_i = 3 KΩ and 15 pF		55	100	ns	6

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously

TEST CIRCUITS

Figure 1 : Input Current.

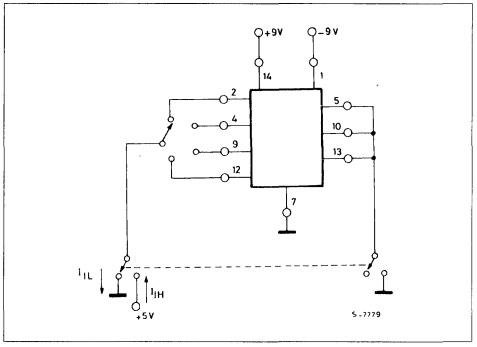


Figure 2 : Output Voltage.

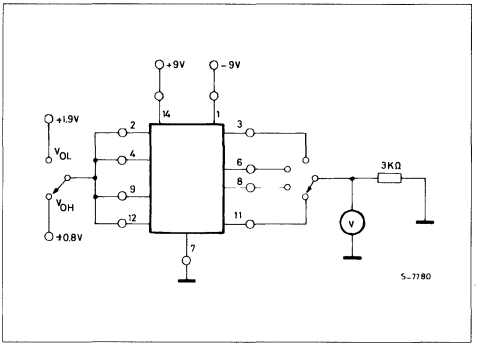


Figure 3 : Output Short-Circuit Current.

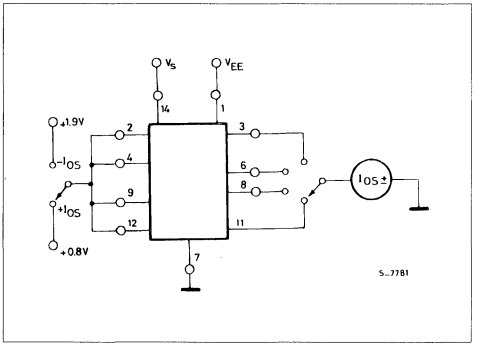


Figure 4 : Output Resistance (power off).

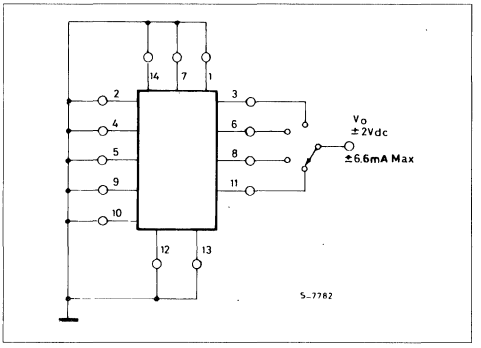


Figure 5 : Power Supply Currents.

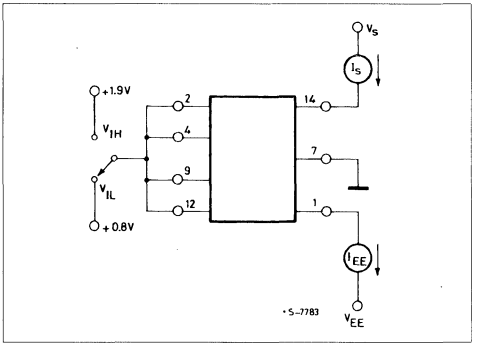


Figure 6 : Switching Response.

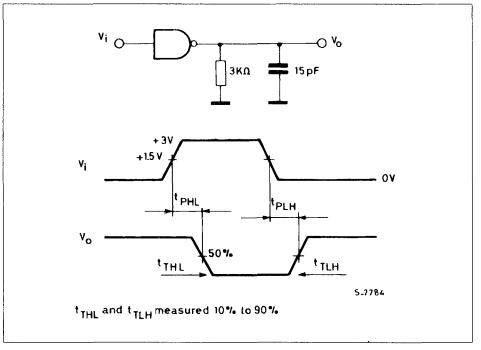


Figure 7 : Transfer Characteristics vs. Power Supply Voltage.

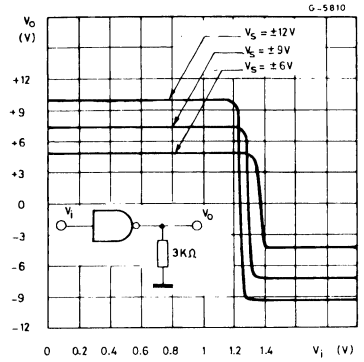


Figure 8 : Short-Circuit Output Current vs. Temperature.

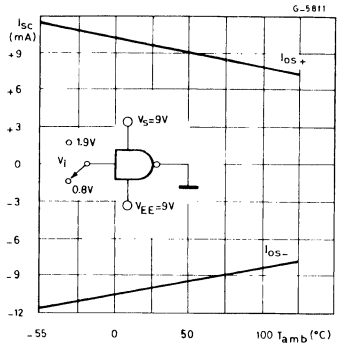


Figure 9 : Output Slew-Rate Load Capacitance.

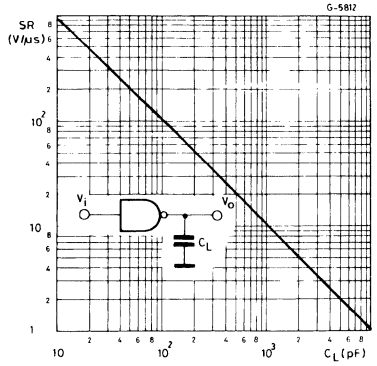


Figure 10 : Output Voltage and Current-Limiting Characteristics.

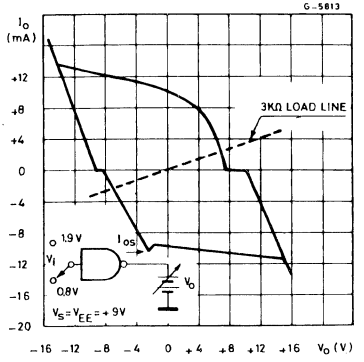
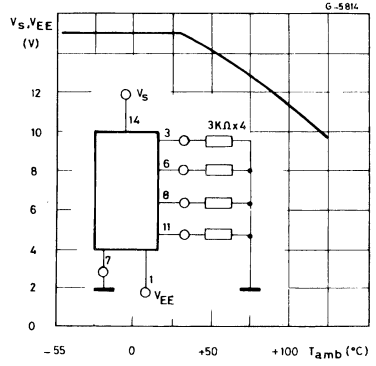


Figure 11 : Maximum Operating Temperature vs. Power-Supply Voltage.



APPLICATION INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15 V in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 V per µs. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T / \Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per µs.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 V, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 V (i.e., $V_S \geq 9.0$ V ; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300Ω output resistor to ground. If **all four outputs** were then shorted to plus or minus 15 V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-suppies of the drivers, a diode should be placed in each power-supply lead to prevent over-heating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±15 V limits specified in the earlier Standard RS232B). The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 V stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Figure 12 : Slew Rate vs. Capacitance for I_{SC} = 10mA.

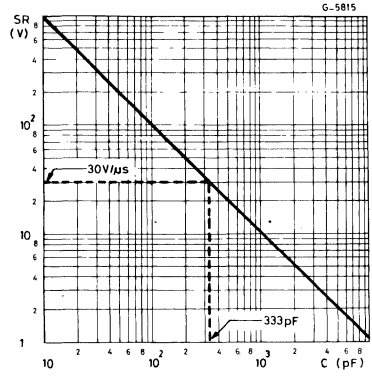
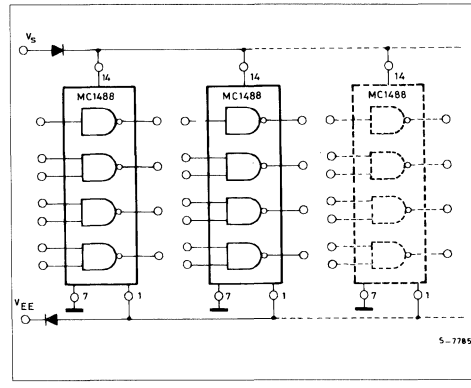


Figure 13 : Power Supply Protection to Meet Power-off Fault Conditions.



OTHER APPLICATION

The MC1488 is an extremely versatile line driver with a miriad of possible applications. Several features of the drivers enhance this versatility :

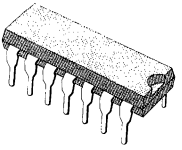
1. Output Current Limiting - this enables the circuit designer to define the ouptut voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins.

2. Power-Supply Range - as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can very from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately - 2.5 V to the minimum specified - 15 V. The MC1488 will drive the ouptut to within 2 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package.

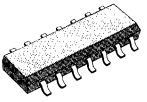
MC1489
MC1489A

QUAD LINE RECEIVERS

- INPUT RESISTANCE –3.0 K to 7.0 KΩ
- INPUT SIGNAL RANGE – ± 30 V
- INPUT THRESHOLD HYSTERESIS BUILT-IN
- RESPONSE CONTROL :
  a) LOGIC THRESHOLD SHIFTING
  b) INPUT NOISE FILTERING



DIP-14
(Plastic (0.25) and Ceramic)



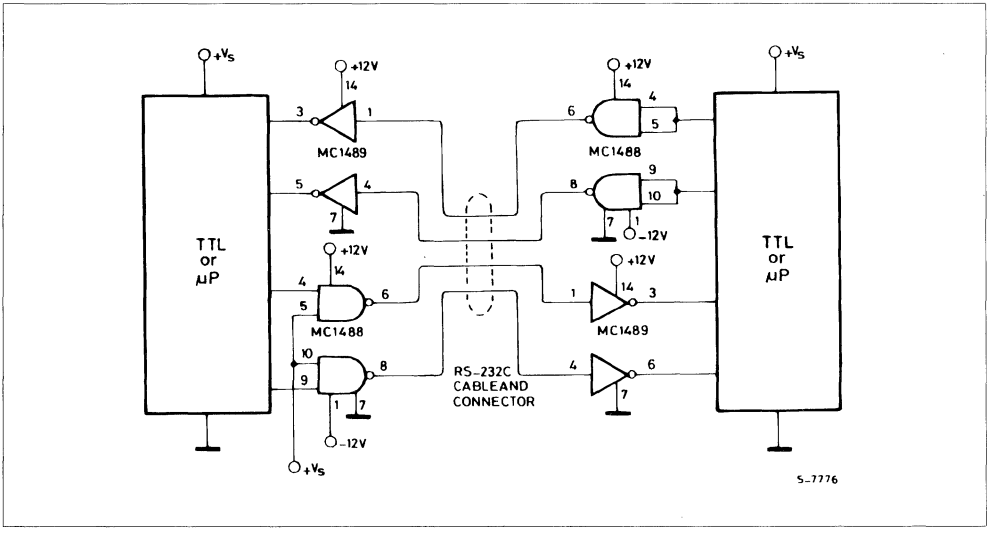
SO-14J

ORDER CODES : MC1489L, MC1489AL
(DIP–14 Ceramic)
MC1489P, MC1489AP
(DIP–14 Plastic)
MC1489D, MC1489AD (SO-14)

DESCRIPTION

The MC1489 monolithic quad line receivers are designed to interface data therminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

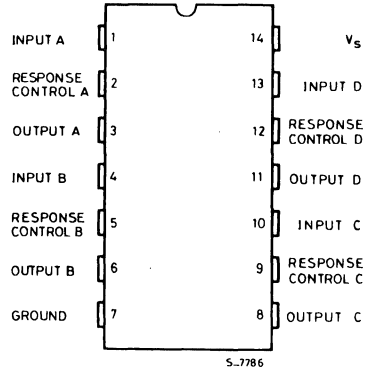
TYPICAL APPLICATION : RS232C Data Transmission



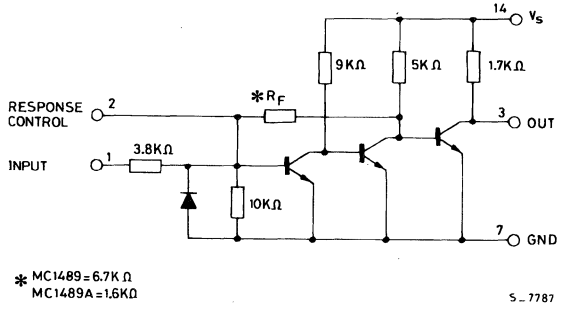
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply Voltage	10	V
V_I	Input Voltage Range	± 30	V
I_{OL}	Output Load Current	20	mA
P_{tot}	Power Dissipation	1	W
T_{amb}	Operating Ambient Temperature	0 to 75	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

CONNECTION DIAGRAMS (top view)



SCHEMATIC DIAGRAM (1/4 of circuit shown)



ELECTRICAL CHARACTERISTICS (Response control pin is open ; V_S = 5 V, T_{amb} = 0 to 75 °C unless otherwise specified)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
I_{IH}	Positive Input Current	V_{IH} = 25 V V_{IH} = 3 V	3.6 0.43		8.3	mA
I_{IL}	Negative Input Current	V_{IL} = - 25 V V_{IL} = - 3 V	- 3.6 - 0.43		- 8.3	mA
V_{IH}	Input Turn-on Threshold Voltage	T_{amb} = 25 °C $V_{OL} \leq$ 0.45 I_L = 10 mA for **MC1489** for **MC1489A**	1 1.75	1.95	1.5 2.25	V
V_{IL}	Input Turn-off Threshold Voltage	T_{amb} = 25 °C $V_{OH} \geq$ 2.5 V I_L = - 0.5 mA	0.75		1.25	V
V_{OH}	Ouptut Voltage High	V_{IH} = 0.75 V I_L = - 0.5 mA I_L = 0.5 mA Input Open Circuit	2.5 2.5	4 4	5 5	V V
V_{OL}	Output Voltage Low	V_{IL} = 3 V I_L = 10 mA		0.2	0.45	V
I_{OS}	Output Short Circuit Current			- 3	- 4	mA
I_S	Power Supply Current	All gates "on" I_O = 0 mA V_{IH} = 5 V		16	26	mA
P_C	Power Consumption	V_{IH} = 5 V		80	130	mW

SWITCHING CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 °C, see Fig. 1)

Symbol	Parameter	Test Condtions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay Time	R_L = 3.9 KΩ		25	85	ns
t_{TLH}	Rise Time	R_L = 3.9 KΩ		120	175	ns
t_{PHL}	Propagation Delay Time	R_L = 390 Ω		25	50	ns
t_{THL}	Fall Time	R_L = 390 Ω		10	20	ns

TEST CIRCUITS

Figure 1 : Switching Response.

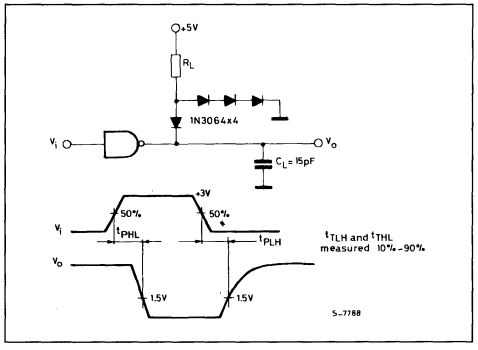
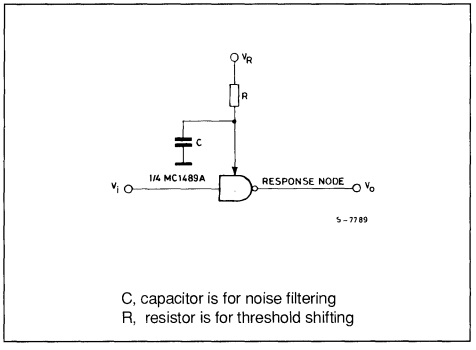


Figure 2 : Response Control Node.



C, capacitor is for noise filtering
R, resistor is for threshold shifting

Figure 3 : Input Current.

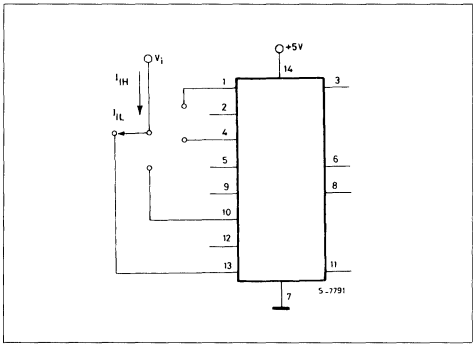


Figure 4 : Output Short-Circuit Current.

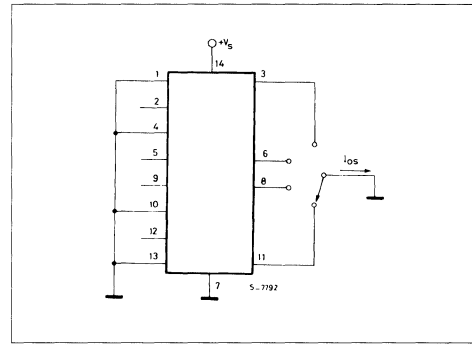


Figure 5 : Output Voltage and Input Threshold Voltage.

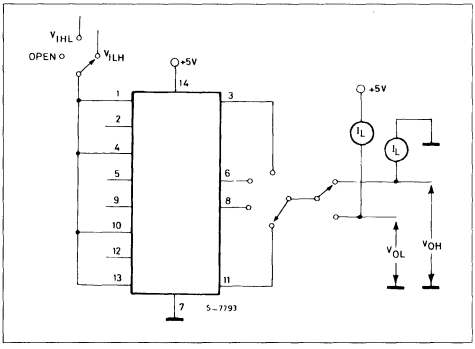
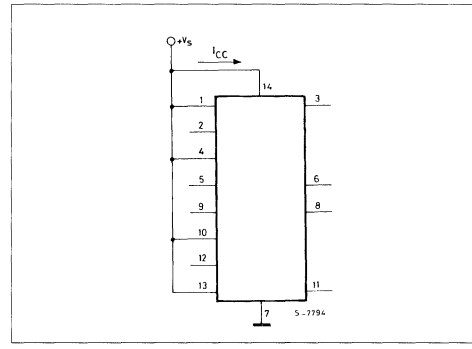


Figure 6 : Power Supply Current.



TYPICAL CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 °C unless otherwise specified)

Figure 7 : Input Current.

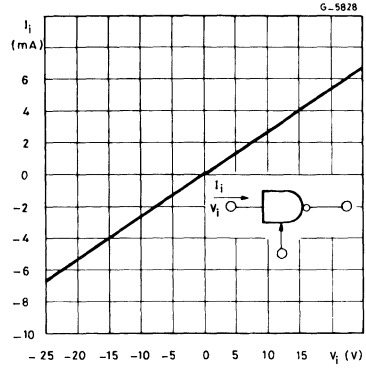


Figure 8 : MC1489 Input Threshold Voltage Adjustament.

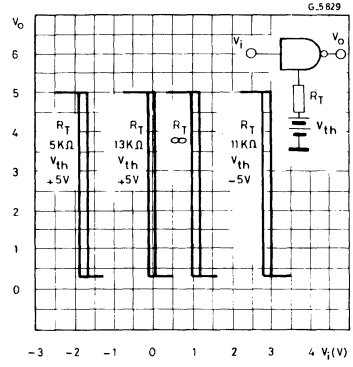


Figure 9 : MC1489A Input Threshold Voltage Adjustment.

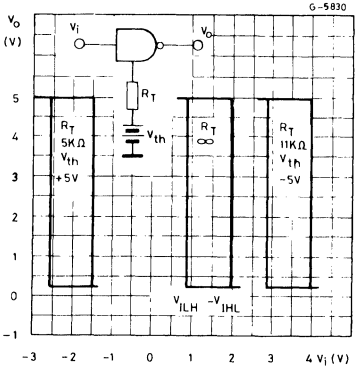


Figure 10 : Input Threshold Voltage vs. Temperature.

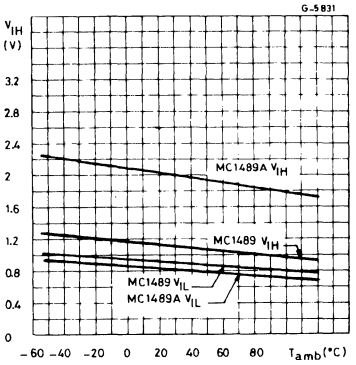
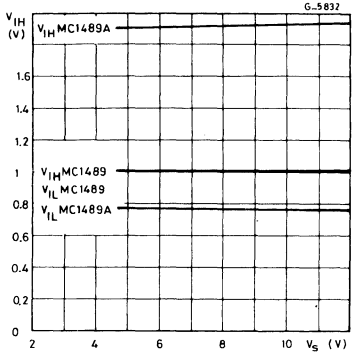


Figure 11 : Input Threshold vs. Power-Supply Voltage.



APPLICATION INFORMATION

GENERAL INFORMATION

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude ; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between - 3.0 and - 25 V as a Logic "1" and inputs between + 3.0 and + 2.5 V as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300 Ω or more to ground) shall be decoded as an "OFF" condition or Logic "1". For the reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

DEVICE CHARACTERISTICS

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and and an external power supply. Figure 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of the high-frequency, high-energy noise pulses. Figure 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for may combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted. (with the appropiate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Figure 12 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

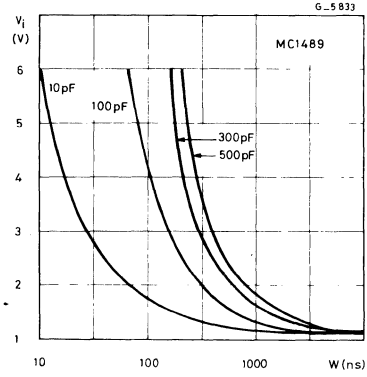


Figure 13 : Typical Turn-on Threshold vs. Capacitance from Response Control Pin to GND.

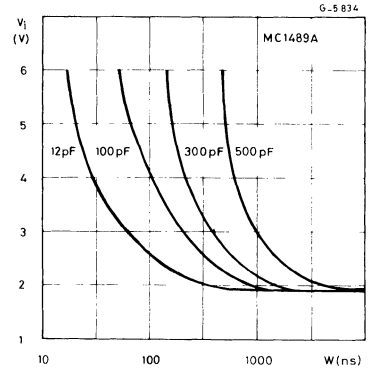
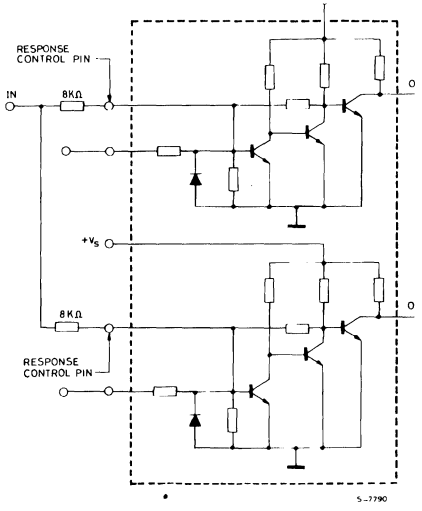
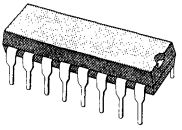


Figure 14: Typical Paralleling of Two MC1489/A Receivers to Meet RS-232C.



STEPPER MOTOR DRIVER

- SINGLE SUPPLY OPERATION + 7.2 V TO + 16 V
- 350 mA/ COIL DRIVE CAPABILITY
- BUILT IN FAST PROTECTION DIODES
- SELECTABLE $\overline{CW}$/CCW AND $\overline{FULL}$/HALF STEP OPERATION
- SELECTABLE HIGH/LOW OUTPUT IMPEDANCE (HALF STEP MODE)
- TTL/CMOS COMPATIBLE INPUTS
- INPUT HYSTERESIS : 250 mV TYP.
- $\overline{PHASE}$ LOGIC CAN BE INITIALIZED TO $\overline{PHASE\ A}$
- $\overline{PHASE\ A}$ OUTPUT DRIVE STATE INDICATION



Powerdip
12 + 2 + 2

ORDER CODE : MC3479C

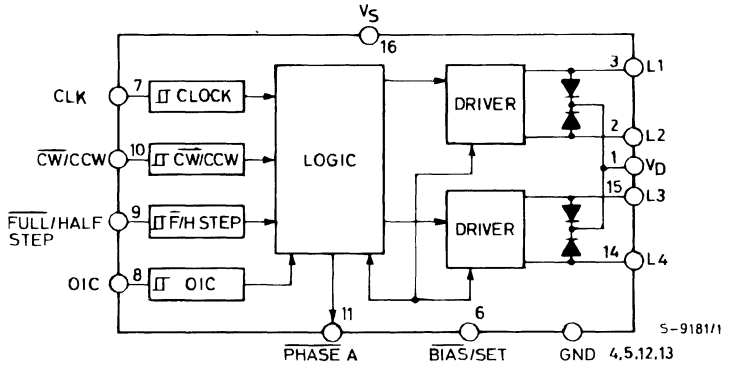
DESCRIPTION

The MC3479C is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input selections a logic decoding/sequencing section two driver stages for the motor coils and an output to indicate the Phase A drive state.

INPUT TRUTH TABLE

	INPUT LOW	INPUT HIGH
CW/CCW	CW	CCW
F/HS	Full Step	Half Step
OIC	High Z	Low Z
CLK	Positive Edge Triggered	

BLOCK DIAGRAM



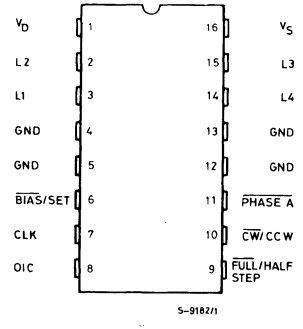
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	16	V_{DC}
V_D	Clamp Diode Cathode Voltage (pin 1)	V_S	V_{DC}
V_{OD}	Driver Output Voltage (pins 2, 3, 14, 15)	V_S	V_{DC}
I_{OD-}	Driver Output Current/Coil	± 500	mA
V_{IN}	Input Voltage (pins 7, 8, 9, 10)	– 0.5 to 7	V_{DC}
I_{BS}	$\overline{\text{Bias/Set}}$ Current (pin 6)	10	mA
V_{OA}	$\overline{\text{Phase A}}$ Output Voltage (pin 11)	16	V_{DC}
I_{OA}	$\overline{\text{Phase A}}$ Sink Current (pin 11)	20	mA
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature range	– 55 to 150	°C

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply Voltage (DC)	7.2	16	V
V_D	Clamp Diode Cathode Voltage (DC)	–	V_S	V
I_{OD}	Driver Output Current (per coil)	–	350	mA
V_I	DC Input Voltage (pin 7, 8, 9, 10)	0	5.5	V
I_{BS}	$\overline{\text{Bias/Set}}$ Current (outputs active)	– 300	75	µA
I_{OA}	$\overline{\text{Phase A}}$ Sink Current	0	8	mA
T_{amb}	Operating Ambient Temperature	0	70	°C

CONNECTION DIAGRAMS



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

PIN DESCRIPTION

Symbol	Name	Pins	Description
V_S	POWER SUPPLY	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is 7.2 V to 16 V.
GND	GROUND	4-5-12-13	Ground Pins for the Logic Circuit and the Motor Coil Current. The physical configuration of the pins dissipating heat from within the package.
V_D	CLAMP DIODE	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and pin 16. See figure 5.
L1, L2, L3, L4	DRIVER OUTPUTS	2-3 14-15	High Current Outputs for the Motor Coils. L1 and L2 are connected to one coil and L3 and L4 to the other coil.
$\overline{B}$/S	$\overline{BIAS}$/SET	6	This pins is typically 0.7 V below V_S. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0 µA) the outputs assume a high impedance condition while the internal logic presets to a Phase A condition.
CK	CLOCK	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if pin 6 is open.
$\overline{F}$/HS	$\overline{FULL}$/HALF STEP	9	When low (logic 0) each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. (see figure 4 for sequence).
$\overline{CW}$/CCW	$\overline{CLOCKWISE}$ COUNTERCLOCKWISE	10	This input allows reversing the rotation of the rotation of the motor. (see figure 4 for sequence).
OIC	OUT IMPEDANCE CONTROL	8	This input is relevant only in the half step mode (pin 9 > 2 V). When low (logic 0) the two driver out of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance reference to V_S. (see figure 4).
$\overline{Ph\ A}$	$\overline{PHASE\ A}$	11	This outputs indicate (when low) that the driver outputs are in the phase A condition (L1 = L3 = V_{OHD} ; L2 = L4 = V_{OLD}).

DC ELECTRICAL CHARACTERISTICS(Specifications apply over the recommended supply voltage and temperature range, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT LOGIC LEVEL						
V_{TLH}	Threshold Voltage (low to high)				2	V
V_{THL}	Threshold Voltage (high to low)		0.8			V
V_{HYS}	Hysteresis		0.4			V
I_{IL} I_{IH1} I_{IH2}	Current	V_I = 0.4 V V_I = 5.5 V V_I = 2.7 V	– 100		 100 20	 µA
DRIVER OUTPUT LEVELS						
V_{OHD}	Output High Voltage	I_{OD} = – 350 mA I_{OD} = – 0.1 mA I_{BS} = – 300 µA	V_S – 2.0 V_S – 1.2			V V
V_{OLD}	Output Low Voltage	I_{BS} = – 300 µA I_{OD} = – 350 mA			0.8	V
D_{VOD}	Difference Mode out Voltage Difference	I_{BS} = – 300 µA I_{OD} = 350 mA			0.15	V
C_{VOD}	Common Mode out Voltage Difference	I_{BS} = – 300 µA I_{OD} = – 0.1 mA			0.15	V
I_{OZ1}	Out Leakage-HiZ State	0 < V_D < V_M, I_{BS} = 5 µA	– 100		+ 100	µA
I_{OZ2}	Out Leakage-HiZ state	0 < V_{OD} < V_M, I_{BS} = – 300 µA Pin 9 = 2 V Pin 8 = 0.8 V	– 100		+ 100	µA
CLAMP DIODES						
V_{DF}	Forward Voltage	I_D = 350 mA		2.5	3	V
I_{DR}	Leakage Current	V_R = 21 V			100	µA
PHASE A OUTPUT						
V_{OLA}	Out Low Voltage	I_{OA} = 8 mA			0.4	V
	Off State Leakage Current	V_{OA} = 16.5 V			100	µA
POWER SUPPLY						
I_{SSB}	Power Supply Current in Stand by State	V_{BS} = V_S			12	mA
I_S	Power Supply Current (I_{OD} = 0) ; I_{BS} = – 300 µA)	L1 = V_{OHD} L2 = V_{OLD} L3 = V_{OHD} L4 = V_{OHD}			75	mA

BIAS SET CURRENT

I_{BS}	Bias Set Current	to set $\overline{\text{PHASE A}}$	– 5			µA

Notes : 3. DVOD = | VOD1.2 - VOD3.4 |
VOD1.2 = (VOHD1 - VOHD2) or (VOHD2 - VOLD1) AND VOD3.4 = (VOHD3 - VOHD4) OR (VOHD4 - VOHD3)
4. CVOD = | VOHD1 - VOHD2 or VOHD3 - VOHD4 |

AC SWITCHING CHARACTERISTICS (T_{amb} = 25 °C ; V_M = 12 V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CK}	Clock Frequency		0		30	KHz
PWCKH	Clock Pulse Width	HIGH	10			µs
PWCKL	Clock Pulse Width	LOW	20			µs
t_{SU}	Set-up Time $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS		5			µs
t_{HO}	Hold Time $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS		10			µs
t_{PCD}	Propagation Delay CLK-to Driver Out			8		µs
t_{PBSD}	Propagation Delay $\overline{\text{Bias}}$/Set to Driver Output			1		µs
t_{PHLA}	Propagation Delay CLK-to Phase A LOW			12		µs
t_{PLHA}	Propagation Delay CLK-to Phase A HIGH			5		µs

Figure 1: AC Test Circuit.

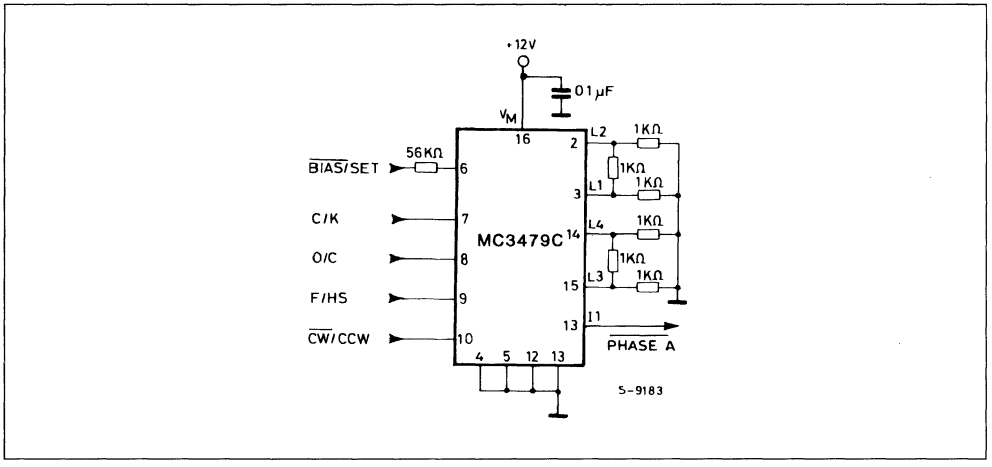


Figure 2 : Typical Application Circuit.

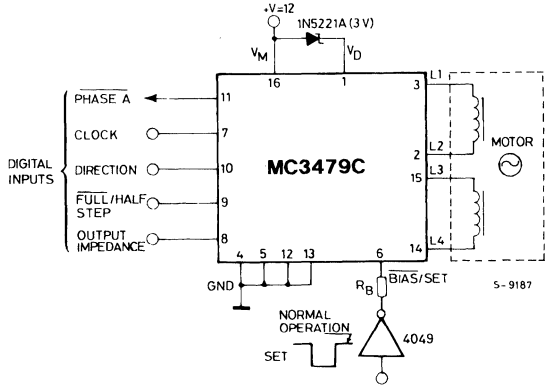


Figure 3 : Bias/Set Timing (refer to fig.1).

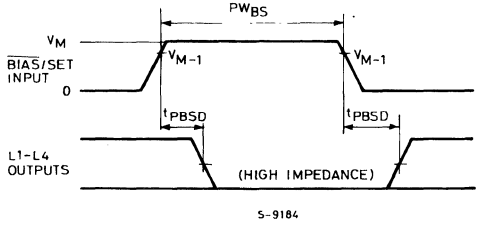


Figure 4 : Clock Timing (refer to fig.1).

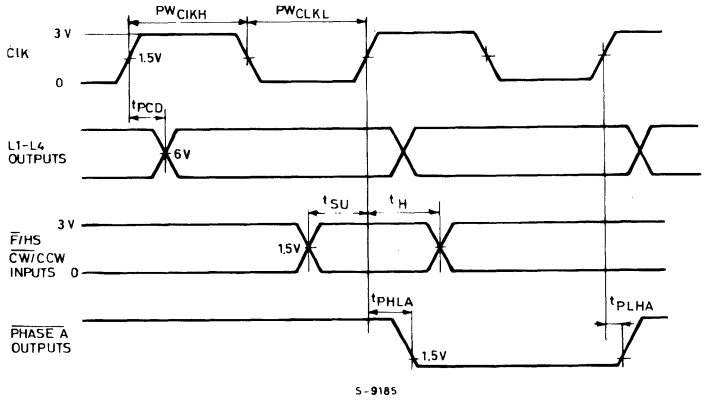
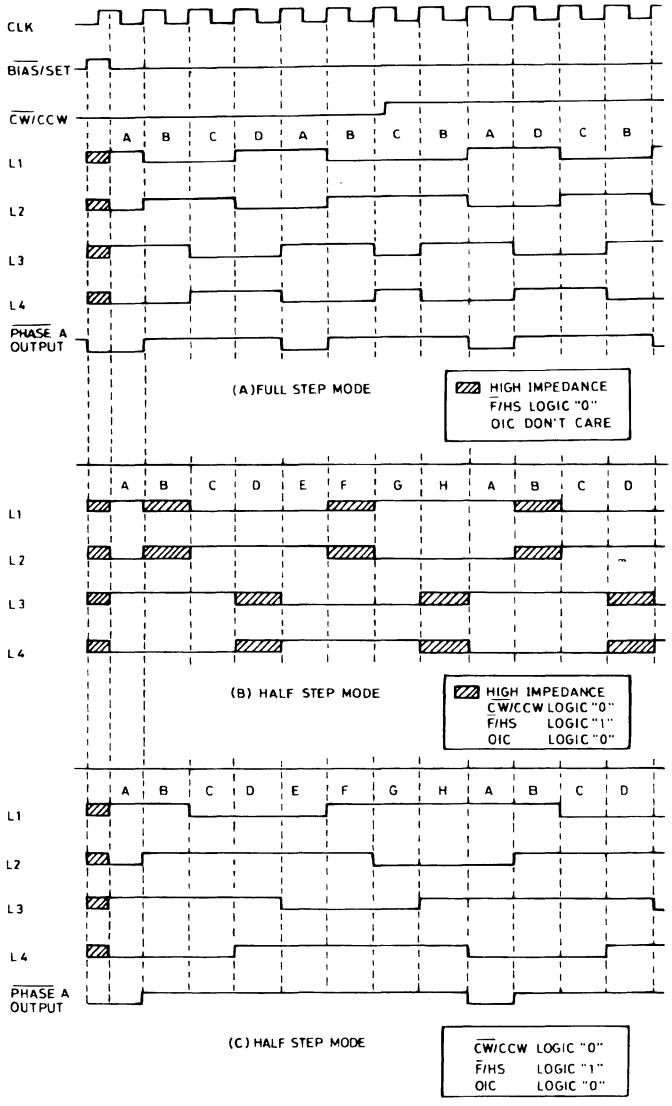


Figure 5 : Output Sequence.



SGS-THOMSON MICROELECTRONICS

PBL3717A

STEPPER MOTOR DRIVER

- FULL STEP - HALF STEP - QUARTER STEP OPERATING MODE
- BIPOLAR OUTPUT CURRENT UP TO 1 A
- FROM 10 V UP TO 46 V MOTOR SUPPLY VOLTAGE
- LOW SATURATION VOLTAGE WITH INTEGRATED BOOTSTRAP
- BUILT IN FAST PROTECTION DIODES
- EXTERNALLY SELECTABLE CURRENT LEVEL
- OUTPUT CURRENT LEVEL DIGITALLY OR ANALOGUE CONTROLLED
- THERMAL PROTECTION WITH SOFT INTERVENTION

DESCRIPTION

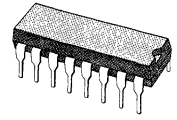
The PBL3717A is a monolithic IC which controls and drives one phase of a bipolar stepper motor with chopper control of the phase current. Current levels may be selected in three steps by means of two logic inputs which select one of three current comparators. When both of these inputs are high the device is disabled. A separate logic input controls the direction of current flow.

A monostable, programmed by an external RC network, sets the current decay time.

The power section is a full H-bridge driver with four internal clamp diodes for current recirculation. An external connection to the lower emitters is available for the insertion of a sensing resistor. Two PBL3717As and few external components form a complete stepper motor drive subsystem.

The raccomended operating ambient temperature ranges is from 0 to 70 °C.

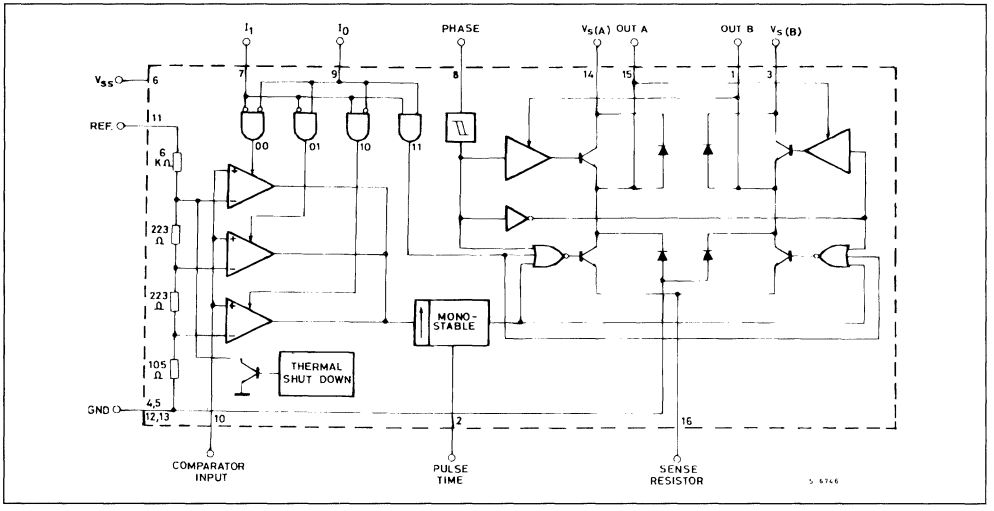
The PBL3717A is supplied in a 12 + 2 + 2 lead Powerdip package.



Powerdip 12 + 2 + 2

ORDER CODE : PBL3717A

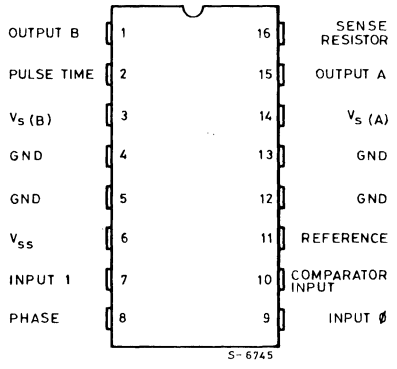
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Power Supply Voltage (pins 14, 3)	50	V
V_{ss}	Logic Supply Voltage (pin 6)	7	V
V_i	Logic Input Voltage (pins 7, 8, 9)	6	V
V_c	Comparator Input (pin 10)	V_{ss}	
V_r	Reference Input Voltage (pin 11)	15	V
I_o	Output Current (DC operation)	1.2	A
T_{stg}	Storage Temperature	– 55 to + 150	°C
T_j	Operating Junction Temperature	150	°C

CONNECTION DIAGRAM (top view)



TRUTH TABLE

Input 0 (pin 9)	Input 1 (pin 7)	
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	High Current

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	11	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient*	40	°C/W

* Soldered on a 35µ thick 20 cm^2 P.C. board copper area.

PIN FUNCTIONS

N°	Name	Function
1	OUTPUT B	Output Connection (with pin 15). The output stage is a "H" bridge formed by four transistors and four diodes suitable for switching applications.
2	PULSE TIME	A parallel RC network connected to this pin sets the OFF time of the lower power transistors. The pulse generator is a monostable triggered by the rising edge of the output of the comparators ($t_{off} = 0.69\ R_T\ C_T$).
3	SUPPLY VOLTAGE B	Supply Voltage Input for Half Output Stage. See also pin 14.
4	GROUND	Ground Connection. With pins 5, 12 and 13 also conducts heat from die to printed circuit copper.
5	GROUND	See pin 4.
6	LOGIC SUPPLY	Supply Voltage Input for Logic Circuitry.
7	INPUT 1	This pin and pin 9 (INPUT 0) are logic inputs which select the outputs of the three comparators to set the current level. Current also depends on the sensing resistor and reference voltage. See truth table.
8	PHASE	This TTL-compatible logic input sets the direction of current flow through the load. A high level causes current to flow from OUTPUT A (source) to OUTPUT B (sink). A schmitt trigger on this input provides good noise immunity and a delay circuit prevents output stage short circuits during switching.
9	INPUT 0	See INPUT 1 (pin 7) .
10	COMPARATOR INPUT	Input connected to the three comparators. The voltage across the sense resistor is feedback to this input through the low pass filter $R_C\ C_C$. The lower power transistor are disabled when the sense voltage exceeds the reference voltage of the selected comparator. When this occurs the current decays for a time set by $R_T\ C_T$, $t_{off} = 0.69\ R_T\ C_T$.
11	REFERENCE	A voltage applied to this pin sets the reference voltage of the three comparators, this determining the output current (also thus depending on R_s and the two inputs INPUT 0 and INPUT 1).
12	GROUND	See pin 4.
13	GROUND	See pin 4.
14	SUPPLY VOLTAGE A	Supply Voltage Input for Half Output Stage. See also pin 13.
15	OUTPUT A	See pin 1.
16	SENSE RESISTOR	Connection to Lower Emitters of Output Stage for Insertion of Current Sense Resistor.

Figure 1 : Test and Application Circuit.

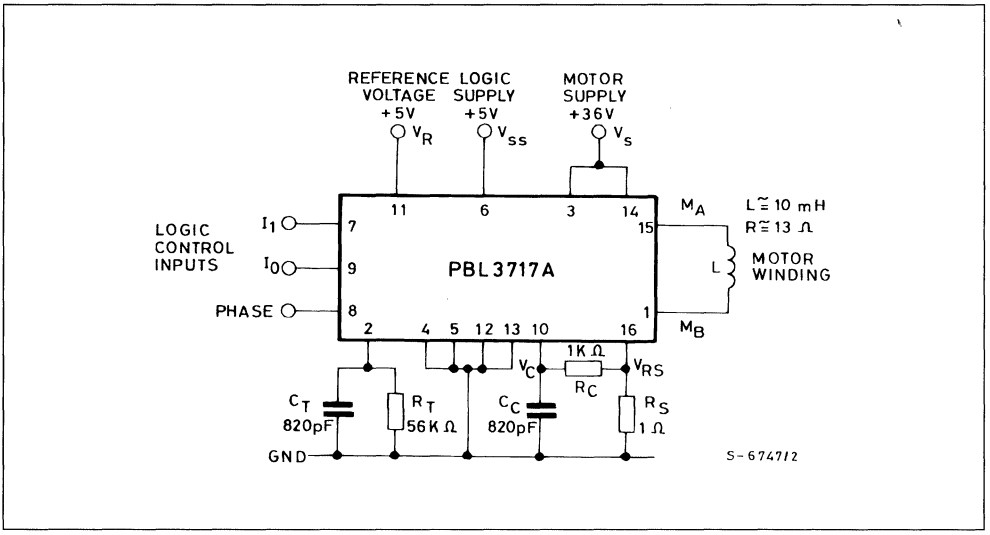
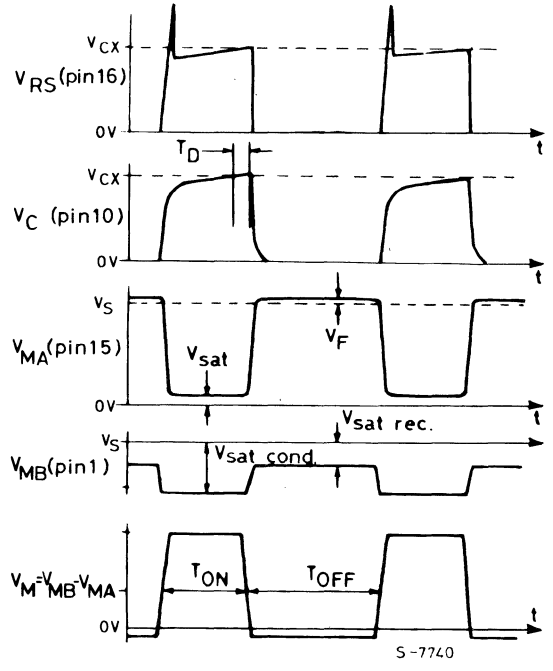


Figure 2 : Waveforms with MA Regulating (phase = 0).



ELECTRICAL CHARACTERISTICS (refer to the test circuit V_s = 36 V, V_{ss} = 5 V, Tamb = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_s	Supply Voltage (pin 3, 14)			10		46	V
V_{ss}	Logic Supply Voltage (pin 6)			4.75		5.25	V
I_{ss}	Logic Supply Current (pin 6)				7	15	mA
I_R	Reference Input Current (pin 11)	V_R = 5 V			0.75	1	mA

LOGIC INPUTS

V_{iL}	Input Low Voltage (pins 7, 8, 9)					0.8	V
V_{iH}	Input High Voltage (pin 7, 8, 9)			2		V_{ss}	V
I_{iL}	Low Voltage Input Current (pins 7, 8, 9)	V_i = 0.4 V	pin 8			− 100	µA
			pins 7, 9			− 400	µA
I_{iH}	High Voltage Input Current (pins 7, 8, 9)	V_i = 2.4 V				10	µA

COMPARATORS

V_{CL}	Comparator Low Threshold Voltage (pin 10)	V_R = 5 V	I_o = L I_1 = H	66	78	90	mV
V_{CM}	Comparator Medium Threshold Voltage (pin 10)	V_R = 5 V	I_o = H I_1 = L	236	251	266	mV
V_{CH}	Comparator High Threshold Voltage (pin 10)	V_R = 5 V	I_o = L I_1 = L	396	416	436	mV
I_C	Comparator Input Current (pin 10)					± 20	µA
t_{off}	Cutoff Time	R_T = 56 KΩ	C_T = 820 pF	25		35	µs
t_d	Turn Off Delay	(see fig. 2)				2	µs
I_{off}	Output Leakage Current (pins 1, 15)	I_o = H	I_1 = H			100	µA

SOURCE DIODE-TRANSISTOR PAIR

V_{sat}	Saturation Voltage (pins 1, 15)	I_M = − 0.5 A (see fig. 2)	Conduction Period		1.7	2.1	V
			Recirculation Period		1.1	1.35	
V_{sat}	Saturation Voltage (pins 1, 15)	I_M = − 1 A (see fig. 2)	Conduction Period		2.1	2.8	V
			Recirculation Period		1.7	2.5	
I_{LK}	Leakage Current	V_s = 46 V				300	µA
V_F	Diode Forward Voltage	I_M = − 0.5 A			1	1.25	V
		I_M = − 1 A			1.3	1.7	
I_{SLK}	Substrate Leakage Current when Clamped	I_M = − 0.5 A				2	mA
		I_M = − 1A				5	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

SINK DIODE-TRANSISTOR PAIR

V_{sat}	Saturation Voltage (pins 1, 15)	I_M = 0.5 A		1.1	1.35	V
		I_M = 1 A		1.6	2.3	V
I_{LK}	Leakage Current	V_s = 46 V			300	µA
V_F	Diode Forward Voltage	I_M = 0.5 A		1.1	1.5	V
		I_M = 1 A		1.4	2	

APPLICATION CIRCUIT

Figure 3 : Two Phase Bipolar Stepper Motor Driver.

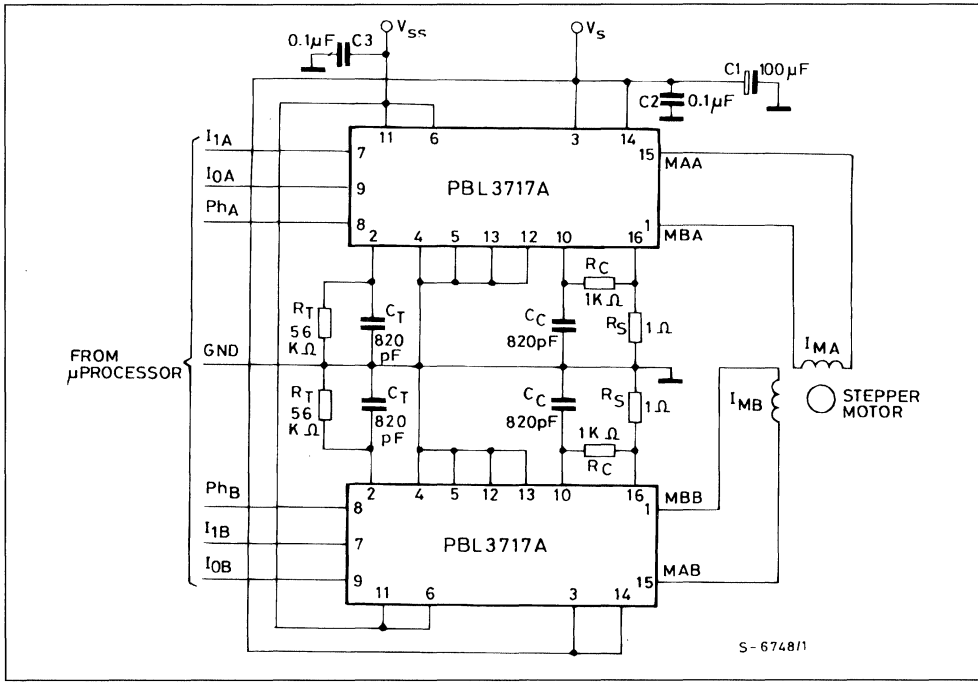


Figure 4 : P.C. Board and Component Layout of the Circuit of fig. 3 (1 : 1 scale).

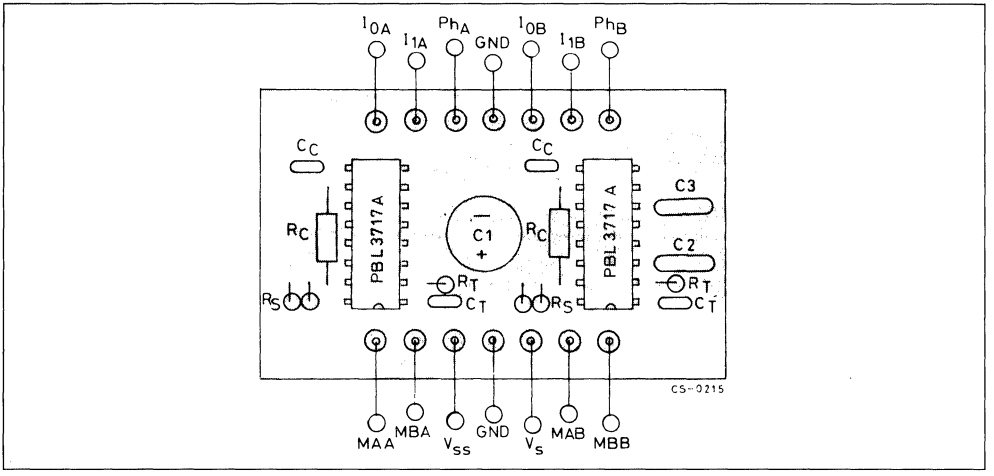
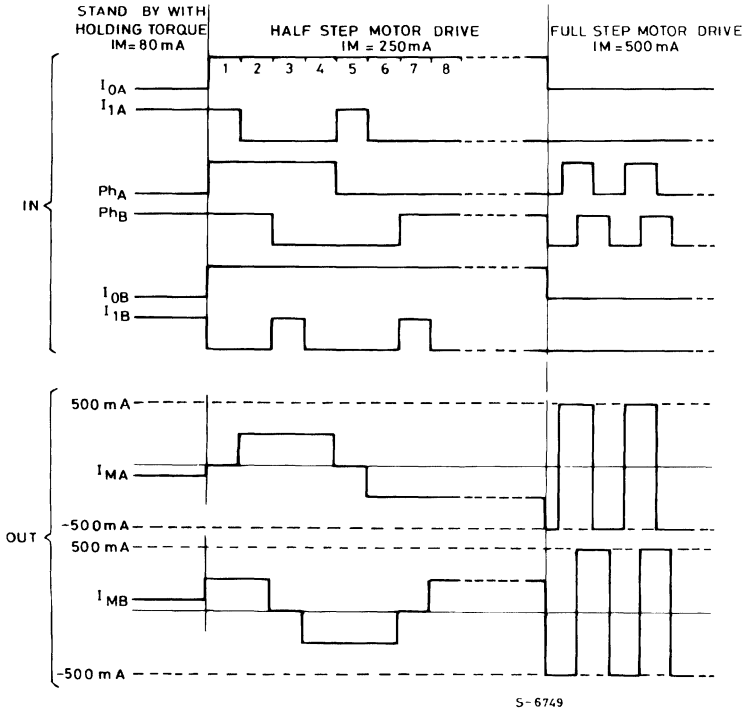


Figure 5 : Input and Output Sequences for Half Step and Full Step Operation.



APPLICATION INFORMATIONS

Fig. 3 shows a typical application in which two PBL3717A control a two phase bipolar stepper motor.

PROGRAMMING

The logic inputs I_0 and I_1 set at three different levels the amplitude of the current flowing in the motor winding according to the truth table of page 2. A high level on the "PHASE" logic input sets the direction of that current from output A to output B ; a low level from output B to output A.

It is recommended that unused inputs are tied to pin 6 (V_{SS}) or pin 4 (GND) as appropriate to avoid noise problem.

The current levels can be varied continuously by changing the ref. voltage on pin 11.

CONTROL OF THE MOTOR

The stepper motor can rotate in either directions according to the sequence of the input signals. It is possible to obtain a full step, a half step and a quarter step operation.

FULL STEP OPERATION

Both the windings of the stepper motor are energized all the time with the same current $I_{MA} = I_{MB}$.

I_0 and I_1 remain fixed at whatever torque value is required.

Calling A the condition with winding A energized in one direction and $\overline{A}$ in the other direction, the sequence for full step rotation is :

$$AB \rightarrow \overline{A}B \rightarrow \overline{A}\,\overline{B} \rightarrow A\overline{B} \text{ etc.}$$

For the rotation in the other direction the sequence must be reserved.

In the full step operation the torque is constant each step.

HALF STEP OPERATION

Power is applied alternately to one winding then both according to the sequence :

$$AB \rightarrow B \rightarrow \overline{A}B \rightarrow \overline{A} \rightarrow \overline{A}\,\overline{B} \rightarrow \overline{B} \rightarrow A\overline{B} \rightarrow A \text{ etc.}$$

Like full step this can be done at any current level ; the torque is not constant but it is lower when only one winding is energized.

A coil is turned off by setting I_0 and I_1 both high.

QUARTER STEP OPERATION

It is preferable to realize the quarter step operation at full power otherwise the steps will be of very irregular size.

The extra quarter steps are added to the half steps sequence by putting one coil on half current according to the sequence.

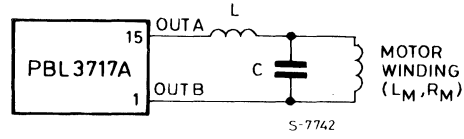
$$AB \rightarrow \frac{A}{2}B \rightarrow B \rightarrow \frac{\overline{A}}{2}B \rightarrow \overline{A}B \rightarrow \overline{A}\frac{B}{2} \rightarrow \overline{A} \text{ etc.}$$

MOTOR SELECTION

As the PBL3717A provides constant current drive, with a switching operation, care must be taken to select stepper motors with low hysteresis losses to prevent motor over heat.

L -C FILTER

To reduce EMI and chopping losses in the motor a low pass L -C filter can be inserted across the outputs of the PBL3717A as shown on the following picture.



$$L \cong \frac{1}{10} LM \qquad C \cong \frac{4 \cdot 10^{-10}}{L}$$

Figure 6 : Source sat. Voltage vs. Output Current (recirc. period).

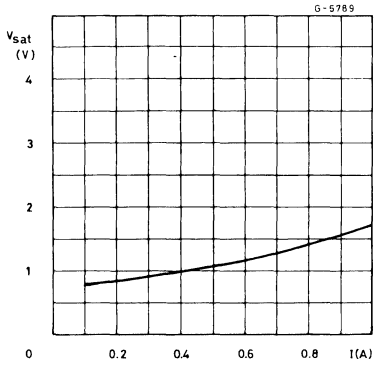


Figure 7 : Source sat. Voltage vs. Output Current (conduction period).

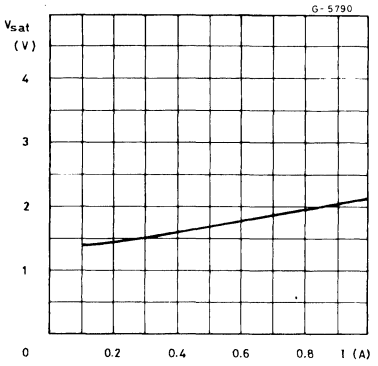


Figure 8 : Sink sat. Voltage vs. Output Current.

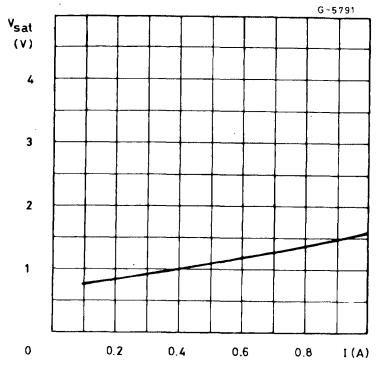
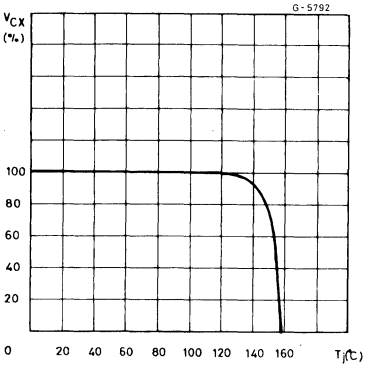


Figure 9 : Comparator threshold vs. Junction Temperature.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the PBL 3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of fig. 11 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thichkness of 35µ (see fig. 10).

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 10 : Example of P.C. Board Copper Area Which is Used as Heatsink.

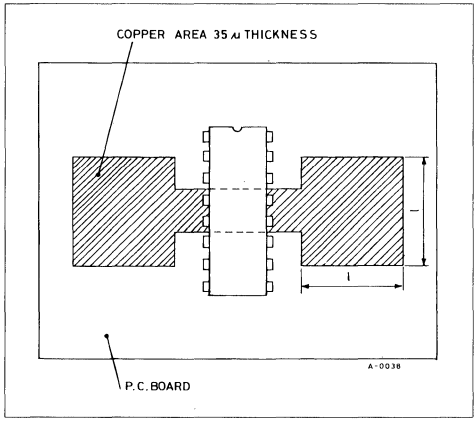
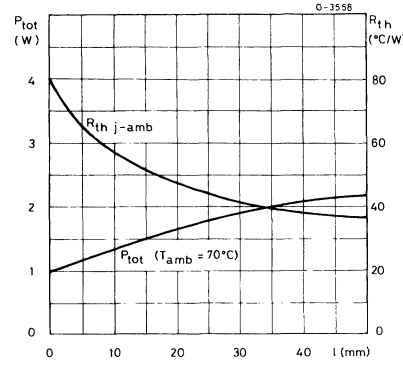


Figure 11 : Max. Dissipable Power and Junction to Ambient Thermal Resistance vs. size "α".

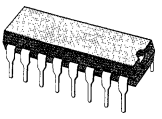


REGULATING PULSE WIDTH MODULATORS

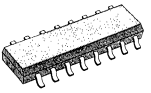
- COMPLETE PWM POWER CONTROL CIRCUITRY
- UNCOMMITTED OUTPUTS FOR SINGLE-ENDED OR PUSH PULL APPLICATIONS
- LOW STANDBY CURRENT .. 8 mA TYPICAL
- OPERATION UP TO 300 KHz
- 1 % MAXIMUM TEMPERATURE VARIATION OF REFERENCE VOLTAGE

DESCRIPTION

The SG1524 , SG2524, and SG3524 incorporate on a single monolithic chip all the function required for the construction of regulating power supplies inverters or switching regulators. They can also be used as the control element for high power-output applications. The SG1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allows either single-ended or push-pull applications. Each device includes an on-ship reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.



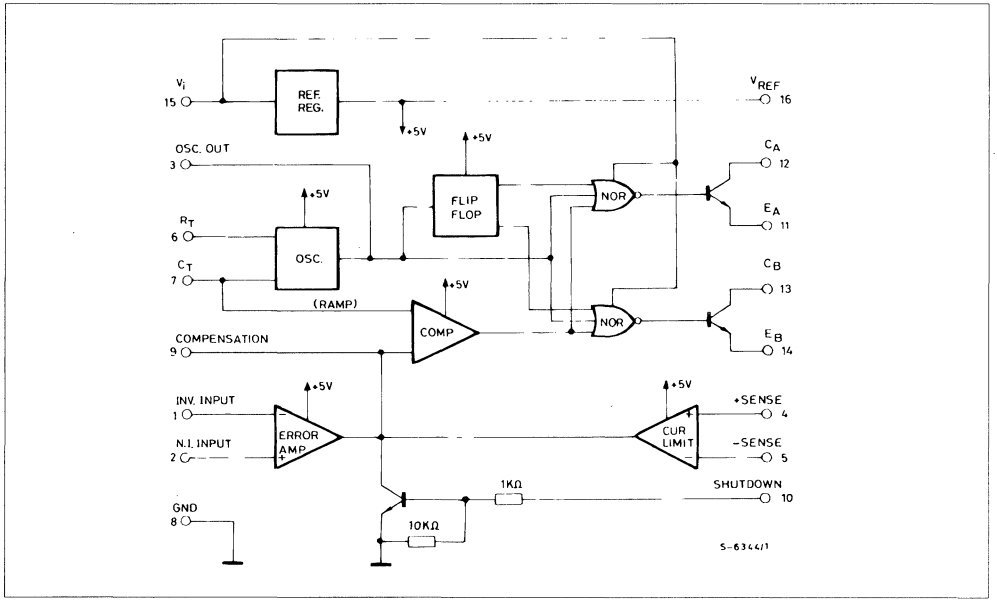
DIP-16
(Plastic –0.25– and Ceramic)



SO16 J

ORDER CODES : SG1524J – SG2524J – SG3524J (Ceramic)
SG2524N – SG3524N (Plastic)
SG2524P – SG3524P (SO–16J)

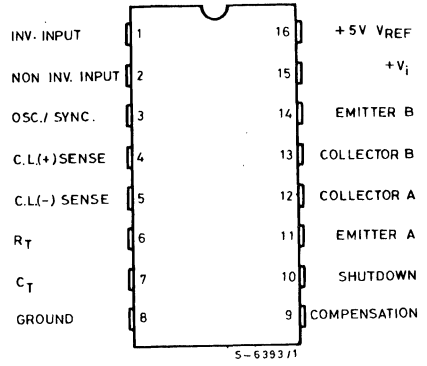
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	Supply Voltage	40	V
I_C	Collector Ouptut Current	100	mA
I_R	Reference Output Current	50	mA
I_T	Current Through C_T Terminal	– 5	mA
P_{tot}	Total Power Dissipation at Tamb = 70 °C	1000	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature Range **SG1524** **SG2524** **SG3524**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

CONNECTION DIAGRAMS



THERMAL DATA

			Plastic DIP-16	Ceramic DIP-16	SO16J
$R_{th\ j\text{-}amb}$	Themal Resistance Junction-ambient	Max	80 °C/W	150 °C/W	–
$R_{th\ j\text{-}aluminia}$	Themal Resistance Junction-aluminia	Max	–	–	50 °C/W

* Thermal resistance junction–alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm; 0.65 mm thickness with infinite heatsink.

ELECTRICAL CHARACTERISTICS (unless otherwise stated , these specifications apply for T_j = – 55 °C to+ 125 °C for the SG1524, – 25 °C to + 85 °C for the SG2524, and 0 °C to + 70 °C for the SG3524, V_N = 20 V, and f = 20 KHz).

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage		4.8	5	5.2	4.6	5	5.4	V
ΔV_{REF}	Line Regulation	V_{IN} = 8 to 40 V		10	20		10	30	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
	Ripple Rejection	f = 120 Hz, T_j = 25 °C		66			66		dB
	Short Circuit Current Limit	V_{REF} = 0, T_j = 25 °C		100			100		mA
$\Delta V_{REF}/\Delta T$	Temp. Stability	Over Operating Temp. Range		0.3	1		0.3	1	%
ΔV_{REF}	Long Term Stability	T_j = 125 °C, t = 1000 Hrs		20			20		mV
OSCILLATOR SECTION									
f_{MAX}	Maximum Frequency	C_T = 0.001 µF, R_T = 2 kΩ		300			300		kHz
	Initial Accuracy	R_T and C_T Constant		5			5		%
	Voltage Stability	V_{IN} = 8 to 40 V, T_j = 25 °C			1			1	%
$\Delta f/\Delta T$	Temperature Stability	Over Operating Temp. Range			2			2	%
	Output Amplitude	Pin 3, T_j = 25 °C		3.5			3.5		V
	Output Pulse Width	C_T = 0.01 µF, T_j = 25 °C		0.5			0..5		µs
ERROR AMPLIFIER SECTION									
V_{OS}	Input Offset Voltage	V_{CM} = 2.5 V		0.5	5		2	10	mV
I_b	Input Bias Current	V_{CM} = 2.5 V		2	10		2	10	µA
G_V	Open Loop Volt. Gain		72	80		60	80		dB
CMV	Common Mode Volt.	T_j = 25 °C	1.8		3.4	1.8		3.4	V
CMR	Comm. Mode Rejec.	T_j = 25 °C		70			70		dB
B	Small Signal Bandwidth	A_v = 0 dB, T_j = 25 °C		3			3		MHz
V_O	Output Voltage	T_j = 25 °C	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION									
	Duty-cycle	% Each Output On	0		45	0		45	%
V_{IT}	Input Threshold	Zero Duty-cycle		1			1		V
V_{IT}	Input Threshold	Maximum Duty-cycle		3.5			3.5		V
I_b	Input Bias Current			1			1		µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions	SG1524 SG2524			SG3524			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT LIMITING SECTION									
	Sense Voltage	Pin 9 = 2 V With Error Amplifier Set for Max. Out, Tj = 25 °C	190	200	210	180	200	220	mV
	Sense Voltage T.C.			0.2			0.2		mV/°C
CMV	Common Mode Volt.		− 1		+ 1	− 1		+ 1	
OUTPUT SECTION (each output)									
	Collector-emitter Volt.		40			40			V
	Collector Leakage Cur.	V_{CE} = 40 V		0.1	50		0.1	50	µA
	Saturation Voltage	I_c = 50 mA		1	2		1	2	V
	Emitter Out. Voltage	V_{IN} = 20 V	17	18		17	18		V
t_r	Rise Time	R_c = 2 KΩ, T_j = 25 °C		0.2			0.2		µs
t_f	Fall Time	R_c = 2 KΩ, T_j = 25 °C		0.1			0.1		µs
I_q*	Total Standby Curr.	V_{IN} = 40 V		8	10		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Figure 1 : Open-loop Voltage Amplification of Error Amplifier vs. Frequency.

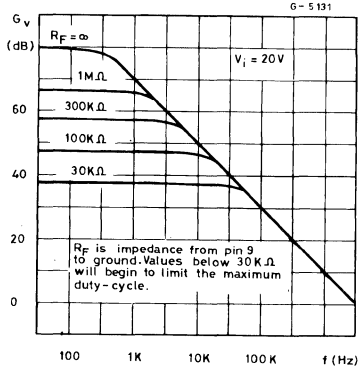


Figure 2 : Oscillator Frequency vs. Timing Components.

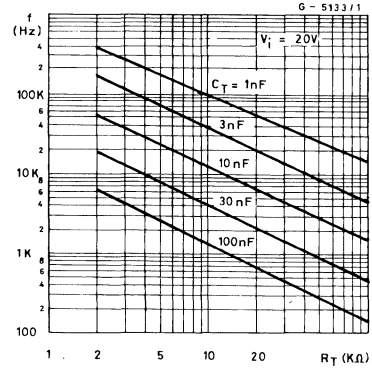


Figure 3 : Output Dead Time vs. Timing Capacitance Value.

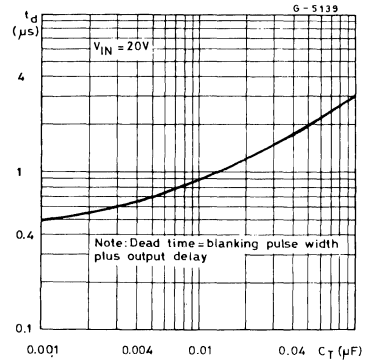


Figure 4 : Output Saturation Voltage vs. Load Current .

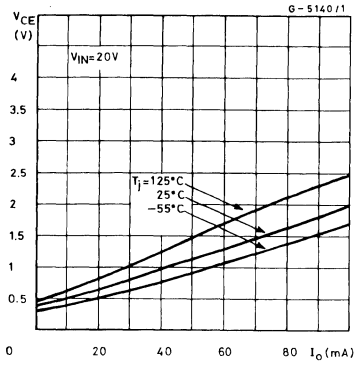
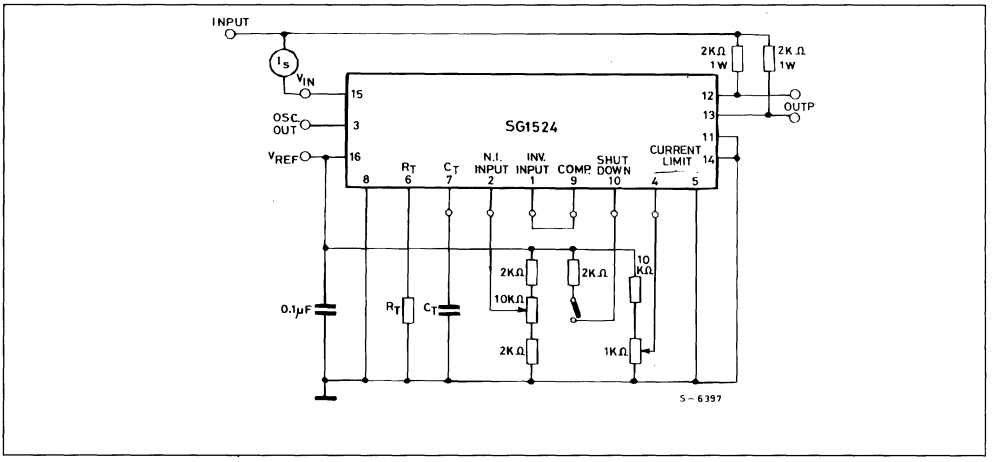


Figure 5 : Open Loop Test Circuit.



PRINCIPLES OF OPERATION

The SG1524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T established a constant charging current for C_T. This results in a linear voltage ramp at CT, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG1524 contains, an on-board 5 V regulator that serves as a reference as well as powering the SG1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generale a feedback signal to error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both output are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs

may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shut-down circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

RECOMMENDED OPERATING CONDITIONS

Supply voltage V_{IN}	8 to 40	V	Timing Resistor, R_T	1.8 to 100	KΩ
Reference Output Current	0 to 20	mA	Timing Capacitor, C_T	0.001 to 0.1	µF
Current through C_T Terminal	- 0.03 to - 2	mA			

TYPICAL APPLICATIONS DATA

OSCILLATOR

The oscillator controls the frequency of the SG1524 and is programmed by R_T and C_T according to the approximate formula :

$$f \approx \frac{1.18}{R_T C_T}$$

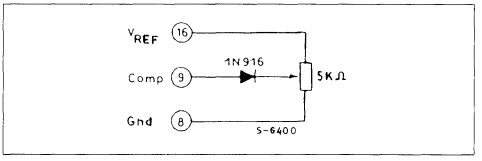
where R_T is in KΩ
C_T is in µF
f is in KHz

Pratical values of C_T fall between 0.001 and 0.1 µF. Pratical values of R_T fall between 1.8 and 100 KΩ. This results in a frequency range typically from 120 Hz to 500 KHz.

BLANKING

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100 pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below :

Figure 6.



SYNCHRONOUS OPERATION

When an external clock is desired, a clock pulse of approximately 3 V can be applied directly to the oscillator ouptut terminal. The impedance to ground at this point is approximately 2 KΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that the external clock.

If two more SG1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

Figure 7: Flyback Converter Circuit.

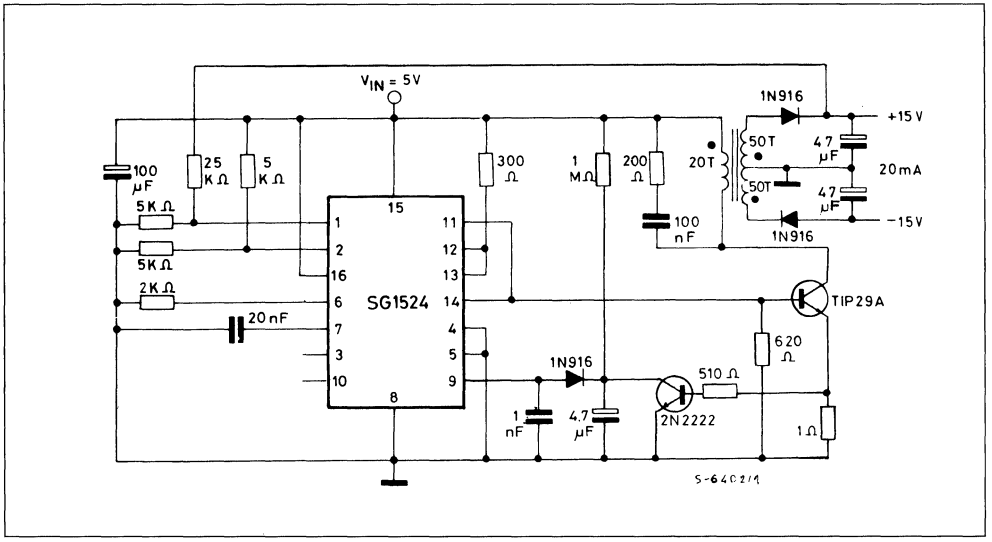
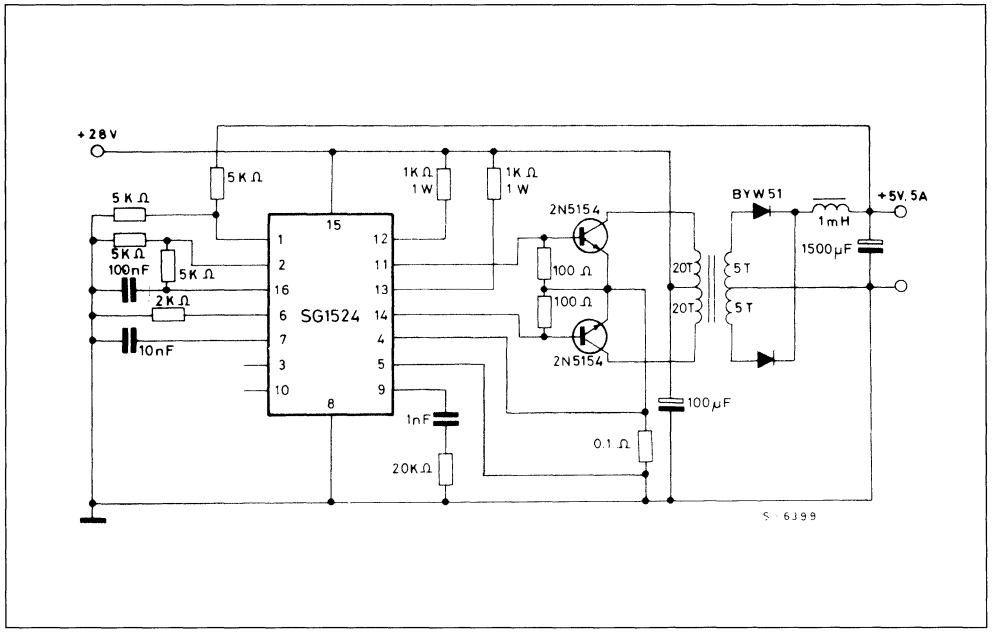


Figure 8: PUSH-PULL transformer-coupled circuit.



SG1525A/27A
SG2525A-3525A/27A

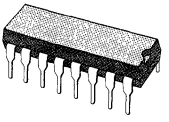
REGULATING PULSE WIDTH MODULATORS

- 8 TO 35 V OPERATION
- 5.1 V REFERENCE TRIMMED TO ± 1 %
- 100 Hz TO 500 KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

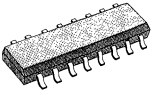
DESCRIPTION

The SG1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1 V reference is trimmed to ± 1 % and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuity and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

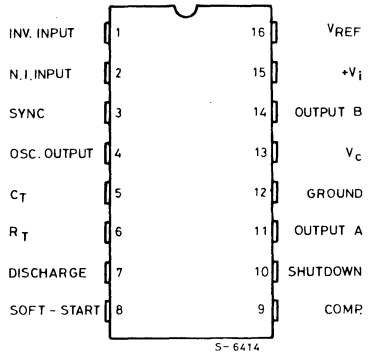
DIP-16
(Plastic -0.25 and Ceramic)



SO16J



CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



Type	Plastic DIP	Ceramic DIP	SO16J
SG1525A	–	SG1525AJ	–
SG1527A	–	SG1527AJ	–
SG2525A	SG2525AN	SG2525AJ	SG2525AP
SG2527A	SG2527AN	SG2527AJ	SG2527AP
SG3525A	SG3525AN	SG3525AJ	SG3525AP
SG3527A	SG3527AN	SG3527AJ	SG3527AP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage	40	V
V_C	Collector Supply Voltage	40	V
I_{OSC}	Oscillator Charging Current	5	mA
I_o	Output Current, Source or Sink	500	mA
I_R	Reference Output Current	50	mA
I_T	Current through C_T Terminal Logic Inputs Analog Inputs	5 – 0.3 to + 5.5 – 0.3 to V_i	mA V V
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to 150	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature : **SG1525A/27A** **SG2525A/27A** **SG3525A/27A**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

THERMAL DATA (DIP-16)

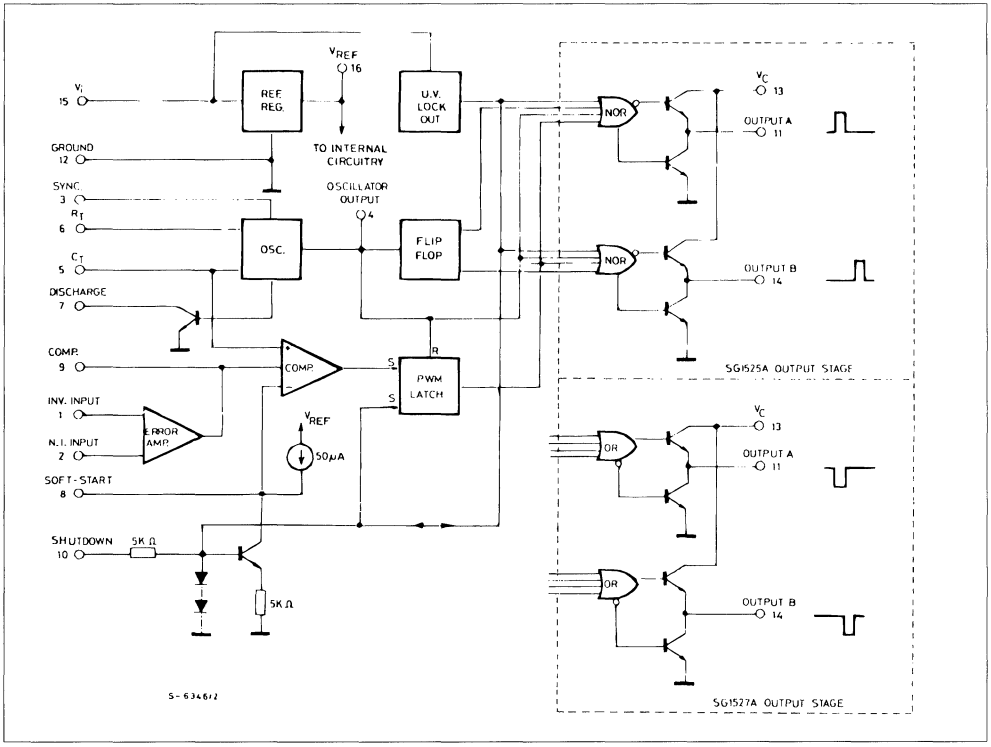
			Ceramic	Plastic
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	–	50 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150 °C/W	80 °C/W

THERMAL DATA (SO16J)

$R_{th\ j\text{-}alumina}$*	Thermal Resistance Junction-alumina	Max	50	°C/W

* Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 × 20 mm ; 0.65 mm thickness with infinite heatsink.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(V_i = 20 V, and over operating temperature, unless otherwise specified)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	T_j = 25 °C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line Regulation	V_i = 8 to 35 V		10	20		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temp. Stability	Over Operating Range		20	50		20	50	mV
*	Total Output Variation	Line, Load and Temperature	5		5.2	4.95		5.25	V
	Short Circuit Current	V_{REF} = 0 T_j = 25 °C		80	100		80	100	mA
*	Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_j = 25 °C		40	200		40	200	µVrms
ΔV_{REF}*	Long Term Stability	T_j = 125 °C, 1000 hrs		20	50		20	50	mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OSCILLATOR SECTION**									
*, •	Initial Accuracy	T_j = 25 °C		± 2	± 6		± 2	± 6	%
*, •	Voltage Stability	V_i = 8 to 35 V		± 0.3	± 1		± 1	± 2	%
$\Delta f/\Delta T$*	Temperature Stability	Over Operating Range		± 3	± 6		± 3	± 6	%
f_{MIN}	Minimum Frequency	R_T = 200 KΩ C_T = 0.1 µF			120			120	Hz
f_{MAX}	Maximum Frequency	R_T = 2 KΩ C_T = 470 pF	400			400			KHz
	Current Mirror	I_{RT} = 2 mA	1.7	2	2.2	1.7	2	2.2	mA
*, •	Clock Amplitude		3	3.5		3	3.5		V
*, •	Clock Width	T_j = 25 °C	0.3	0.5	1	0.3	0.5	1	µs
	Sync Threshold		1.2	2	2.8	1.2	2	2.8	V
	Sync Input Current	Sync Voltage = 3.5 V		1	2.5		1	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)									
V_{OS}	Input Offset Voltage			0.5	5		2	10	mV
I_b	Input Bias Current			1	10		1	10	µA
I_{os}	Input Offset Current				1			1	µA
	DC Open Loop Gain	$R_L \geq$ 10 MΩ	60	75		60	75		dB
*	Gain Bandwidth Product	G_v = 0 dB T_j = 25 °C	1	2		1	2		MHz
*, z	DC Transconduct.	30 KΩ ≤ R_L ≤ 1 MΩ T_j = 25 °C	1.1	1.5		1.1	1.5		ms
	Output Low Level			0.2	0.5		0.2	0.5	V
	Output High Level		3.8	5.6		3.8	5.6		V
CMR	Comm. Mode Reject.	V_{CM} = 1.5 to 5.2 V	60	75		60	75		dB
PSR	Supply Voltage Rejection	V_i = 8 to 35 V	50	60		50	60		dB
PWM COMPARATOR									
	Minimum Duty-cycle				0			0	%
	Maximum Duty-cycle		45	49		45	49		%
•	Input Threshold	Zero Duty-cycle	0.7	0.9		0.7	0.9		V
		Maximum Duty-cycle		3.3	3.6		3.3	3.6	V
*	Input Bias Current			0.05	1		0.05	1	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SHUTDOWN SECTION									
	Soft Start Current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	25	50	80	µA
	Soft Start Low Level	V_{SD} = 2.5 V		0.4	0.7		0.4	0.7	V
	Shutdown Threshold	To outputs, V_{SS} = 5.1 V T_j = 25 °C	0.6	0.8	1	0.6	0.8	1	V
	Shutdown Input Current	V_{SD} = 2.5 V		0.4	1		0.4	1	mA
*	Shutdown Delay	V_{SD} = 2.5 V T_j = 25 °C		0.2	0.5		0.2	0.5	µs
OUTPUT DRIVERS (each output) (V_C = 20 V)									
	Output Low Level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output High Level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-Voltage Lockout	V_{comp} and V_{ss} = High	6	7	8	6	7	8	V
I_C	Collector Leakage	V_C = 35 V			200			200	µA
t_r*	Rise Time	C_L = 1 nF, T_j = 25 °C		100	600		100	600	ns
t_f*	Fall Time	C_L = 1 nF, T_j = 25 °C		50	300		50	300	ns
TOTAL STANDBY CURRENT									
I_s	Supply Current	V_i = 35 V		14	20		14	20	mA

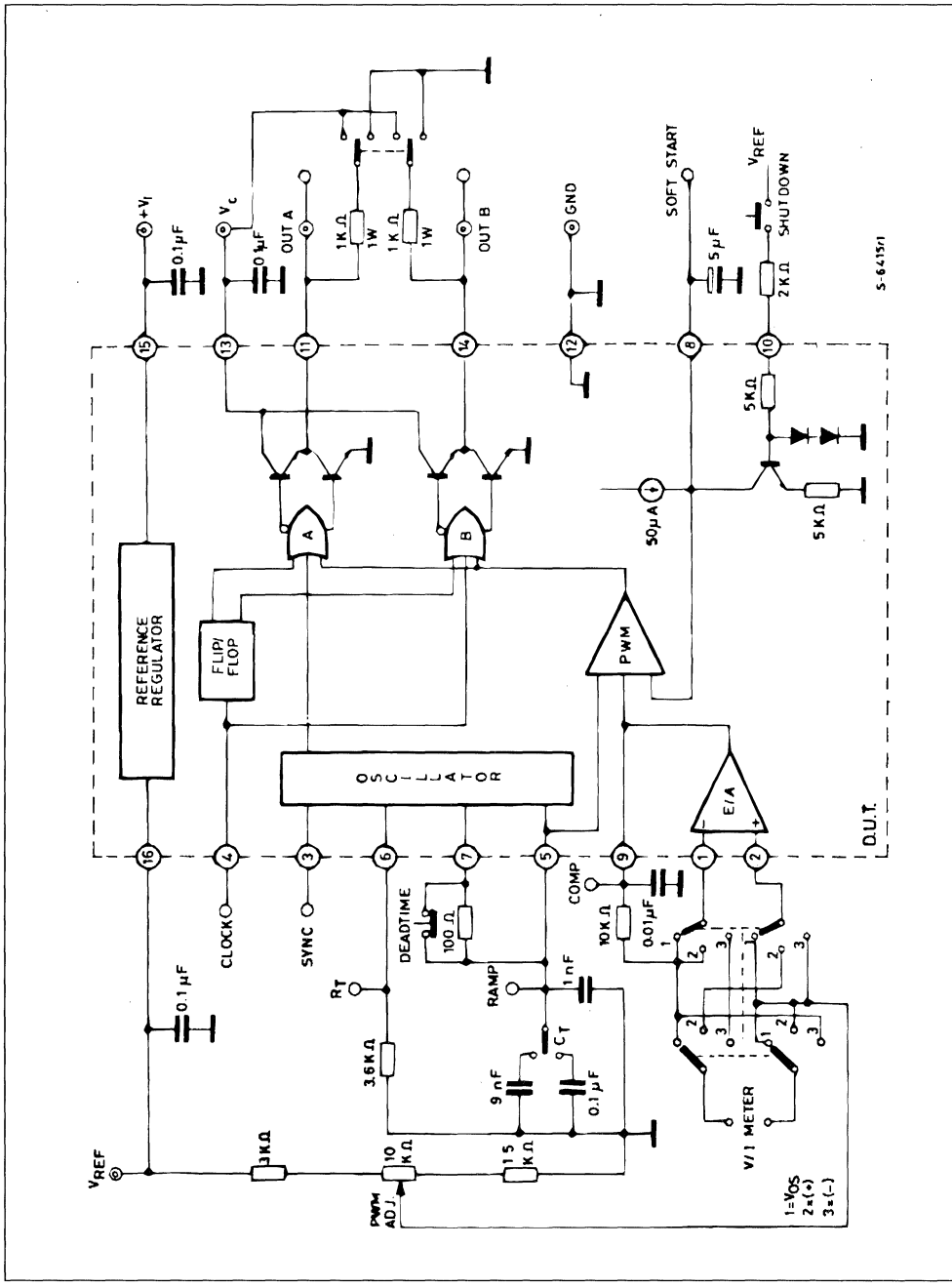
* These parameters, although guaranteed over the recommended operating conditions, are not 100 % tested in production.

• Tested at f_{osc} = 40 KHz (R_T = 3.6 KΩ, C_T = 0.1 µF, R_D = 0 Ω). Approximate oscillator frequency is defined by :

$$f = \frac{1}{C_T (0.7 R_T + 3 R_D)}$$

■ DC transconductance (g_M) relates to DC open-loop voltage gain (G_v) according to the following equation : $G_v = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_v when the error amplifier output is loaded.

TEST CIRCUIT



RECOMMENDED OPERATING CONDITIONS (•)

Parameter	Value
Input Voltage (V_i)	8 to 35 V
Collector Supply Voltage (V_C)	4.5 to 35 V
Sink/Source Load Current (steady state)	0 to 100 mA
Sink/Source Load Current (peak)	0 to 400 mA
Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 400 KHz
Oscillator Timing Resistor	2 KΩ to 150 KΩ
Oscillator Timing Capacitor	0.001 µF to 0.1 µF
Dead Time Resistor Range	0 to 500 Ω

(•) Range over which the device is functional and parameter limits are guaranteed.

Figure 1 : Oscillator Charge Time vs. R_T and C_T.

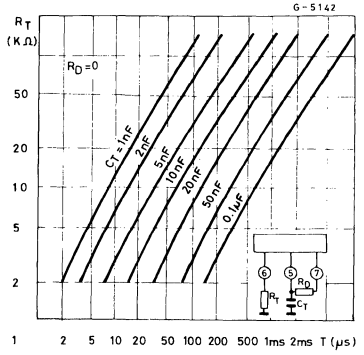


Figure 2 : Oscillator Discharge Time vs. R_D and C_T.

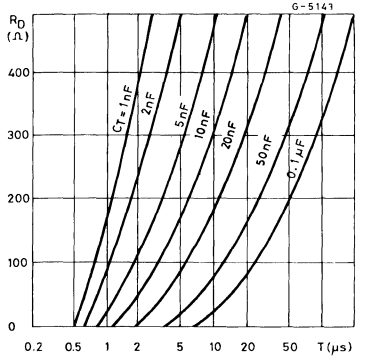


Figure 3 : SG1525A Output Saturation Characteristics.

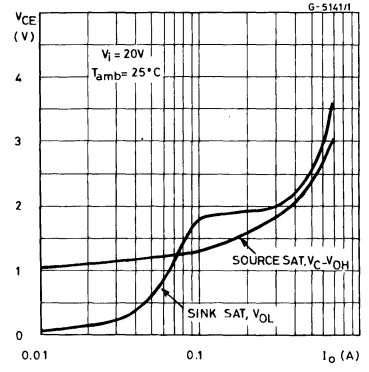


Figure 4 : Error Amplifier Voltage Gain and Phase vs. Frequency.

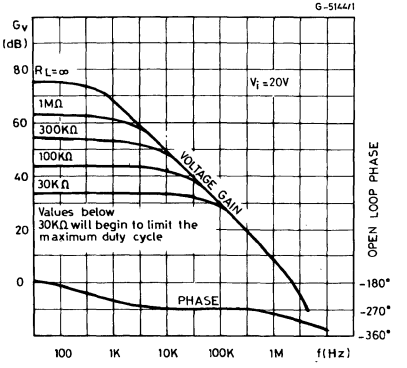
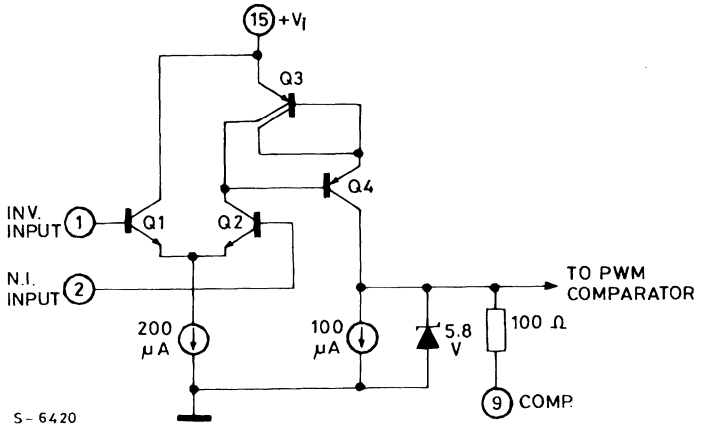


Figure 5 : SG1525A Error Amplifier.



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions : the PWM latch is immediately set providing the fastest turn-off signal to the outputs ; and a 150 µA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Figure 6 : SG1525A Oscillator Schematic.

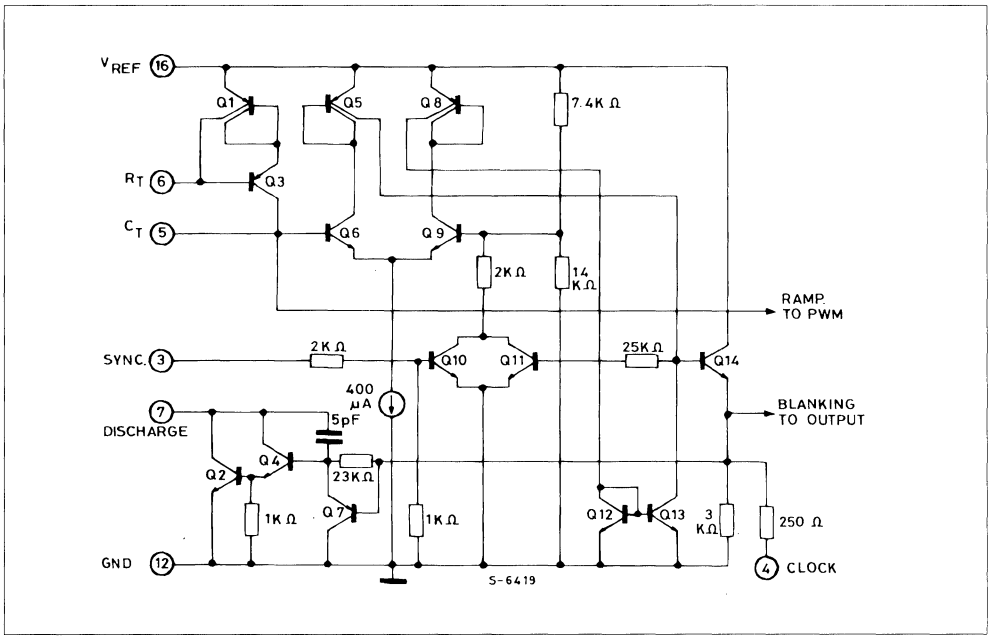


Figure 7 : SG1525A Output Circuit (1/2 circuit shown).

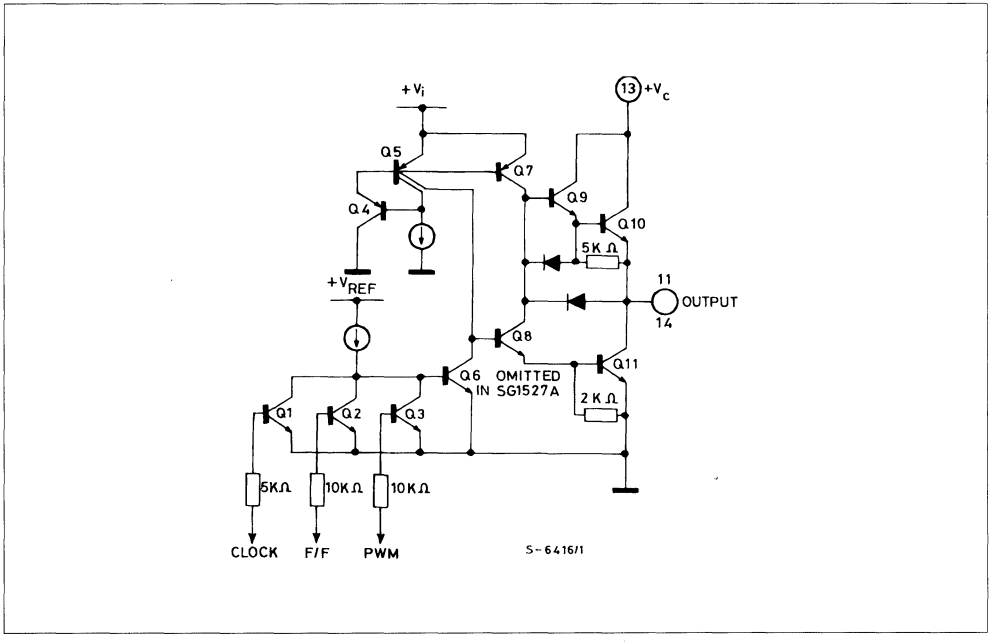
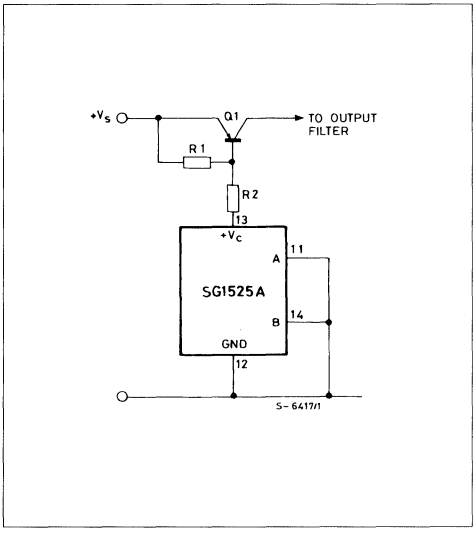
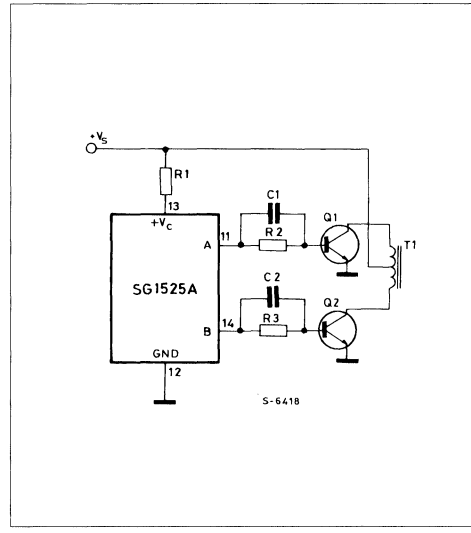


Figure 8.



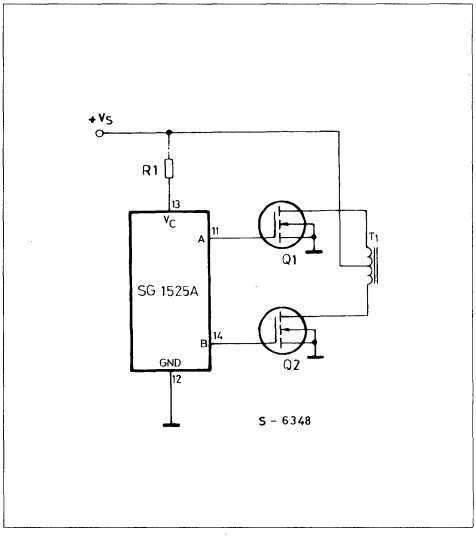
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 9.



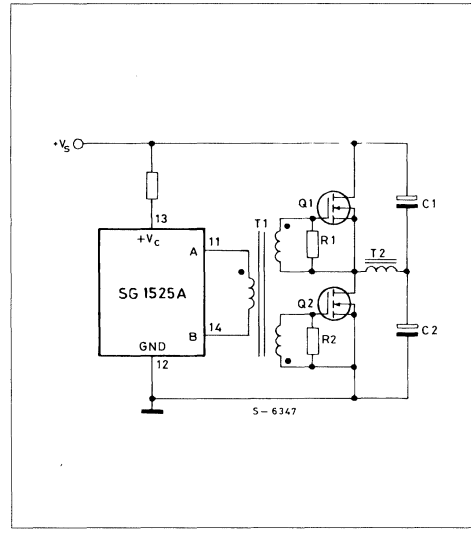
In conventional push-pull bipolar designs, forward base drive is controlled by R_1 - R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.

Figure 10.



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Figure 11.



Low power transformers can be driven directly by the SG1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

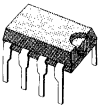
SGS-THOMSON MICROELECTRONICS

TDA0159A

PROXIMITY DETECTOR

- SUPPLY VOLTAGE : + 5 TO + 16 V
- OSCILLATOR FREQUENCY : 50 kHz TO 10 MHz
- OUTPUT CURRENT : ± 20 mA

MINIDIP/2



S0-8J

ORDER CODES : TDA0159ADP (Minidip)
TDA0159AFP (SO-8)

DESCRIPTION

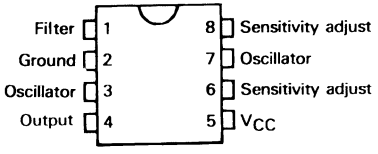
The TDA0159A has been designed for metallic body detection by detecting variations in high frequency Eddy current losses. The circuit acts as an oscillator with the addition of an external tuned circuit. Output signal level is varied by an approaching metallic object.

The circuit is protected against overvoltages (+ 26 to + 35 V) by a built-in peak limiter.

Output to ground and output to V_{CC} short-circuit protections are also implemented.

PIN CONNECTION

MINIDIP / SO-8



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (internally limited by zener)	26	V
I_O	Output Current (internally limited)	± 20	mA
f_{osc}	Oscillator Frequency	10	MHz
T_j	Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature Range	− 55 to + 150	°C

OPERATING MODE

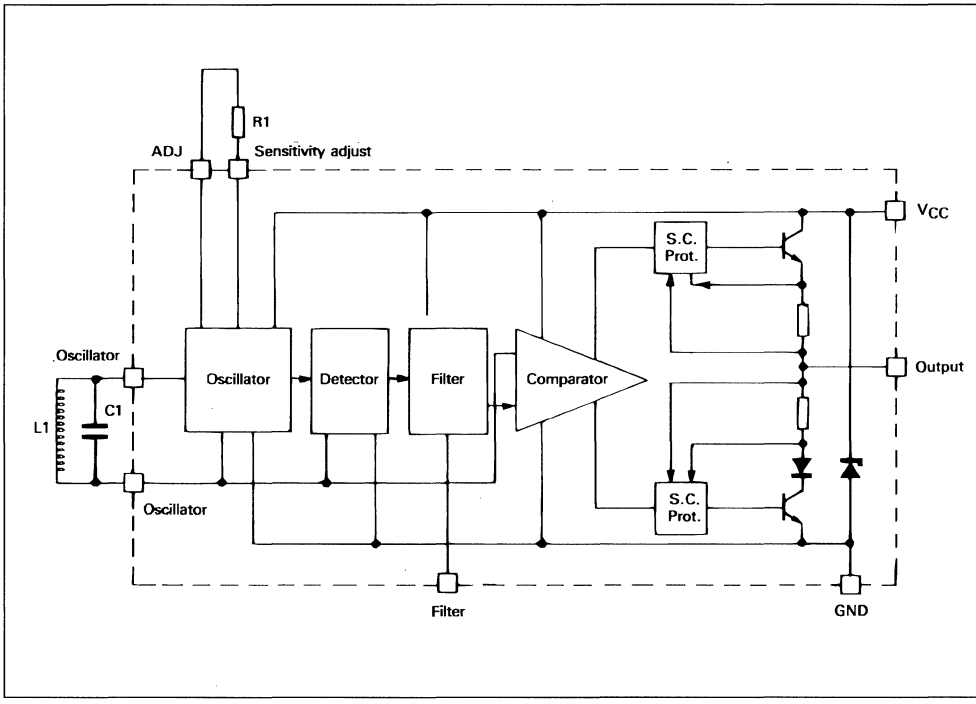
Between terminals 7 and 3 integrated circuit acts like a negative resistance equal to external resistor R1 connected on terminals 6 and 8.

The oscillation stops when load resistance Rp of tuned circuit is smaller than R1. Then the output voltage is high (pin 4).
The oscillation sustains when loss resistance Rp of tuned circuit is higher than R1. Then the output voltage is low.

$$(fOSC = \frac{1}{2\pi \sqrt{(L1 \times C1)}})$$

Eddy currents induced by coil L1 in a metallic piece, fix loss resistance Rp.

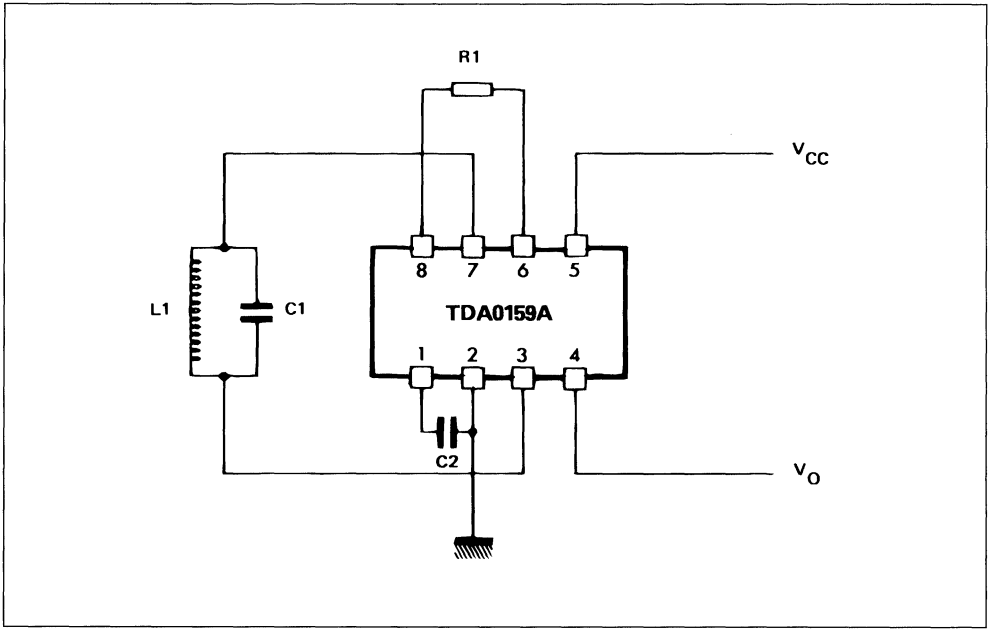
SCHEMATIC DIAGRAM



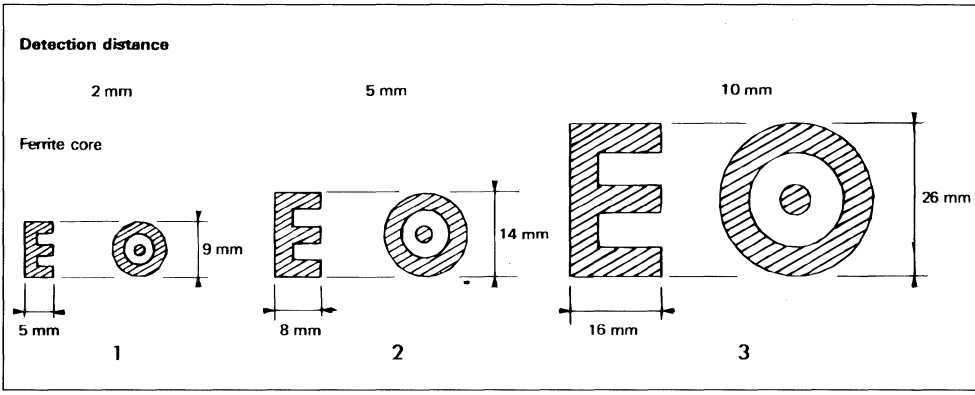
ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	5	–	16	V
$V_{CC(max)}$	Maximum Voltage (non-destructive t < 1 min)	–	–	24	V
$V_{CC(peak)}$	Clipping Voltage (limited by integrated zener diode, I_{CC} continuous < 10 mA, I_C pulse < 150 mA (peak), t < 10 ms)	26	30	35	V
I_{CC}	Supply Current (V_{CC} = + 13.5 V, I_O = 0)	–	2	–	mA
V_{OL}	Output Low Voltage (remote target V_{CC} = + 13.5 V, $I_O \geq -10$ mA)	–	–	2	V
V_{OH}	Output High Voltage Determined by Internal $V_{CC} \geq +7$ V (close target) 7 V ≤ V_{CC} ≤ + 16 V, $I_O \leq 10$ mA 5 V ≤ V_{CC} ≤ + 7 V, $I_O \leq 4$ mA	 5.4 3.9	 – –	 6.7 V_{CC}-0.2	V
f_{osc}	Oscillator Frequency (operating conditions)	–	–	10	MHz
f	Target Detection Frequency	–	–	10	kHz
R_n	Negative Value of the Resistance between Pin 7 and Pin 3 : 4 kΩ < R1 < 50 kΩ (R1 = sensitivity adjustement resistor)	0.9 x R1	R1	1.1 x R1	–
R1	Maximum Value of Sensitivity Adjustement Resistor R1 Connected between Pin 6 and Pin 8	–	–	50	kΩ
H_{yst}	Hysteresis (measured on detection range)	–	2	–	%

APPLICATION SCHEMATIC



TYPICAL APPLICATION EXAMPLES



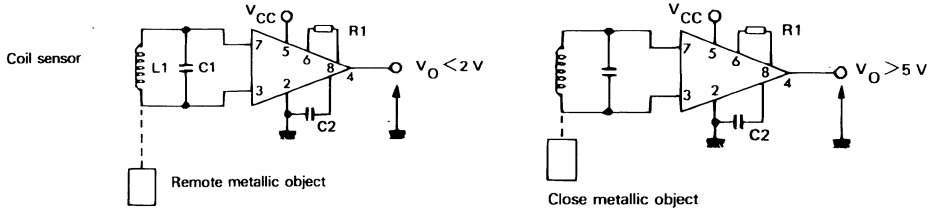
	Detection Distance (*)	L1 (μH)	C1 (pF)	f_{osc} (kHz)	R1 (kΩ)	C2 pF
1	2 mm	30	120	2 650	6.8	–
2	5 mm	300	470	425	27	100
3	10 mm	2 160	4 700	50	27	10 000

* Ingot steel target.

COIL CHARACTERISTICS

	Core	Coil Former	Wire	Number of Turns
1	Cofelec 432 FP 9 X 5 SE	1/2 CAR 091 – 2	THOMSON Fils et Câbles Thomrex 14 (14 / 100 mm)	40
2	Cofelec 432 FP 14 X 8 SE	1/2 CAR 142 – 2	THOMSON Fils et Câbles Thomrex 14 (14 / 100 mm)	100
3	Cofelec 432 FP 26 X 16 SE	1/2 CAR 262 – 2	THOMSON Fils et Câbles Thomrex 14 (14 / 100 mm)	200

* * The above results are obtained with single wire coil. When using Litz wire instead of single wire, the parallel resistance of the coil becomes higher and the value of R1 may be increased, resultaint in better sensitivity.



SGS-THOMSON MICROELECTRONICS

TDA0161

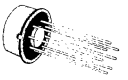
PROXIMITY DETECTORS

- OUTPUT CURRENT : 10 mA
- OSCILLATOR FREQUENCY : 10 MHz
- SUPPLY VOLTAGE : + 4 TO + 35 V

MINIDIP/2

SO-8J

TO-99



ORDER CODES : TDA0161DP (Minidip)
TDA0161FP (SO-8J)
TDA0161CM (TO-99)

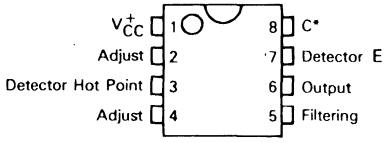
DESCRIPTION

These monolithic integrated circuits are designed for metallic body detection by detecting the variations in high frequency Eddy current losses. With an external tuned circuit they act as oscillators. Output signal level is altered by an approaching metallic object.

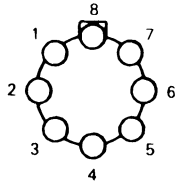
Output signal is determined by supply current changes. Independent of supply voltage, this current is high or low according to the presence or the absence of a close metallic object.

PIN CONNECTIONS (top views)

MINIDIP/SO-8



TO-99



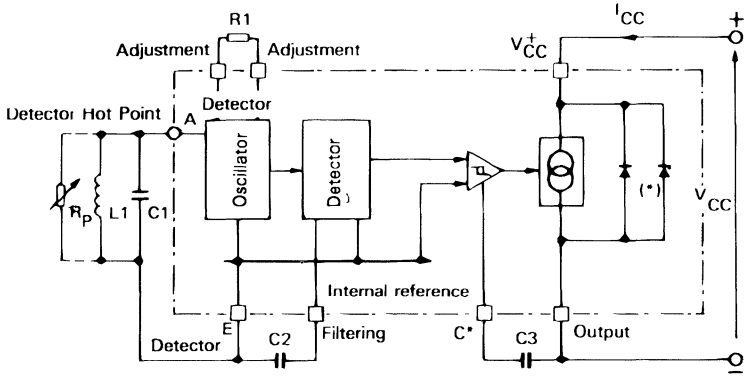
1 - Detector Hot Point
2 - Adjust
3 - Filtering
4 - Output
5 - Detector E
6 - C
7 - V_{CC}^{+}
8 - Adjust

Pin 4 connected to case

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	35	V
T_j	Junction Temperature DP, FP Suffix CM Suffix	 + 150 + 175	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

TDA0161DP : - 40 °C < T_{amb} < + 100 °C
TDA0161FP : - 40 °C < T_{amb} < + 100 °C
TDA0161CM : - 40 °C < T_{amb} < + 140 °C
P_{tot} < 150 mW
(unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	TDA0161	4	–	35	V
–	Reverse Voltage Limitation (I_{CC} = - 100 mA)		–	– 1	–	V
I_{CC}	Supply Current, Close Target (T_{amb} = + 25 °C) + 4 V < V_{CC} < + 35 V	TDA 0161	8	10	12	mA
I_{CC}	Supply Current, Remote Target + 4 V < V_{CC} < + 35 V	TDA 0161	–	–	1	mA
–	Supply Current Transition Time C3 = 0 C3 ≠ 0		 – –	 1 [100 x C3(nF)]	 –	µs
f_{osc}	Oscillator Tuning Frequency		–	–	10	MHz
f_O	Output Frequency (C3 = 0)		0	–	10	kHz
ΔI_{CC}	Output Current Ripple - C3 = 0, C2 (pF) > 150/f_{osc} (MHz)		–	–	20	µA
R_n	Negative Resistance on Terminals A and E (4 kΩ < R1 < 50kΩ, f_{osc}< 3 MHz)		0.9 R1	R1	1.1 R1	–
H_{yst}	Hysteresis at Detection Point C2 (Pf) > 150/f_{osc} (MHz)		0.5	–	5	%

* If the circuit is used at a frequency higher than 3 MHz, it is recommended to connect a capacitor of 100 pF between terminals E and D.

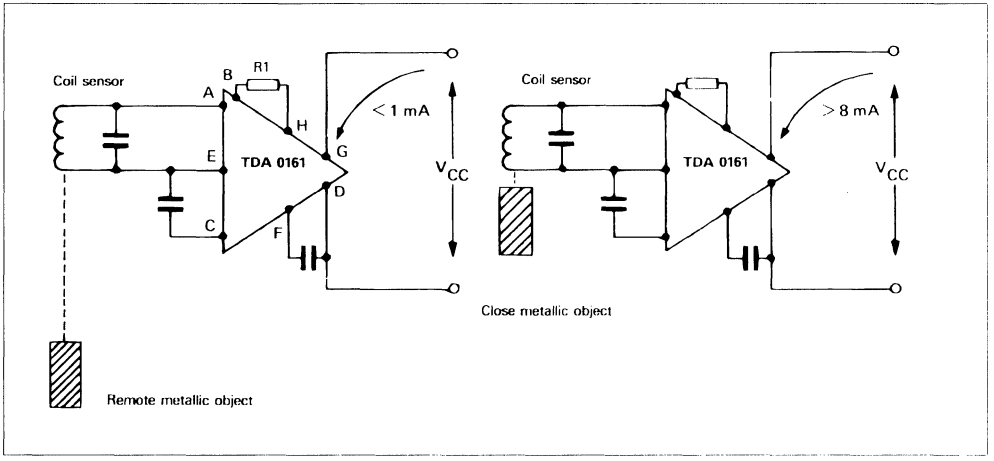
OPERATING MODE

Between terminals A and E, the integrated circuit acts like a negative resistance equal to the external resistor R1 connected between terminals B and H.

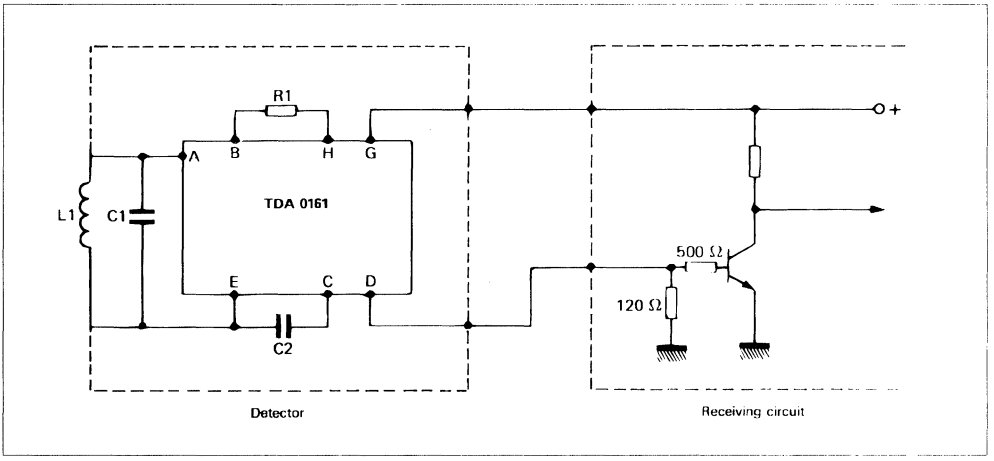
The oscillation stops when loss resistance Rp of tuned circuit becomes smaller than R1. Then, the supply current will be I_{CC} = 10 mA (pins G and D).

The oscillation sustains when loss resistance Rp of tuned circuit becomes higher than R1. Then, the supply current will be I_{CC} 1 mA (pins G and D).

Eddy currents induced by coil L1 in a metallic body, determine loss resistance Rp.



TYPICAL APPLICATIONS



Detection Range (*)	L1 (μH)		C1 (pF)	f_{osc} (kHz)	R1 (kΩ)	C2 pF
2 mm	30	(1)	120	2650	6.8	47
5 mm	300	(2)	470	425	27	470
10 mm	2160	(3)	4700	50	27	3300

(*) Ingot steel target.

COIL CHARACTERISTICS

	Core	Coil Former	Wire**	Number of Turns
1	Cofelec 432 FP 9 x 5 SE	1/2 CAR 091 - 2	THOMSON Fils et Câbles Thomrex 14 (14/100 mm)	40
2	Cofelec 432 FP 14 x 8 SE	1/2 CAR 142 - 2	THOMSON Fils et Câbles Thomrex 14 (14/100 mm)	100
3	Cofelec 432 FP 26 x 16 SE	1/2 CAR 262 - 2	THOMSON Fils et Câbles Thomrex 14 (14/100 mm)	200

** The above results are obtained with single wire coil. When using Litz wire instead of single wire, the parallel resistance of the coil becomes higher and the value of R1 may be increased, resulting in better sensitivity.

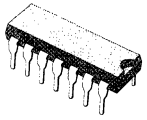
SGS-THOMSON MICROELECTRONICS

TDE0160

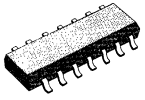
PROXIMITY DETECTOR

- SUPPLY VOLTAGE : + 4 TO + 36 V
- SUPPLY CURRENT : < 1.2 mA
- OUTPUT TRANSISTORS : I = 20 mA ; $V_{CE\ (sat)} \leq 1100$ mV
- OSCILLATOR FREQUENCY : < 1 MHz
- LOSS RESISTANCE : 5 TO 50 kΩ.

DIP-14/2
(Plastic)



SO-14J



ORDER CODES : TDE0160DP (DIP-14)
TDE 0160FP (SO-14J)

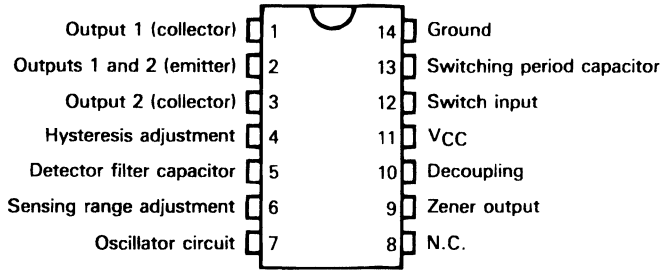
DESCRIPTION

The TDE0160 is designed to detect metal bodies by the effect of Eddy currents on the HF losses of a coil. It has two complementary open collector outputs with peak limiting. Hysteresis is adjustable, and an electronic switching circuit is incorporated for disabling both outputs.

An internal zener diode maintains the supply voltage to the circuit in "dipole" operation.

PIN CONNECTION

DIP-14 / SO-14J

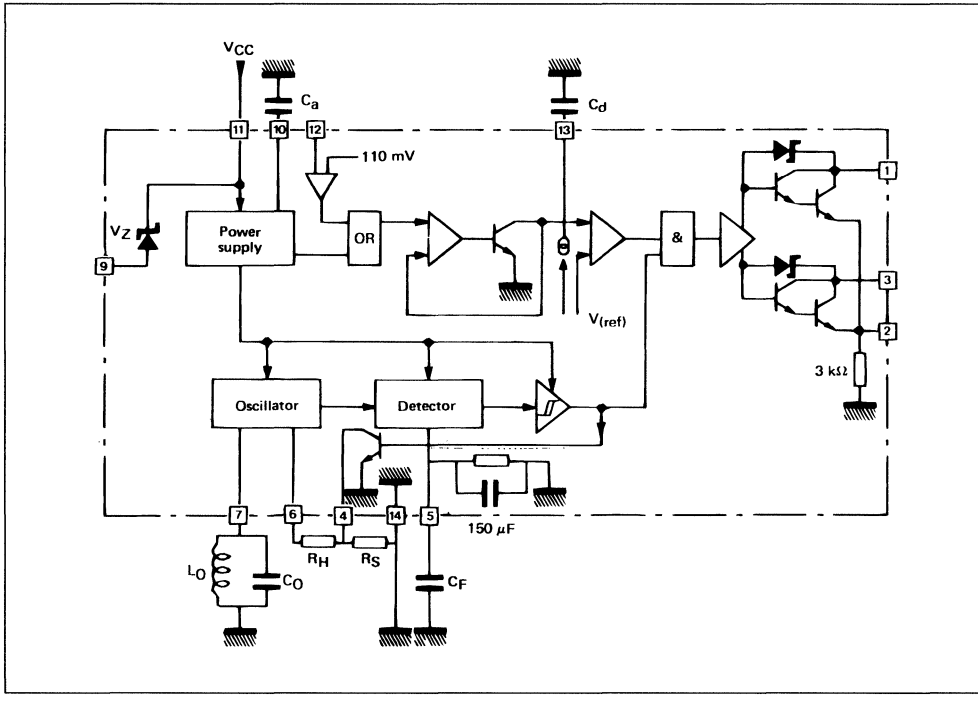


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	36	V
V_O	Output Voltage*	36	V
I_O (I_1-I_3)	Output Current (I_1-I_3)	40	mA
I_Z	Zener Current	40	mA
T_j	Junction Temperature	+ 150	°C
T_{oper}	Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Internal peak limiting to protect against transient voltage surges.

SCHEMATIC DIAGRAM

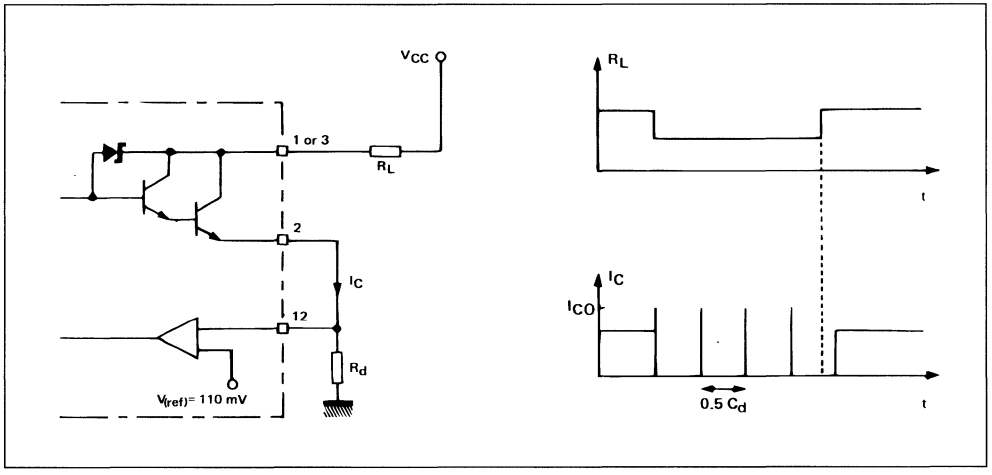


ELECTRICAL CHARACTERISTICS (T_{amb} = + 25 °C unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	Pin 11	4	–	36	V
V_Z	Zener Voltage (I_Z = 20 mA)	Pins 9–11	3	–	4	V
I_{CC}	Supply Current	Pin 11	–	–	1.2	mA
–	Limiting (I = 0.1 mA)	Pin 1 or 3	–	42	–	V
–	Output Transistor Saturation Voltage (I_1 or I_3 = + 20 mA)	Pin 1 or 3	–	0.9	1.1	V
–	Output Transistor Leakage Current (V = + 30 V)	Pin 1 or 3	–	–	2	µA
–	Switching Threshold	Pin 12	90	110	130	mV
R_n	Negative Resistance* (5 kΩ < R_H < 50 kΩ; f = 100 kHz ; R_S = 0)		–	$R_n = R_H$	–	–
–	Inherent Hysteresis (R_2 = 0)		–	1	2	%
–	Programmed Hysteresis (H < 15 %)		–	$\frac{R_S}{R_S + R_H}$	–	%
f_{osc}	Oscillation Frequency		–	–	1	MHz
–	Switching Frequency (with matched oscillator circuit)		–	750	–	Hz
–	Switching Time-delay		–	0.5 C_d (µF)	–	s
–	Switching Response Time (C_d = 10 nF ; V_{CC} = + 20 V)		–	10	–	µs

* See characteristic curves

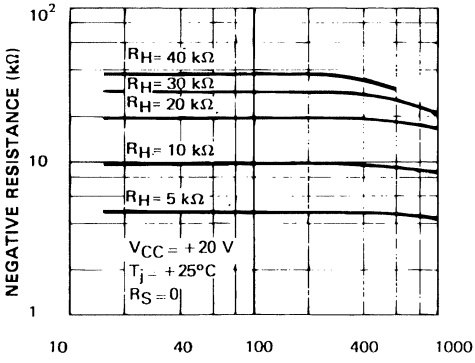
SWITCHING OPERATION



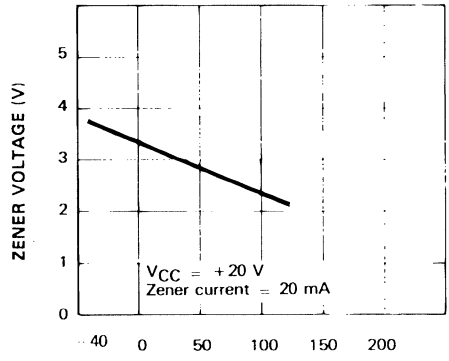
If I_C exceeds I_{CO}, where $I_{CO} = \frac{V_{(ref)}}{R_d}$, the switch cuts off the output transistors and tests the value of current I_C, with time constant 0.5 C_d.

On power up the internal start system cuts off the output transistors until V_{CC} reaches a value permitting normal operation of the circuit.

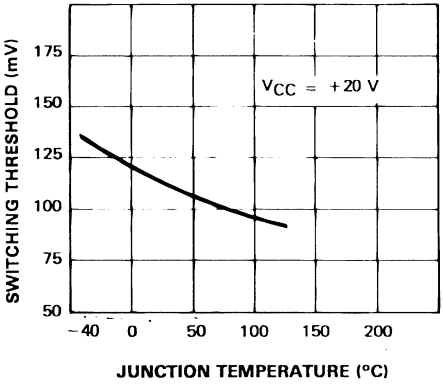
NEGATIVE RESISTANCE
vs
FREQUENCY



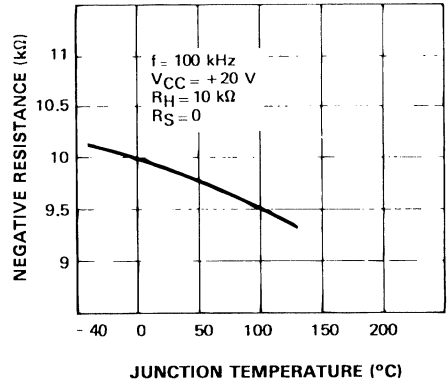
ZENER VOLTAGE
vs
JUNCTION TEMPERATURE



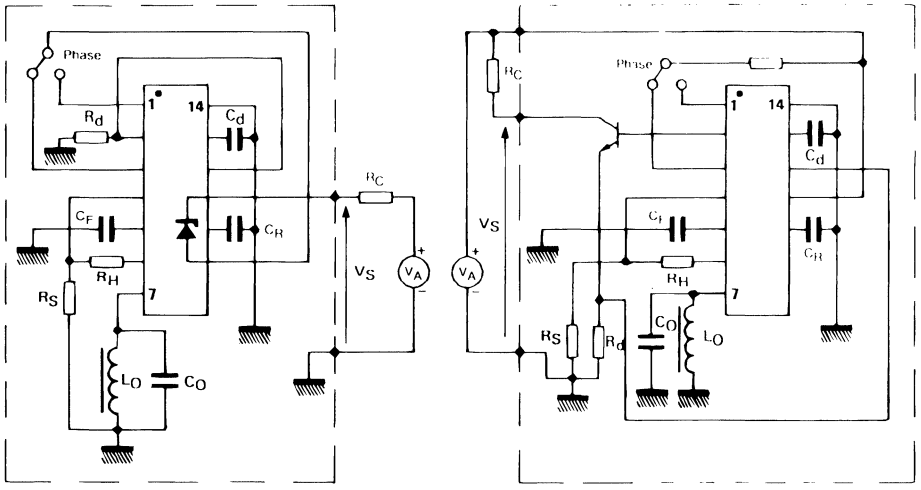
SWITCHING THRESHOLD
vs
JUNCTION TEMPERATURE

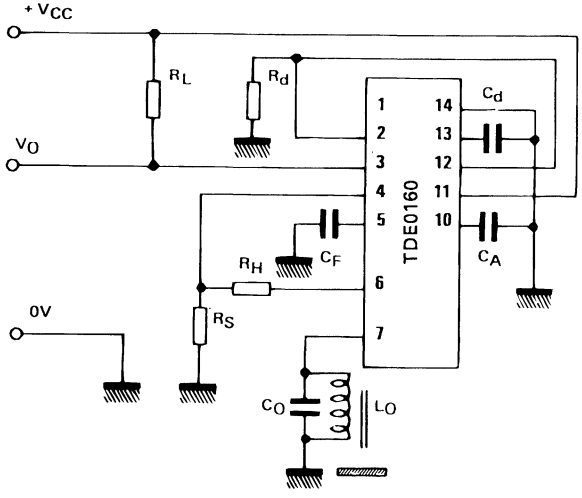


NEGATIVE RESISTANCE
vs
JUNCTION TEMPERATURE



TYPICAL APPLICATION DIAGRAMS





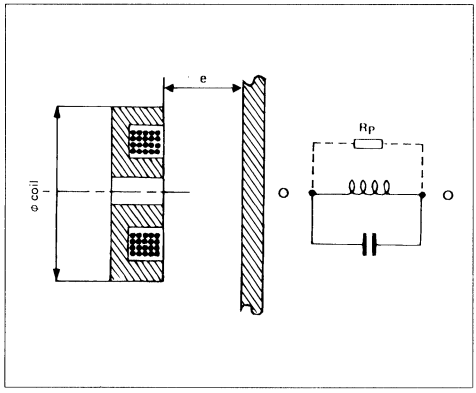
c)

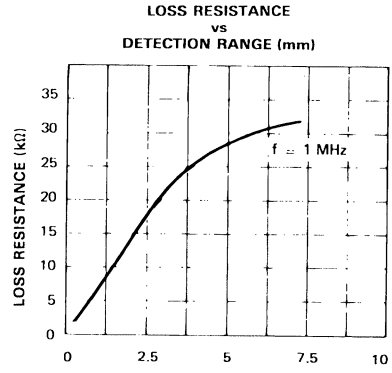
C_a : 10 nF
C_f : 1 nF
C_d : 10 nF
C_0 : 390 pF
L_0 : 65 µH to 1 MHz
R_d : 10 Ω
R_H : 15 kΩ
R_S : 3 kΩ
R_L : 2.2 kΩ

V_{CC} : 20 V
$f_0 \approx$ 1MHz
e_{mean} = 2.5mm

Φ coil : 14 mm
Core COFELEC 432 FP
Turns : 47
Stranded wire : 15 x 5/100

MILD STEEL

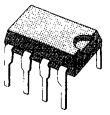

e
φ coil
Rp


LOSS RESISTANCE
vs
DETECTION RANGE (mm)
LOSS RESISTANCE (kΩ)
35
30
25
20
15
10
5
0
0
2.5
5
7.5
10
f = 1 MHz

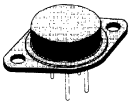
TDE1647/A, TDE1747 TDE1607, TDF1607

INTERFACE CIRCUIT - RELAY AND LAMP-DRIVER

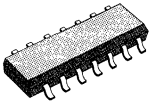
- OPEN GROUND PROTECTION (TDE1747)
- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION TO GROUND
- THERMAL PROTECTION WITH HYSTERESIS TO AVOID THE INTERMEDIATE OUTPUT LEVELS
- LARGE SUPPLY VOLTAGE RANGE : + 10 V TO + 45 V
- SHORT-CIRCUIT PROTECTION TO V_{CC}



MINIDIP/2
(DP)



METAL CAN
(CM)



SO-14J

DESCRIPTION

The TDE1647, TDE1747, TDE1607, TDF1607 are monolithic designed for high current and high voltage applications, specifically to drive lamps, relays stepping motors.

These devices are essentially blow-out proof. Current limiting is available to limit the peak output current to safe values, the adjustment only requires one external resistor. In addition, thermal shut down is provided to keep the I.C. from overheating. If internals dissipation becomes too great, the driver will shut down to prevent excessive heating. Moreover, TDE1747 has an open ground protection. The output is also protected from short-circuits with the positive power supply.

The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies down to the single + 12 V or + 24 used for industrial electronic systems.

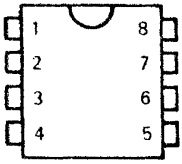
ORDER CODES

Part Number	Temperature Range	Package		
		CM	DP	FP
TDE1647	– 25 °C to + 85 °C	•	•	
TDE1747	– 25 °C to + 85 °C	•	•	•
TDE1607	– 25 °C to + 85 °C	•	•	
TDF1647A	– 25 °C to + 85 °C	•		
TDF1607	– 40 °C to + 85 °C		•	

Example : TDE1647DP - TDE1607CM

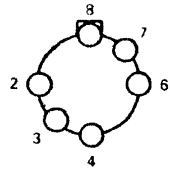
PIN CONNECTION (top view)

MINIDIP



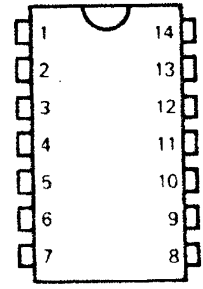
1. N.C. - 2 Inverting input
3. Non-inverting input - 4. GND
5. Output - 6. V_{sense} - 7. V_{CC} - 8. N.C.

METAL CAN



2. Inverting input -
3. Non-inverting input - 4. GND -
6. Output - 7. V_{sense} - 8. V_{CC}

SO-14



1. N.C. - 2. N.C. - 3. N.C. - 4. V_{CC}
5. Inverting input - 6. N.C. -
7. Non-inverting input - 8. GND -
9. N.C. - 10. Output - 11. V_{sense}
12. N.C. - 13. N.C. - 14. N.C.

ABSOLUTE MAXIMUM RATINGS

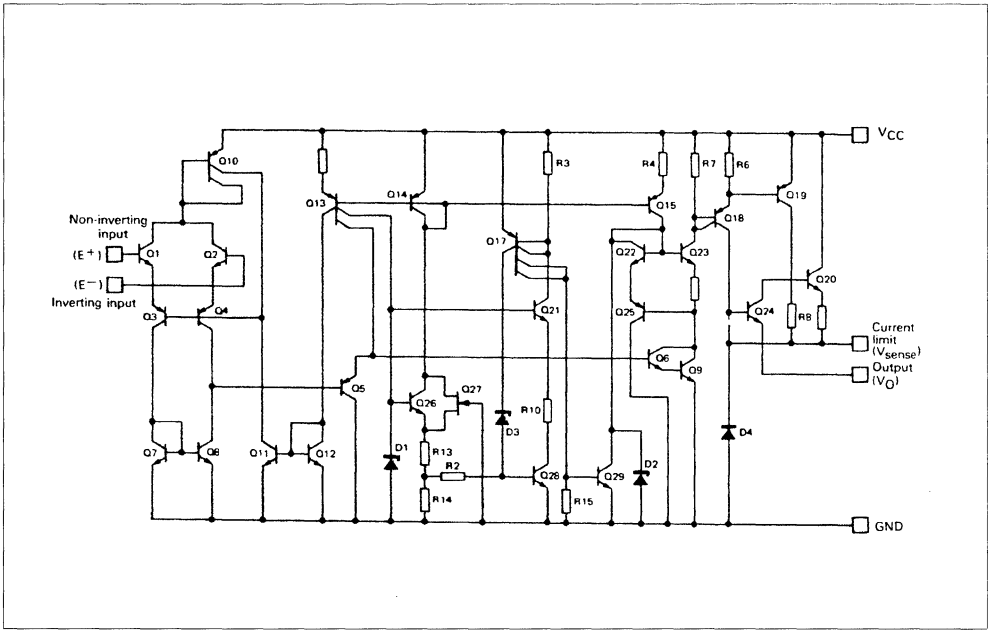
Symbol	Parameter	TDE1647/A TDE1747	TDE1607	Unit
V_{CC}	Supply Voltage	50 *	36	V
V_{ID}	Differantial Input Voltage	50	36	V
V_I	Input Voltage	50	36	V
I_O	Output Current	1000	500	mA
P_{tot}	Power Dissipation (T_{amb} = + 25 °C)	Internally Limited		W
T_{stg}	Storage Temperature Range	– 65 to + 150		°C
T_{oper}	Operating Ambient Temperature Range TDE TDF	 – 25 to + 85 – 40 to + 85		°C

(*) V_{CC} = + 60 V, t ≤ 10 mS for TDE 1647A.

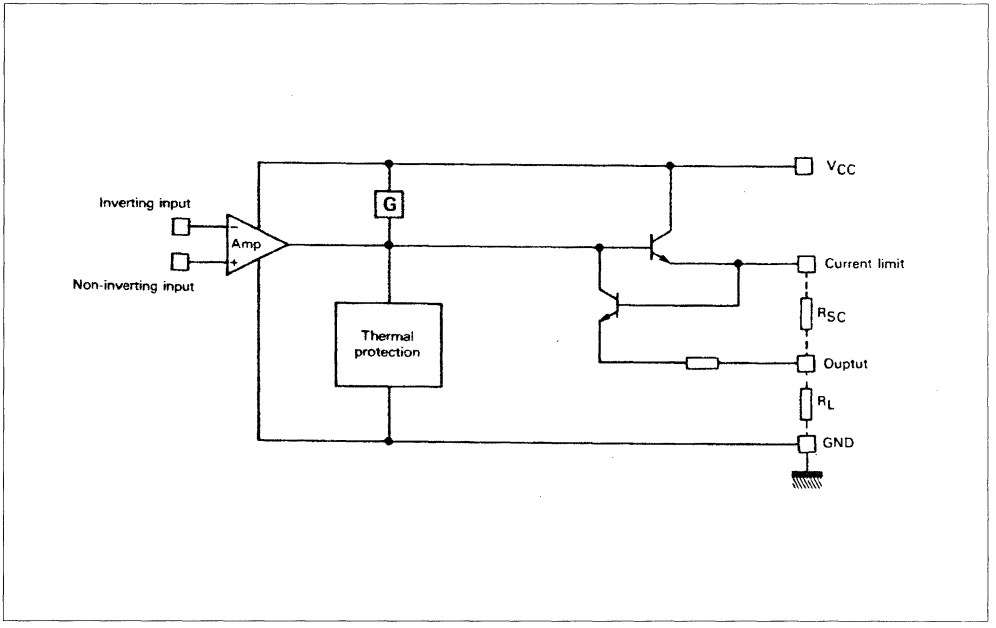
THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	METAL CAN MINIDIP	45 50	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	METAL CAN MINIDIP	185 120	°C/W
R_{th}	Junction-ceramic Substrate (case glued to substrate)	SO14	90	°C/W
R_{th}	Junction-ceramic Substrate (case glued to substrate, substrate temperature maintened constant)	SO14	65	°C/W

SCHEMATIC DIAGRAM



SIMPLIFIED CIRCUIT



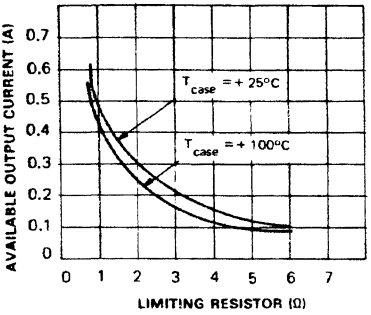
ELECTRICAL CHARACTERISTICS (note 1) $T_j \leq +150$ °C
TDE1647, A TDE1747 : -25 °C $\leq T_{amb} \leq +85$ °C, $+8$ V $\leq V_{CC} \leq +45$ V, $I_O = 300$ mA
TDE1607DP : -25 °C $\leq T_{amb} \leq +85$ °C, $+8$ V $\leq V_{CC} \leq +30$ V, $I_O = 150$ mA
TDE1607CM : -25 °C $\leq T_{amb} \leq +85$ °C, $+8$ V $\leq V_{CC} \leq +30$ V, $I_O = 300$ mA
TDE1607DP : -40 °C $\leq T_{amb} \leq +85$ °C, $+8$ V $\leq V_{CC} \leq +30$ V, $I_O = 150$ mA

Symbol	Parameter	TDE1647, A TDE1747			TDF1607DP TDE1607CM(a) TDE1607DP, FP			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	Input Offset Voltage - (note 2)	–	2	50	–	2	50	mV
I_{IB}	Input Bias Current	–	0.1	1.5	–	0.1	1.5	µA
I_{CC}	Supply Current ($V_{CC} = +24$ V, $I_O = 0$)							mA
	High Level	–	4	6	–	4	6	
	Low Level	–	2	4	–	2	4	
$V_{I(max)}$	Common-mode Input Voltage Range	2	–	$V_{CC}-2$	2	–	$V_{CC}-2$	V
I_{SC}	Short-circuit Current Limit ($T_{amb} = +25$ °C, $V_{CC} = +24$V)							mA
	$R_{SC} = 1.5\ \Omega$ TDE1747	–	480	–	–	–	–	
	$R_{SC} = 1.5\ \Omega$ TDE1647	–	540	–	–	–	–	
	$R_{SC} = 3.3\ \Omega$	–	–	–	–	230	–	
	$R_{SC} = \infty$	–	35	50	–	35	50	
$V_{CC}-V_O$	Output Saturation Voltage (output high) ($R_{SC} = 0$, $V_{I+}-V_{I-} \geq 50$ mV)							V
	$I_O = 300$ mA, $T_j = +25$ °C	–	1.15	1.4	–	1.2	1.8(a)	
	$T_j = +150$ °C	–	1.05	1.3	–	1.1	1.5(a)	
	$I_O = 150$ mA, $T_j = +25$ °C TDF1607DP TDE1607DP	–	–	–	–	1.2	1.8	
	$T_j = +150$ °C TDF1607DP TDE1607DP	–	–	–	–	1.1	1.5	
I_{OL}	Low Level Output Current ($V_O = 0$, $V_{CC} = +24$ V)							
	$T_j = +25$ °C	–	–	–	–	0.01	10(a)	
	TDF1607DP TDE1607DP	–	–	–	–	–	100	
	$T_{min} \leq T_j \leq$ max	–	0.01	10	–	0.01	50(a)	
	TDF1607DP TDE1607DP	–	–	–	–	–	500	

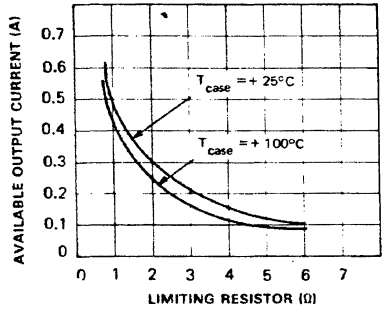
Notes : 1. For operating at high temperature, the TDF1607, TDE1607, TDE1747, TDE1647/A must be derated based on a + 150 C maximum junction temperature and a junction-ambient thermal resistance of 185 °C/W for Metal Can, 120 °C/W for Mini-dip and 100 °C/W for the SO14.
2. The offset voltage given is the maximum value of input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.

Available output current versus limiting resistor

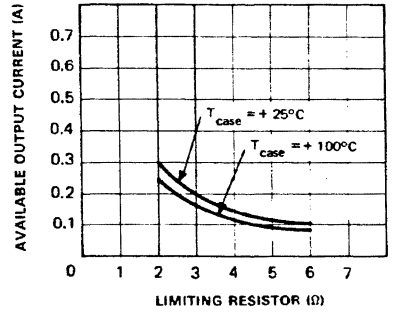
TDE1747



TDE1647,A - TDE1607 CM

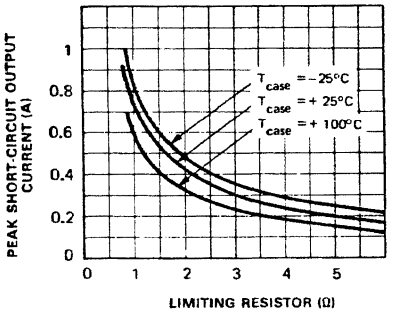


TDF1607 DP - TDE1607 DP

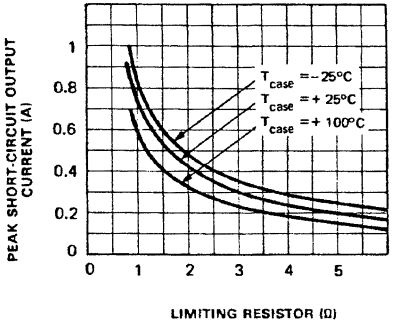


Peak short-circuit output current versus limiting resistor

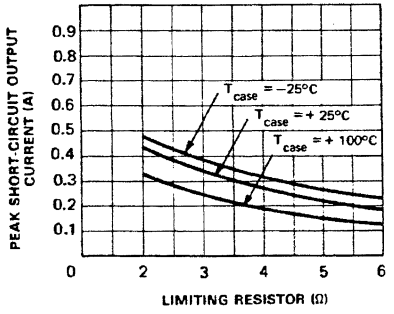
TDE1747



TDE1647,A - TDE1607 CM

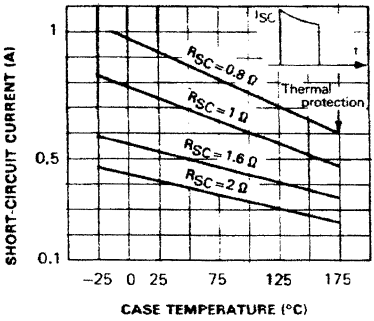


TDF1607 DP - TDE1607 DP

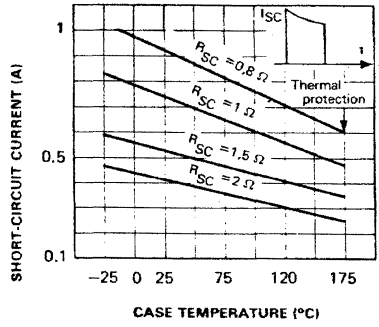


Short-circuit current versus case temperature

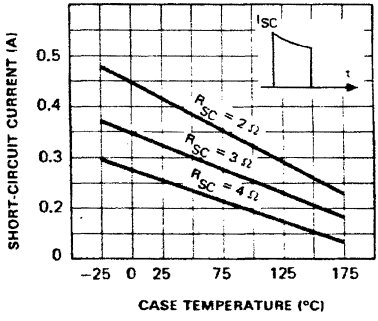
TDE1747



TDE1647,A - TDE1607 CM

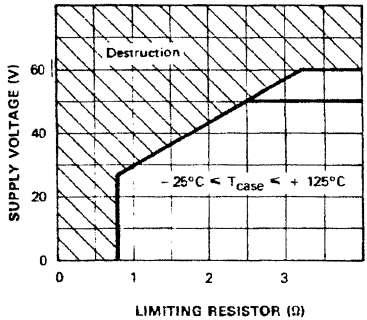


TDF1607 DP - TDE1607 DP

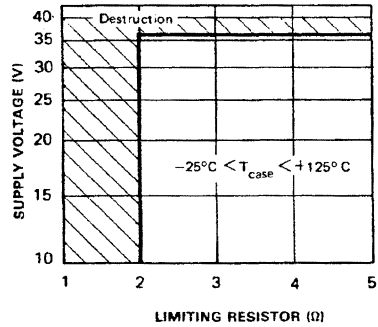


Mimimum limiting resistor value versus supply voltage

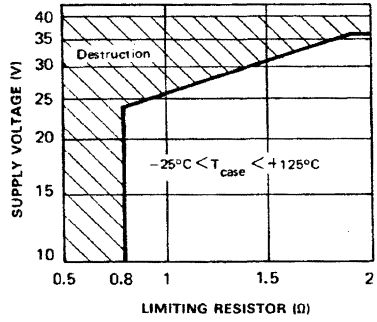
TDE1647,A - TDE1747



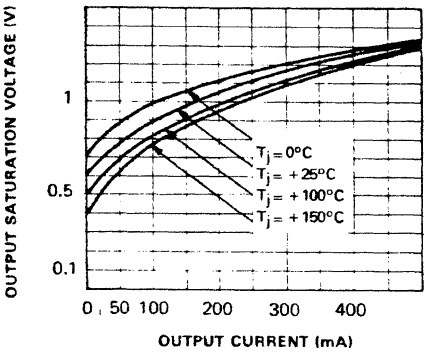
TDF1607 - TDE1607 DP



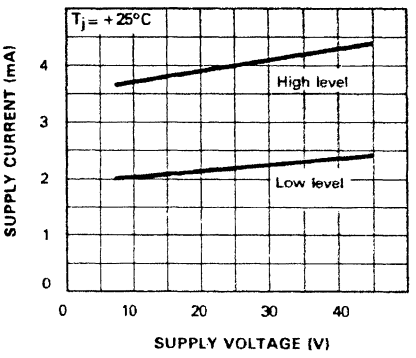
TDE1607 CM



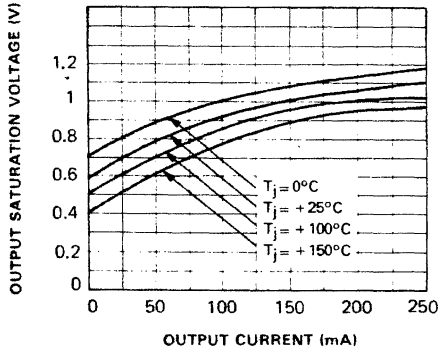
TDE1647,A - TDE1747 - TDE1607 CM



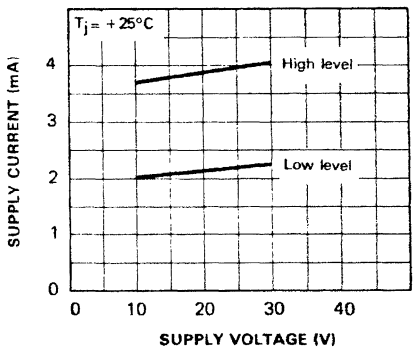
TDE1647,A - TDE1747



TDF1607 DP - TDE1607 DP

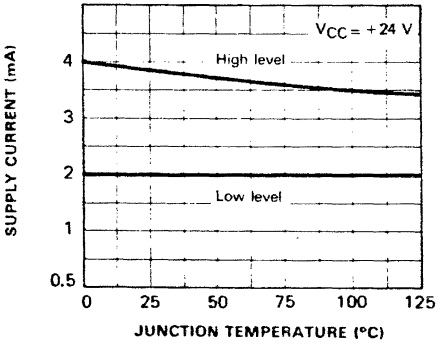


TDF1607 DP - TDE1607 DP



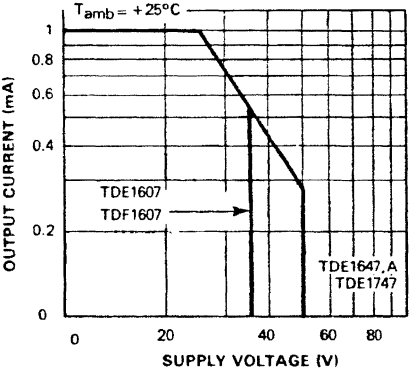
Supply current versus junction temperature

TDE1647,A - TDE1747 - TDE1607

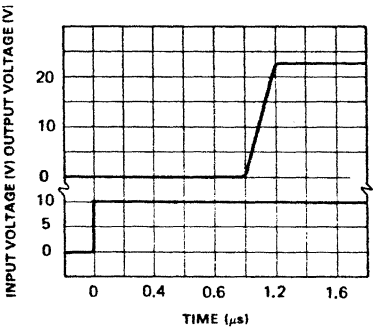


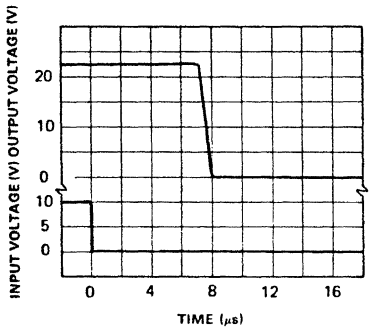
Safe operating area (non repetitive surge)

TDF1607 - TDE1607 - TDE1647,A - TDE1747

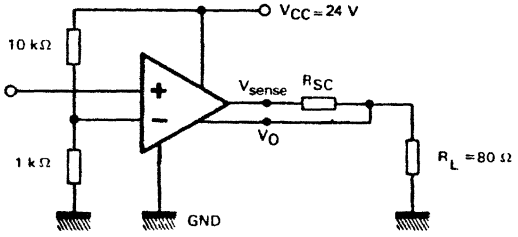


Response Time.





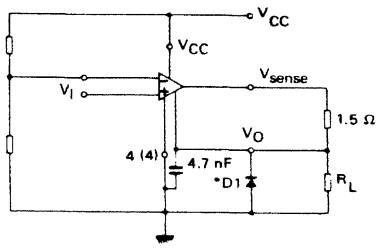
Test Circuit.



TYPICAL APPLICATIONS

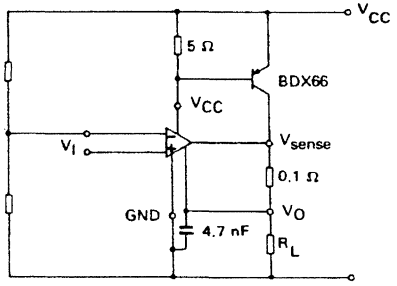
TDE1647, A - TDE1747.

Basic Circuit.

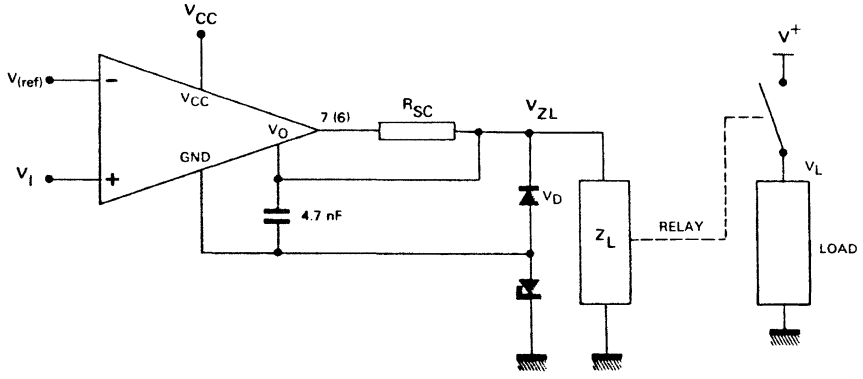


* D1 : required if inductive load.

Output Current Extension (5 A).

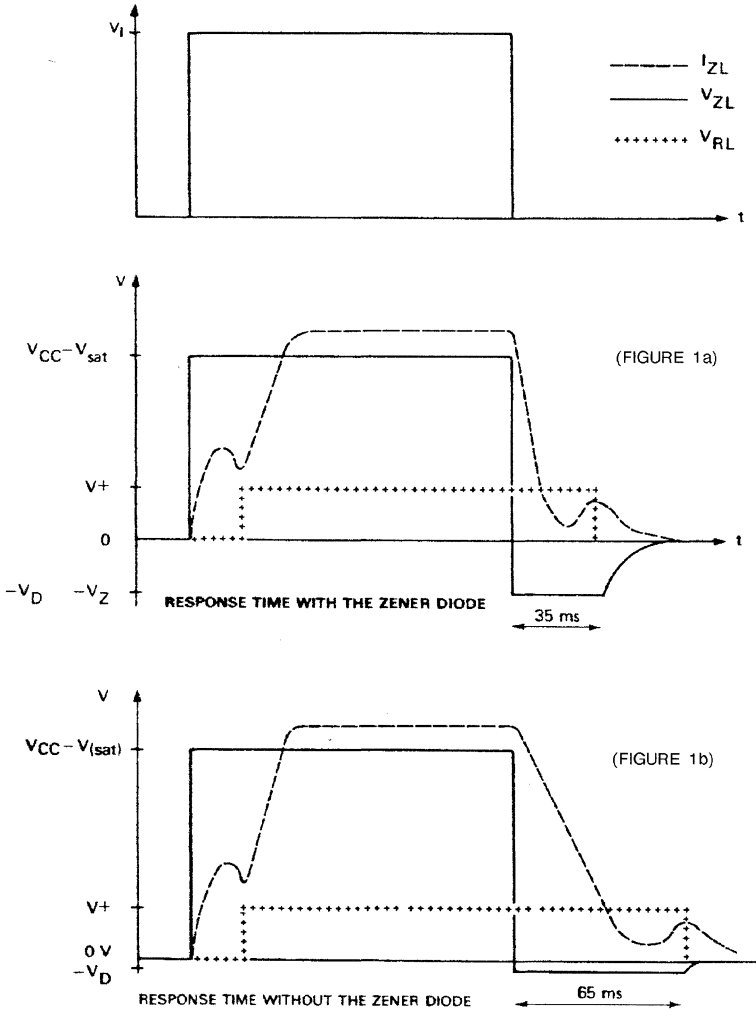


DRIVING LOW IMPEDANCE RELAYS (I_O = 300 mA)



The device in the above application operates at :
V_{CC} = + 45 V, I_O = 300 mA with a heatsink such that $R_{th(j-a)} \leq 80$ °C/W. The device supports an output voltage of $V_{CC} = V_Z$ during the current cut off time, which is decreased by the zener diode.
This voltage must be ≤ to the maximum supply voltage.

WAVEFORMS



Note : 1. In the case of the figure 1a, the TDE1647, A-CM can withstand + 60 V @ 400 mA for $t \leq 5$ µs.

INTERFACE CIRCUIT - RELAY AND LAMP-DRIVER

- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION
- THERMAL PROTECTION WITH HYSTERESIS TO AVOID THE INTERMEDIATE OUTPUT LEVELS
- LARGE SUPPLY VOLTAGE RANGE : + 8 V to + 45 V

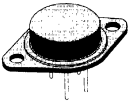
DESCRIPTION

The TDE1737-TDF1737 is a monolithic amplifier designed for high current and high voltage applications, specifically to drive lamps, relays and control of stepper motors.

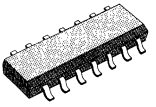
This device is essentially blow-out proof. Current limiting is available to limit the peak output current to a safe value, the adjustment only requires one external resistor. In addition, thermal shut down is provided to keep the I.C. from overheating. If internal dissipation becomes too great, the driver will shut down to prevent excessive heating.

The output is also protected against short-circuits with the positive power supply.

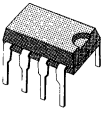
The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies down to the single + 12 V or + 24 used for industrial electronic systems.



METAL CAN
CM SUFFIX



SO-14 J
FP SUFFIX



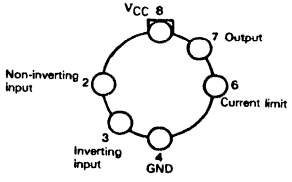
MINIDIP/2
DP SUFFIX

ORDER CODES

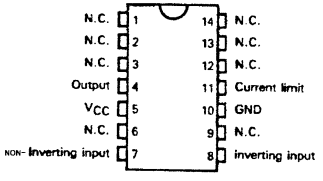
Part Number	Temperature Range	Package		
		CM	DP	FP
TDE1737	– 25 °C to + 85 °C	•	•	•
TDF1737	– 40 °C to + 85 °C		•	•
Example : TDE1737DP				

PIN CONNECTION (top views)

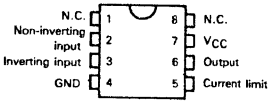
METAL CAN



SO-14



MINIDIP



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_s	Supply Voltage		50	V
V_I	Input Voltage		50	V
V_{ID}	Differential Input Voltage		50	V
I_O	Output Current		1000	mA
P_{tot}	Power Dissipation		Internally Limited	W
T_{oper}	Operating Free–air Temperature Range	TDE1737	– 25 to + 85	°C
T_{oper}	Operating Free–air Temperature Range	TDF1737	– 40 to + 85	°C
T_{stg}	Storage Temperature Range		– 65 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	METAL CAN MINIDIP	45 50	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	METAL CAN MINIDIP	185 120	°C/W
	Junction-ceramic Substrate (case glued to substrate)	SO14	90	°C/W
	Junction–ceramic Substrate (case glued to substrate, substrate temperature maintened constant)	SO14	65	°C/W

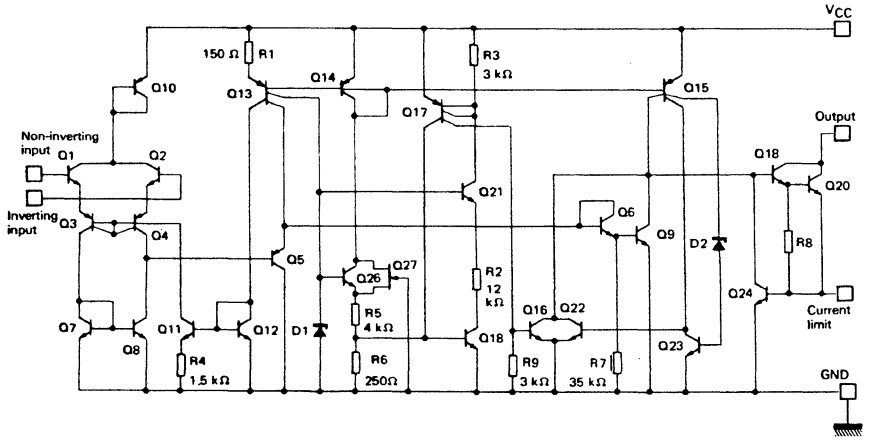
ELECTRICAL CHARACTERISTICS

TDE1737 – 25 °C ≤ T_{amb} ≤ + 85 °C, + 8 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 300 mA, T_j ≤ + 150 °C
(unless otherwise specified)
TDF1737 – 40 °C ≤ T_{amb} ≤ + 85 °C, + 8 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 300 mA, T_j ≤ 150 °C

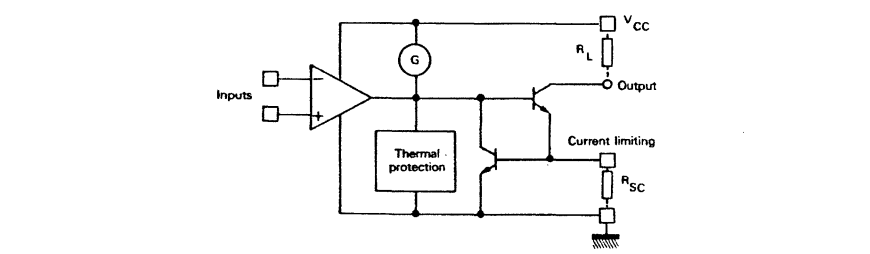
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage - (note 1)	–	2	50	mV
I_{IB}	Input Bias Current	–	0.1	1.5	µA
I_{CC}	Supply Current (V_{CC} = + 24 V, I_O = 0)	–	3	5	mA
V_{CM}	Common-mode Input Voltage Range	2	–	V_{CC}–2	V
I_{SC}	Short-circuit Current Limit (R_{SC} = 1.5 Ω, T_{case} = + 25 °C)	–	500	–	mA
V_{CC}–V_O	Output Saturation Voltage (output low) ($V_I^+ - V_I^- \geq 50$ mV I_O = 300 mA, R_{SC} = 0)	–	1	1.5	V
I_{OL}	Output Leakage Current (output high) ($V_O = V_{CC}$ = + 24 V, T_{amb} = + 25 °C)	–	–	10	µA

Notes : 1. The offset voltage given is the maximum value of input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.
2. Devices bonded on a 40 cm^2 glass-epoxy printed circuit 0.15 cm thick with 4 cm^2 of cooper.

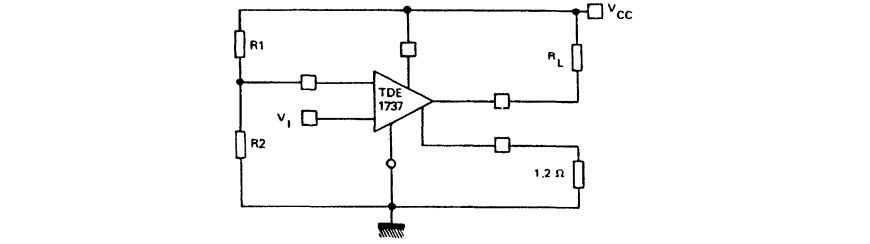
SCHEMATIC DIAGRAM



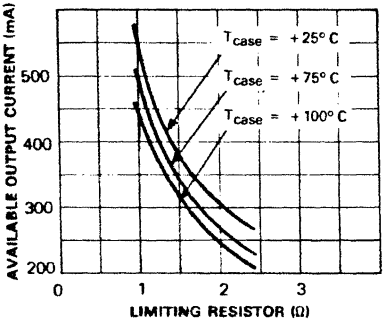
SIMPLIFIED SCHEMATIC



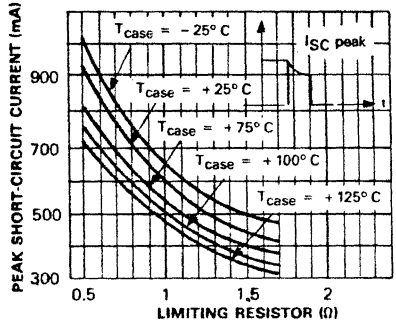
TYPICAL APPLICATION -



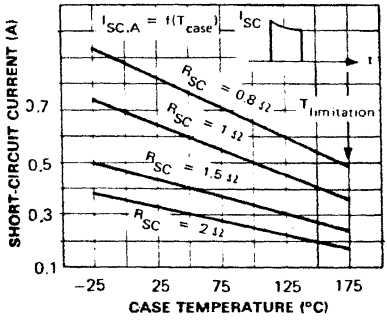
Available output current versus limiting resistors



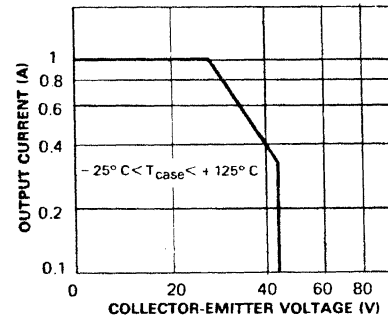
Peak short-circuit current versus limiting resistor



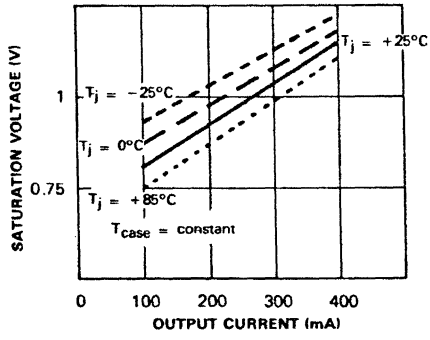
Short-circuit current versus case temperature



Safe operating area (non repetitive overload)



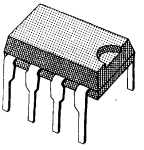
Saturation voltage versus output current



INTERFACE CIRCUIT (RELAY AND LAMP-DRIVER)

- OPEN GROUND PROTECTION
- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION
- INTERNAL THERMAL PROTECTION WITH EXTERNAL RESET
- LARGE SUPPLY VOLTAGE RANGE
- ALARM OUTPUT
- INPUT VOLTAGE CAN BE HIGHER THAN V_{CC}
- OUTPUT VOLTAGE CAN BE LOWER THAN GROUND ($V_{CC} - V_O \leq V_{CC}$ [max])

MINIDIP/2



ORDER CODES : TDE1767 DP
TDE1767 ADP
TDE1787 DP
TDE1787 ADP

DESCRIPTION

The TDE1767,A/TDE1787,A are monolithic amplifiers designed for high current and high voltage applications, specifically to drive lamps, relays, stepping motors.

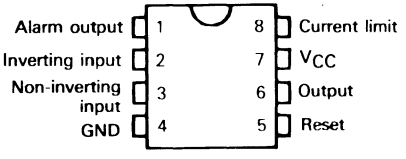
These devices are essentially blow-out proof. The output is protected from short-circuits with the positive supply or ground. In addition thermal shut down is provided to keep the IC from overheating. If internal dissipation becomes too high, the driver will shut down to prevent excessive heating. The output stays null after the overheating is off, if the reset input is low. If high the output will alternatively switch-on and off until the overload is removed.

The device operates over a wide range of supply voltages from standard 15 V operational amplifier supplies to the single + 6 V or + 48 V used for industrial electronic systems. Input voltages can be higher than the V_{CC}.

An alarm output suitable for driving a LED is provided. This LED, normally on (if referred to ground), will die out or flash during an overload depending on the state of the reset input.

The output is low in open ground conditions.

PIN CONNECTION (top view)



THERMAL DATA

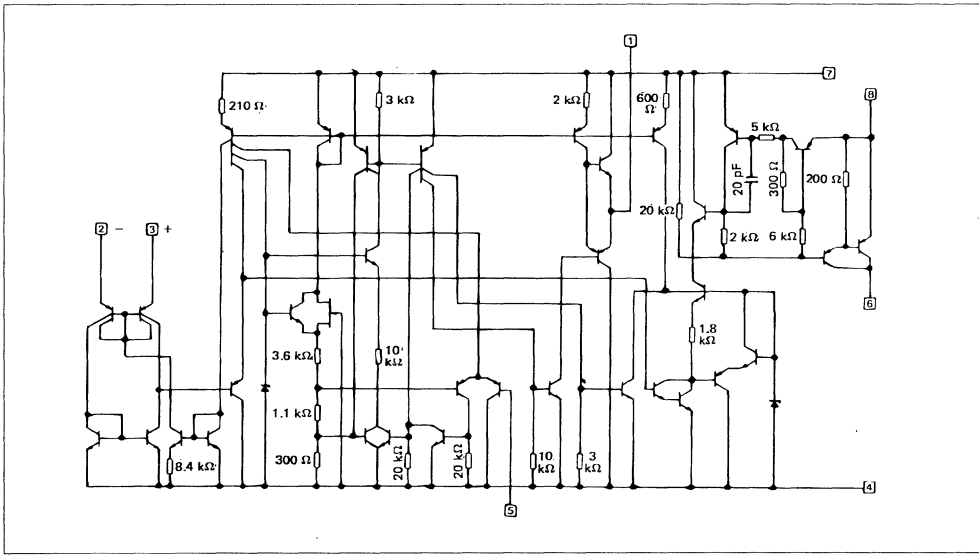
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	30	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance*	80	°C/W

* Devices bonded on a 40 cm2 glass-epoxy printed circuit 0.15 cm thick with 4 cm2 of copper.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	TDE1767A/TDE1787A	TDE1767/TDE1787	Unit
V_{CC}	Supply Voltage	60	50	V
V_{ID}	Input Differential Voltage	60	50	V
V_I	Input Voltage	– 10 to + 60	– 10 to + 50	V
I_O	Output Current	1.2	1.2	A
$V_{I(reset)}$	Reset Input Voltage	– 0.5 to + 60	– 0.5 to + 50	V
I_{OA}	Alarm Output Current	– 10 to + 20	– 10 to + 20	mA
P_{tot}	Power Dissipation	Internally Limited		mW
T_{oper}	Operating Ambient Temperature Range	– 25 to + 85	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	– 65 to + 150	°C

SCHEMATIC DIAGRAM



EQUIVALENT SCHEMATIC

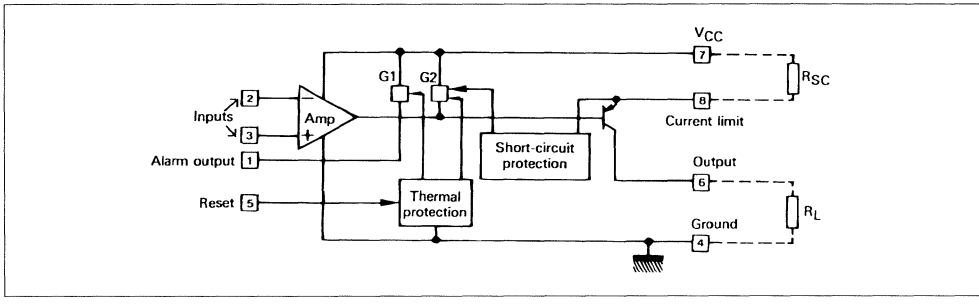
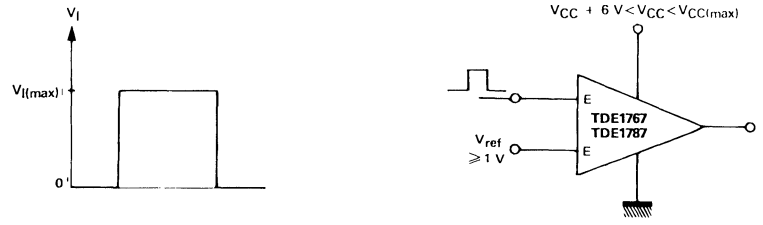


Figure 1.



The reference input can be the inverting or non-inverting one.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)
TDE1767A : – 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 60 V, I_O ≤ 500 mA, T_j ≤ + 150 °C
TDE1767 : – 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 500 mA, T_j ≤ + 150 °C
TDE1787A : – 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 60 V, I_O ≤ 300 mA, T_j ≤ + 150 °C
TDE1787A : – 25 °C ≤ T_{amb} ≤ + 85 °C, + 6 V ≤ V_{CC} ≤ + 45 V, I_O ≤ 300 mA, T_j ≤ + 150 °C

Symbol	Parameter		Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage - (note 1)		–	2	50	mV
I_{CC}	Power Supply Current (measured on pin 4)					mA
	Output High (T_{amb} = + 25 °C)		–	5.8	8	
	Output High (V_{CC} = $V_{CC\ (max)}$, T_j = + 150 °C)		–	5	7	
	Output Low (V_{CC} = $V_{CC\ (max)}$, T_{amb} = + 25 °C)		–	1.5	4	
I_{IB}	Input Bias Current		–	15	100	µA
V_{CM}	Common-mode Input Voltage Range					V
	(note 2)	**TDE1787A, TDE1767A**	1	–	60	
		TDE1787, TDE1767	1	–	45	
V_I	Input Voltage Range (V_{ref} ≥ + 1 V)					V
	(figure 1, note 2)	**TDE1787A, TDE1767A**	0	–	60	
		TDE1787, TDE1767	0	–	45	
I_{SC}	Short-circuit Output Current					mA
	(V_{CC} = + 35 V, t = 10ms)					
	R_{SC} = 0.18 Ω	**TDE1767A**	–	700	–	
	R_{SC} = 0.33 Ω	**TDE1787A**	–	380	–	
V_{sense}	Current Limit Sense Voltage : V_O = V_{CC} – 2 V, t = 10 ms		140	150	175	mV
	(V_O = V_{CC} – 2 V) : V_O = 0 V, t = 10 ms		130	140	165	
$V_{O(sat)}$	Output Saturation Voltage (output high $V_I^+ - V_I^- \geq 50$ mV,					V
	R_{SC} = 0, V_{CC} = + 30 V)					
	T_j = + 25 °C	**TDE1787A, TDE1767A**	–	1	1.1	
		TDE1787, TDE1767	–	1	1.2	
	T_j = + 150 °C	**TDE1787A, TDE1767A**	–	1.1	1.2	
		TDE1787, TDE1767	–	1.1	1.3	
I_{OL}	Output Leakage Current (output low)		–	–	100	µA
I_A	Available Alarm Output Current					mA
	Output Source Current (V_{AH} = V_{CC} – 2.5 V)		– 4	– 5	–	
	Output SInk Current (in thermal shut-down) V_A = 1.4 V		5	10	–	
I_{reset}	Reset Input Current		–	2	40	µA
$V_{th\ (reset)}$	Reset Threshold		–	1.4	–	V
–	Output Leakage Current (open ground)		–	10	–	µA

Notes : 1. The offset voltage given is the maximum value of differential input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.
2. Input voltage range is independent of the supply voltage.

Fig. 2 – PEAK SHORT-CIRCUIT CURRENT vs LIMITING RESISTOR.

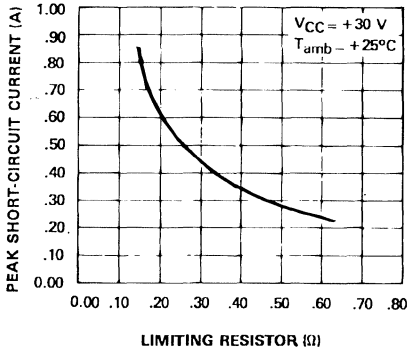


Fig. 3 – AVAILABLE OUTPUT CURRENT vs LIMITING RESISTOR.

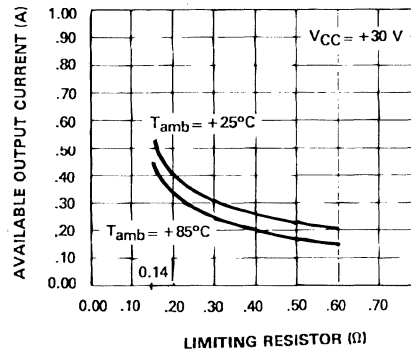


Fig. 4 – POWER SUPPLY CURRENT (pin 4).

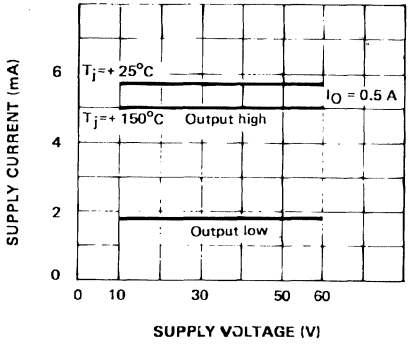


Fig. 5 – OUTPUT SATURATION VOLTAGE vs OUTPUT CURRENT.

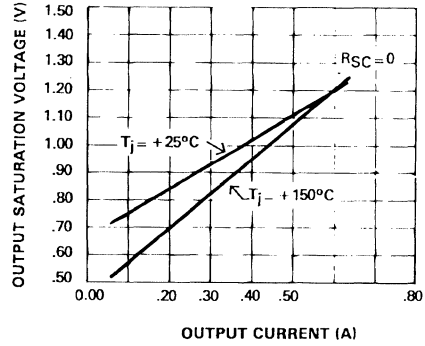


Fig. 6 – OUTPUT TRANSISTOR SAFE OPERATING AREA (pulsed).

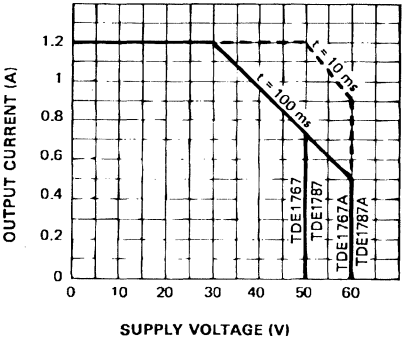
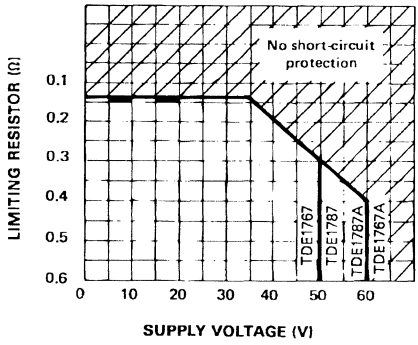


Fig. 7 – NORMAL OPERATING AREA (short-circuit protected).



ALARM OUTPUT CAPABILITY CURRENT

Fig. 8 CURRENT SINKING.

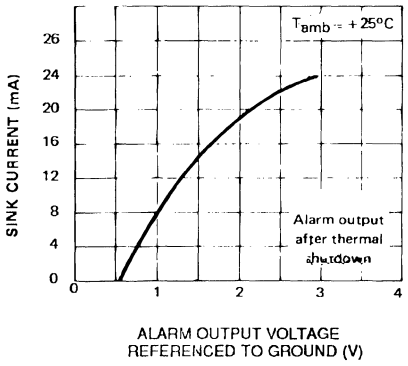


Fig. 9 – CURRENT SOURCING

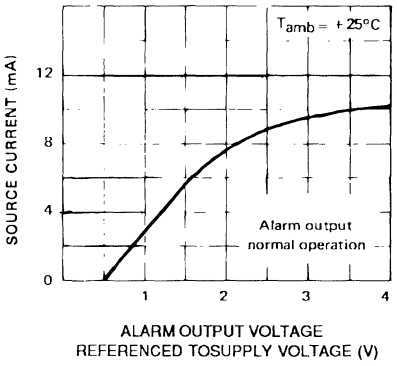


Fig. 10 – RESPONSE TIME.

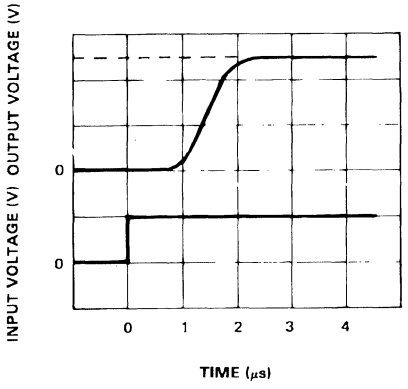


Fig. 11 – RESPONSE TIME.

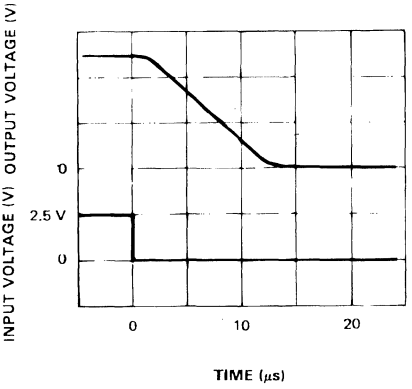
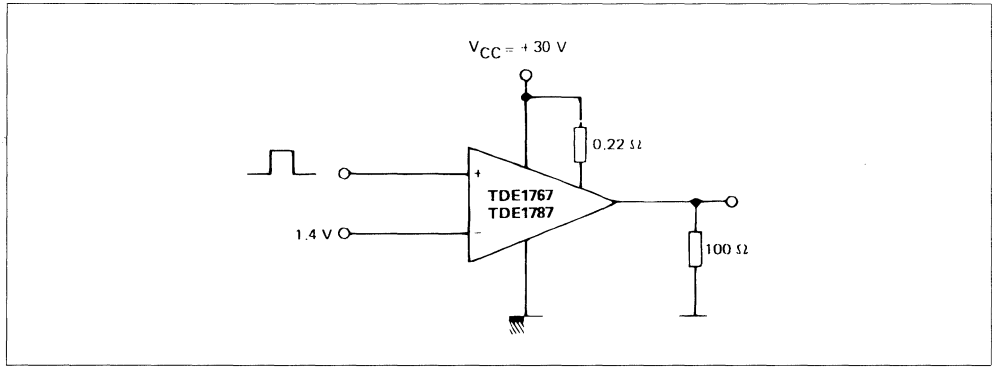


Figure 12 : Test Circuit.



TYPICAL APPLICATIONS

Figure 13 : Open Load Detection.

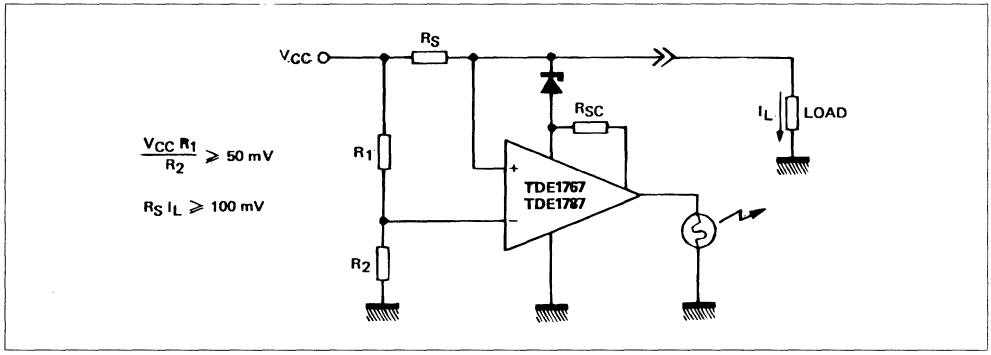


Figure 14 : Driving Lamps, Relays, Etc...

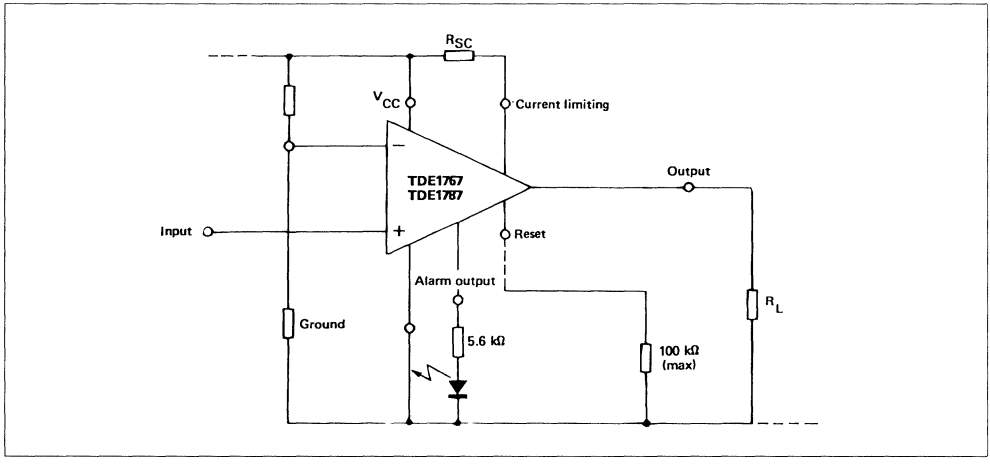


Figure 15 : Common Reset.

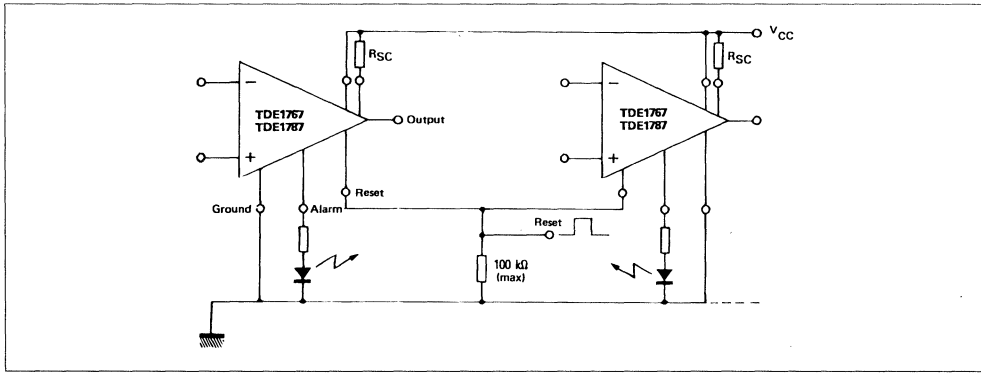
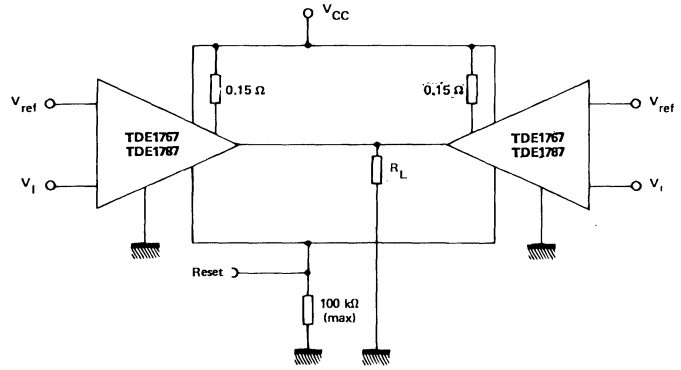


Figure 16 : Parallel Driving of Loads Up to 1 A.



USING ALARM OUTPUT

Figure 17 : Parallel Alarm Outputs.

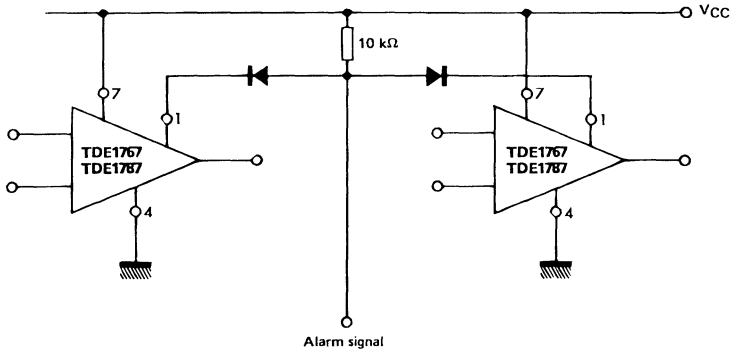


Figure 18 : Led to VCC.

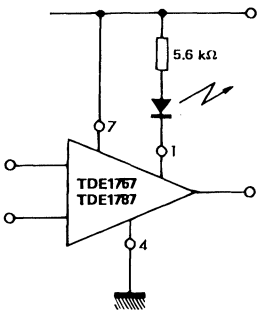


Figure 19 : Led to Ground.

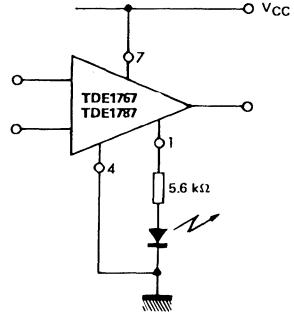


Figure 20 : Interface between High Voltage and Low Voltage Systems.

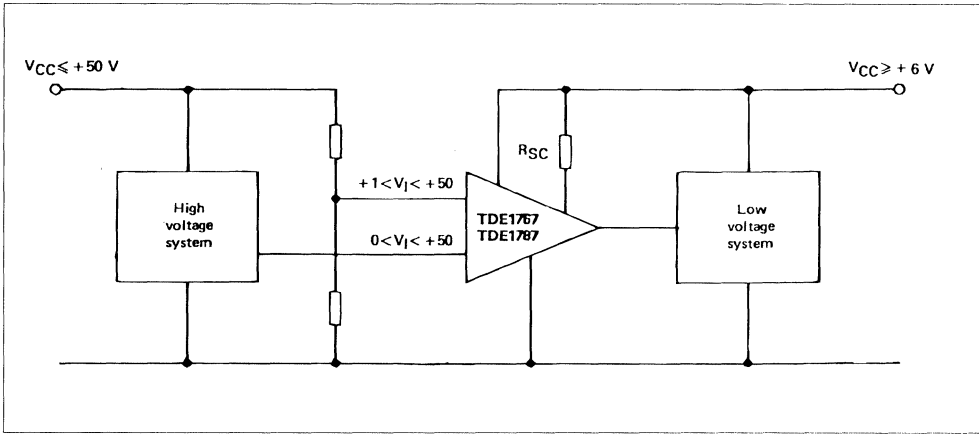
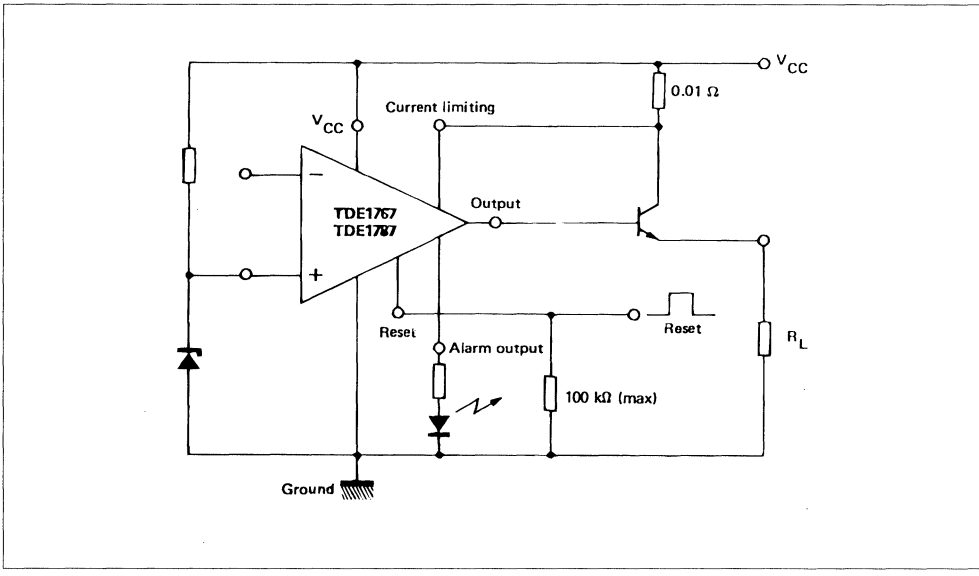


Figure 21 : Increasing Output Current Up to 10 A.



0.5 A INTELLIGENT POWER SWITCH

- HIGH OUTPUT CURRENT 500 mA
- SHORT-CIRCUIT PROTECTION UP TO V_{CC} = + 35 V
- INTERNAL THERMAL PROTECTION WITH EXTERNAL RESET AND SYNCHRONIZATION CAPABILITY
- OPEN GROUND PROTECTION
- OUTPUT VOLTAGE CAN BE LOWER THAN GROUND FOR FAST INDUCTIVE LOAD DE-MAGNETIZATION
- DIFFERENTIAL INPUTS FOR ANY LOGIC SYSTEM COMPATIBILITY
- INPUT VOLTAGE CAN BE HIGHER THAN V_{CC}
- LARGE SUPPLY VOLTAGE RANGE FROM 6 V TO 35 V
- SINK AND SOURCE ALARM OUTPUTS
- NO NEED EXTERNAL CLAMPING DIODE FOR DEMAGNETIZATION ENERGY UP TO 150 mJ
- SEVERAL DEVICES CAN BE CONNECTED IN PARALLEL

DESCRIPTION

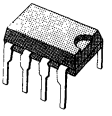
The TDE1798/TDF1798 is an interface circuit delivering high currents and capable of driving any type of loads.

This device is essentially blow out proof. The output is protected from short-circuits with the positive supply or ground. In addition thermal shut down is provided to keep the IC from overheating. If internal dissipation becomes too high, the driver will shut down to prevent excessive heating. The output stays null after the overload is off, if the reset input is low. If high the output will alternatively switch on and off until the overload is removed.

Higher current can be obtained by paralleling the outputs of several devices. In this case, the devices can be reactivated simultaneously after an overload if their reset input are connected in parallel.

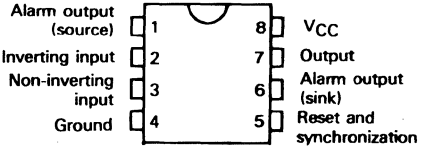
The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies to the single + 6 V or + 35 V used for industrial electronic systems. Input voltage can be higher than the V_{CC}. The output is low in open ground conditions.

MINIDIP/2

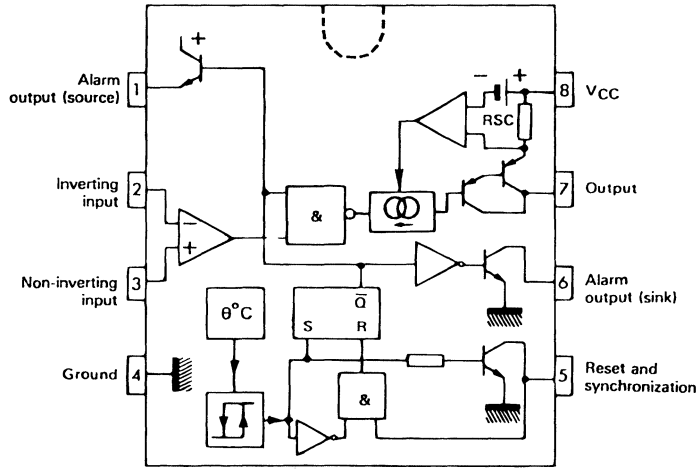


ORDER CODES : TDE1798DP

PIN CONNECTIONS (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		50	V
V_{ID}	Input Differential Voltage		50	V
V_I	Input Voltage		− 30 to + 50	V
$V_{I(reset)}$	Reset Input Voltage		V_{CC} − 50 V to V_{CC}	V
I_O	Output Current		Internally Limited	A
P_{tot}	Power Dissipation		Internally Limited	mW
	Reset Input Sink Current (in thermal shut-down)		15	mA
W_D	Repetitive Maximum Demagnetization Energy 10^6 Operations		150	mJ
T_{oper}	Operating Ambient Temperature Range	TDE1798DP TDF1798DP	− 25 to + 85 − 40 to + 85	°C
T_{stg}	Storage Temperature Range		− 65 to + 150	°C
$I_{A(sink)}$	Alarm Output Sink Current		25	mA
$I_{A(source)}$	Alarm Output Source Current		12	mA

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{th\ (j-c)}$	Maximum Junction-case Thermal Resistance (note 1)	30	°C/W
$R_{th\ (j-a)}$	Maximum Junction-ambient Thermal Resistance (note 1)	70	°C/W

Note : 1. Devices bounded on 40 cm^2 glass-epoxy printed circuit 0.15 cm thick with 4 cm^2 of copper.

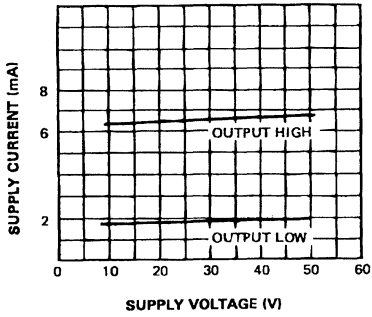
ELECTRICAL CHARACTERISTICS (note 2)

TDE – 25 °C ≤ T_j ≤ + 85 °C, 6 V ≤ V_{CC} ≤ + 35 V, I_O ≤ 500 mA, T_j ≤ + 150 °C (unless otherwise specified)
TDF – 40 °C ≤ T_j ≤ 85 °C, 6 V ≤ V_{CC} < 35 V, I_O ≤ 500 mA, T_j ≤ 150 °C

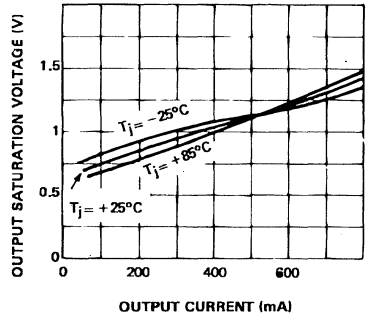
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage (note 3)	–	2	50	mV
I_{CC}	Power Supply Current Output High (T_{amb} = + 25 °C, I_O = 500 mA) Output Low	– –	6.5 2	8 4	mA
I_{IB}	Input Bias Current	–	15	40	µA
V_{ICR}	Common-mode Input Voltage Range (note 4)	1	–	45	V
V_I	Input Voltage Range (V_{ref} > + 1 V, note 4 and 5)	– 25	–	45	V
I_{SC}	Short-circuit Output Current (V_{CC} = 30 V, t = 10 ms)	0.7	0.9	1.3	A
$V_{CC} - V_O$	Output Saturation Voltage I_O = 500 mA ($\lvert V^+ I - V^- I \rvert$ > 50 mV)	–	1	1.25	V
I_{OL}	Output Low Leakage Current T_j = + 85 °C (V_{CC} = 30 V, V_O = 0 V)	–	10	100	µA
$I_{(pin\ 1)source}$ $I_{(pin\ 6)sink}$	Available Alarm Output Current Output Source Current (V (pin 1) = VCC – 2.5 V) Output Sink Current (in thermal shut-down), V (pin 6) = 2 V	 4 6	 8 15	 – –	mA
 I_{RH} I_{RL}	Reset Input Current	 – – 1	 15 0	 40 – 1	µA
$V_{th\ (reset)}$	Reset Threshold	0.8	1.4	2	V
I_{reset}	Reset Output Sink Current (in thermal shut-down) for V_{reset} ≤ + 0.8 V	2	–	–	mA
$I_{OL(open\ GND)}$	Output Leakage Current (open ground)	–	10	100	µA
V_{BRVEO}	Output Transistor Avalanche Voltage ($V_{CC} - V_O$)	65	–	110	V

Notes : 2. For operating at high temperature, the TDE1798 and TDF1798 must be derated based on a – 150 °C maximum junction temperature and a junction-ambient thermal resistance of 70 °C/W.
3. The offset voltage given is the maximum value of input differential voltage required to drive the output voltage within 2 V of the ground or the supply voltage.
4. Input voltage range is independent of the supply voltage.
5. The reference input can be the inverting or the non-inverting one.

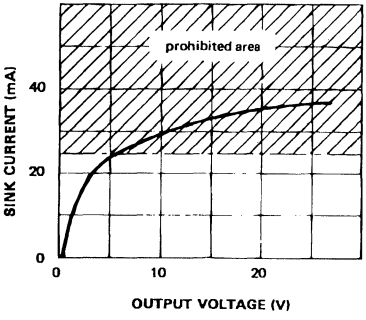
POWER SUPPLY CURRENT.



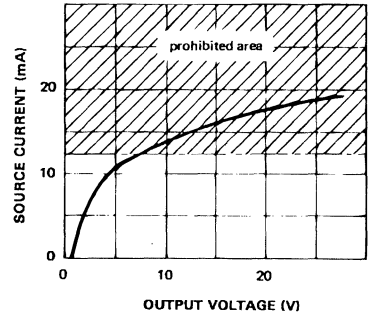
OUTPUT SATURATION VOLTAGE.



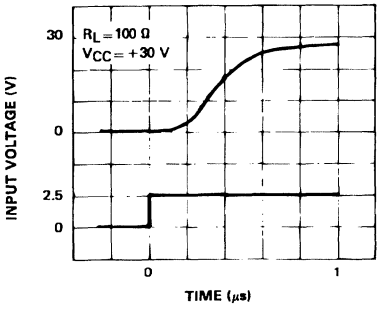
ALARM OUTPUT CURRENT SINK
(after thermal shut down).

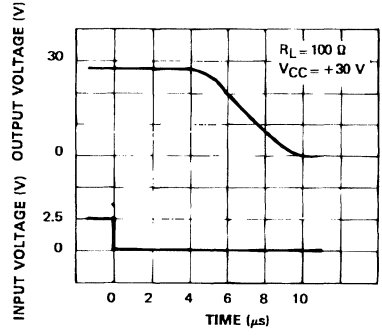


ALARM OUTPUT CURRENT SOURCE
(normal operation).



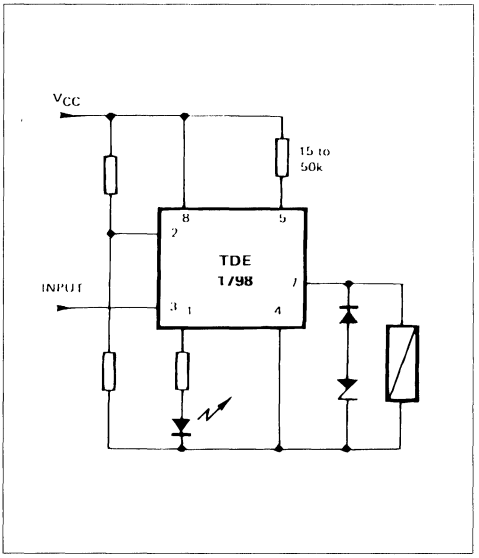
RESPONSE TIME.



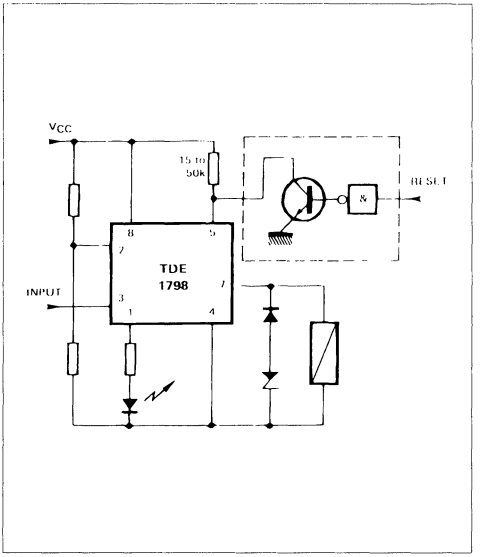


TYPICAL APPLICATIONS

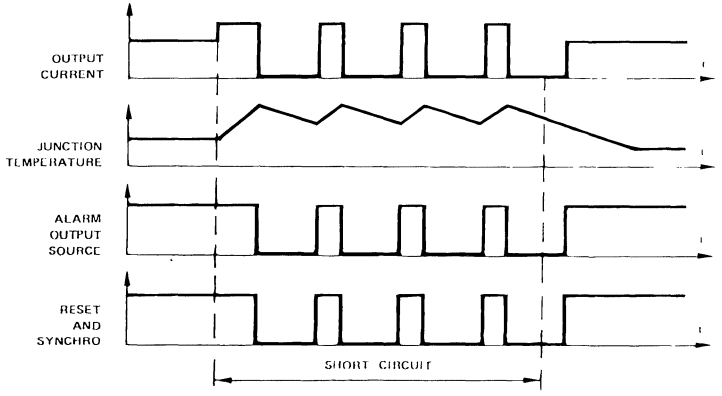
TYPICAL APPLICATION AUTOMATIC RESET



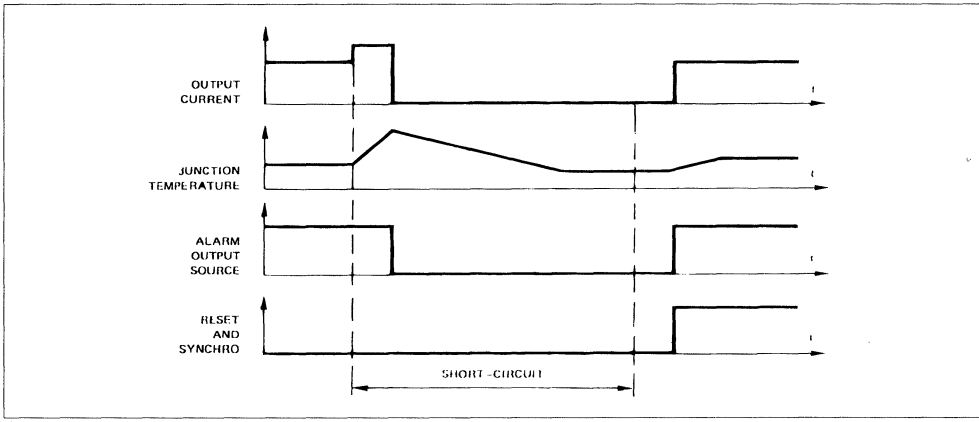
TYPICAL APPLICATION CONTROLLED RESET



SHORT CIRCUIT CONDITIONS WITH AUTOMATIC RESET



SHORT CIRCUIT CONDITIONS WITH CONTROLLED RESET



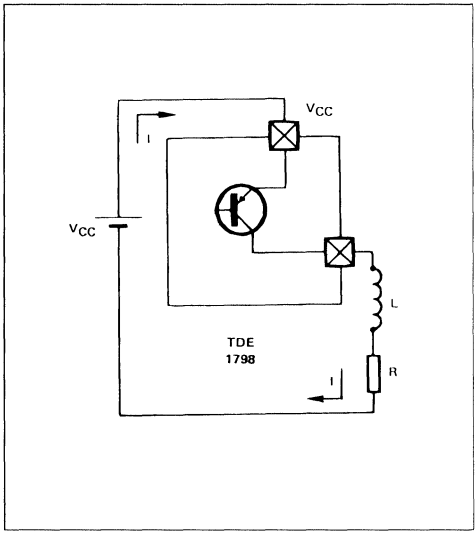
DEMAGNETIZATION OF INDUCTIVE LOADS WITHOUT EXTERNAL CLAMPING DEVICES.

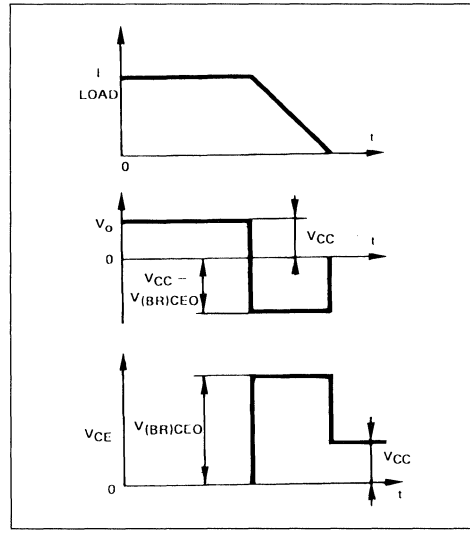
With no external clamping device, the energy of demagnetization is dissipated in the TDE1798 output stage, and the clamping voltage is the collector - emitter breakdown voltage $V_{(BR)\,CEO}$.

This method provides a very fast demagnetization of inductive loads and can be used up to 150 mJ.

The amount of energy W dissipated in the output stage during a demagnetization is :

$$W = V_{(BR)} \frac{L}{R} \left(I_O - \frac{V_{(BR)} - V_{CC}}{R} \text{Log} \left(1 + \frac{V_{CC}}{V_{(BR)} - V_{CC}} \right) \right)$$



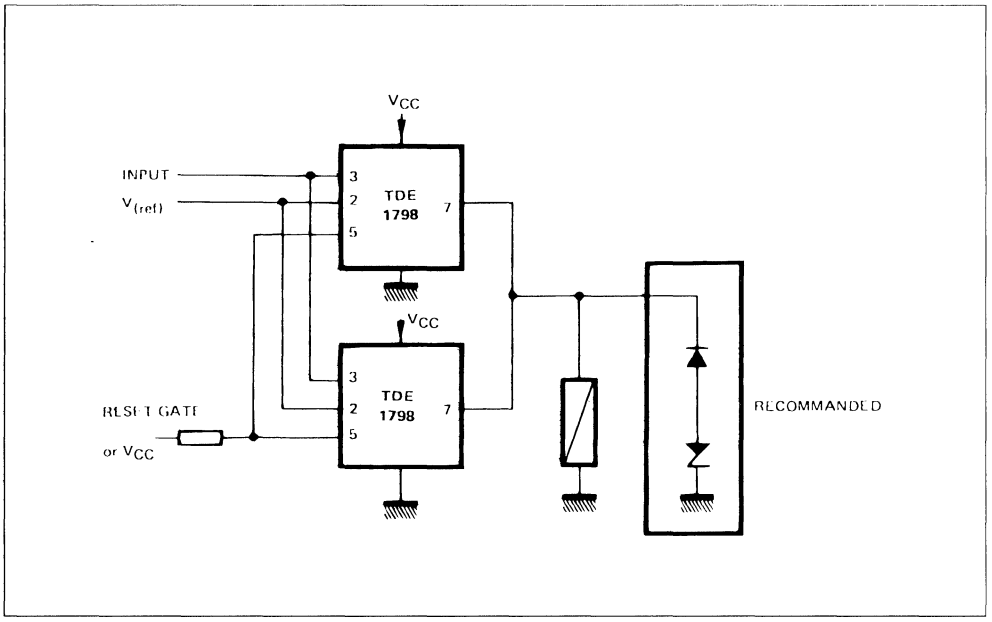


Remark 1 : This energy is dissipated inside the case, then must be included in the whole power dissipation.

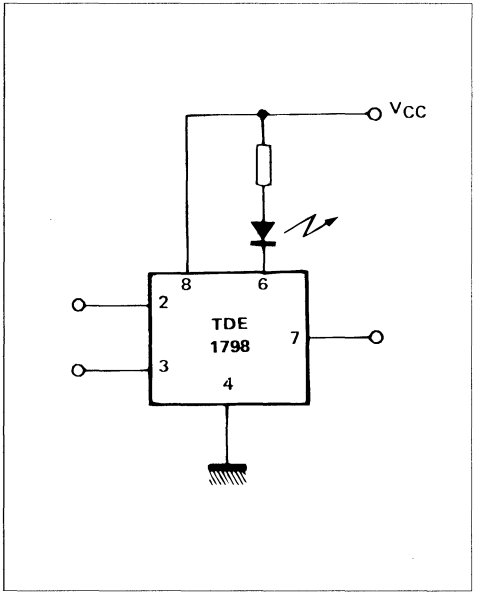
Remark 2 : The use of external clamping devices is recommended in case of parallel driving of loads.

The dispersion of the collector-emitter breakdown voltage V(BR) would induce the circuit with the lowest V(BR) to dissipate the whole demagnetization energy (which is roughly proportionnal to I_O^2).

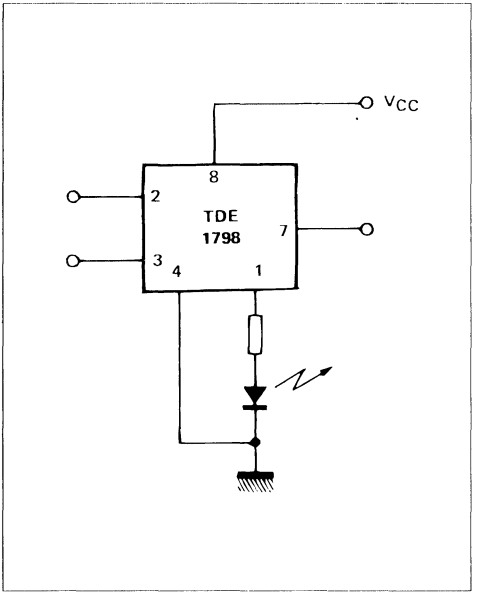
A 1 AMP. DRIVER (reset may be either automatic or controlled)



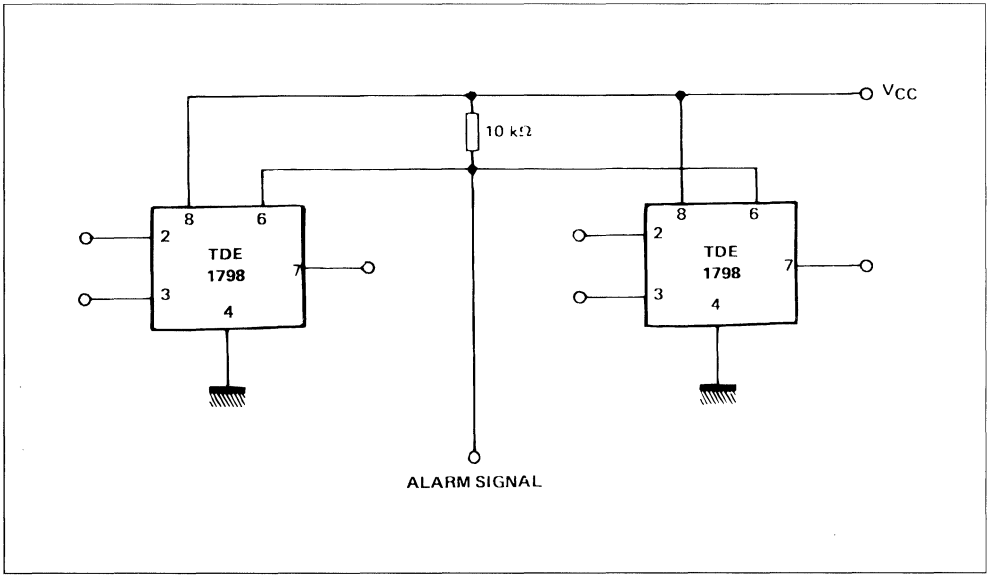
ALARM OUTPUT SINK



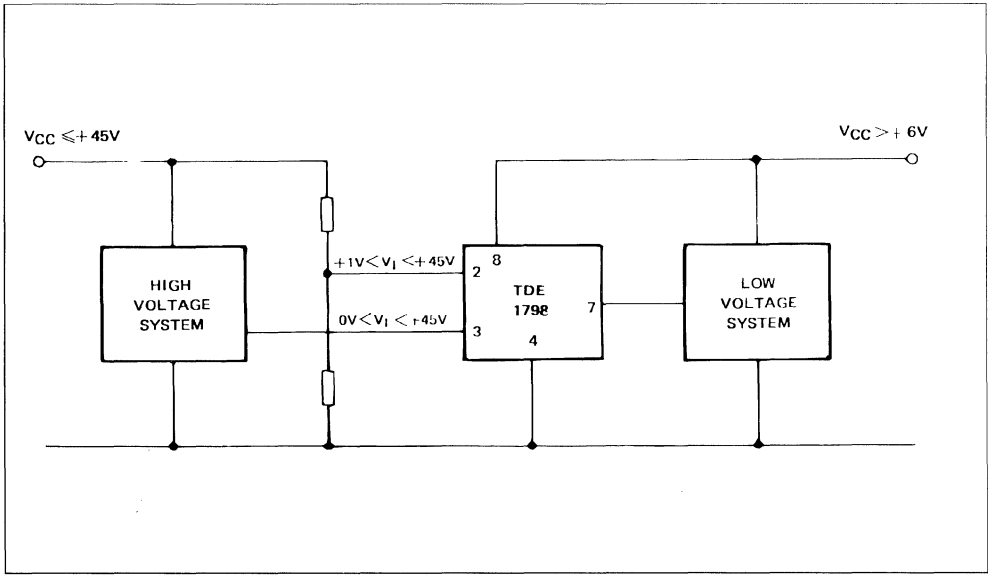
ALARM OUTPUT SOURCE



PARALLEL ALARM OUTPUTS



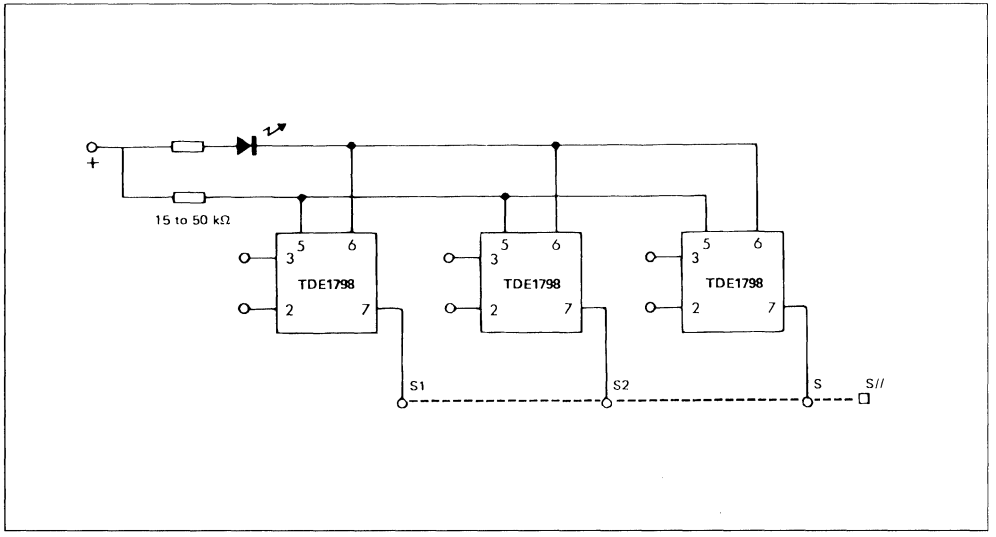
INTERFACE BETWEEN HIGH VOLTAGE AND LOW VOLTAGE SYSTEM



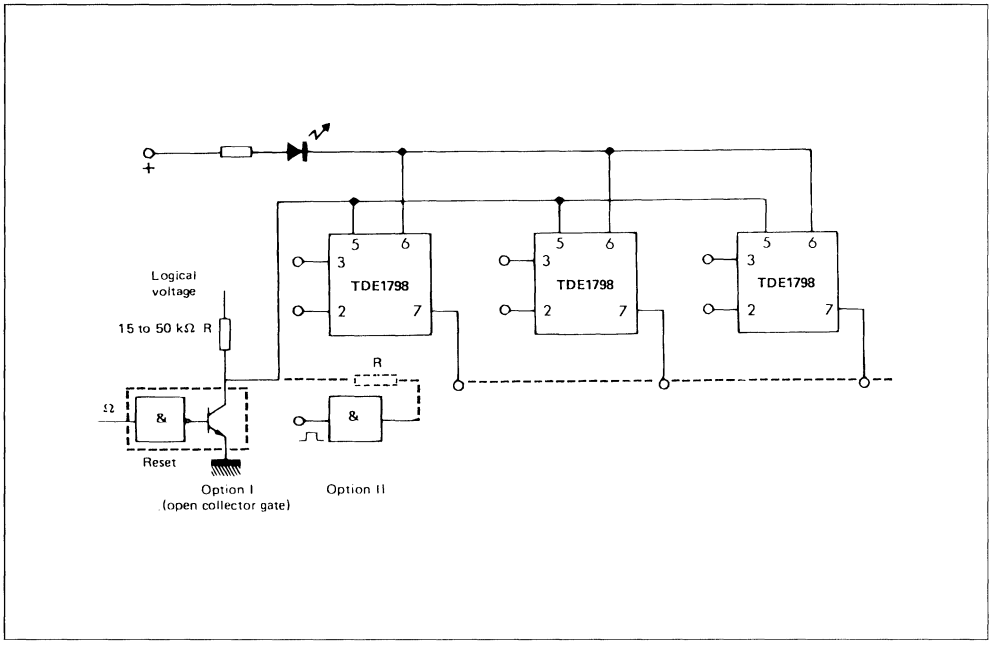
RESET AND SYNCHRONIZATION

Recommended diagram when the outputs are in parallel. After thermal disjunction a restart is possible when all the circuits are returned in operating conditions.

SYNCHRONOUS AUTOMATIC RESET (parallel or independent outputs)



SYNCHRONOUS CONTROLLED RESET (parallel or independent outputs)

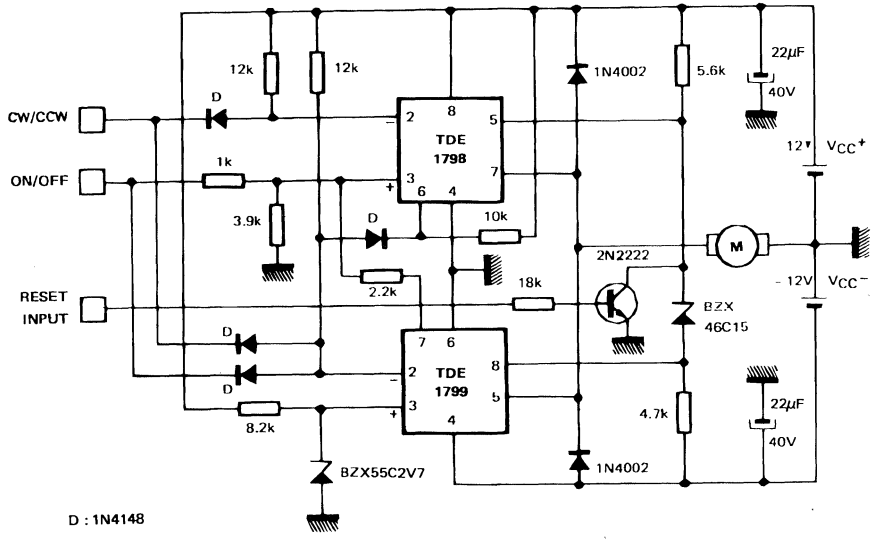


TWO QUADRANTS D.C. MOTOR DRIVE

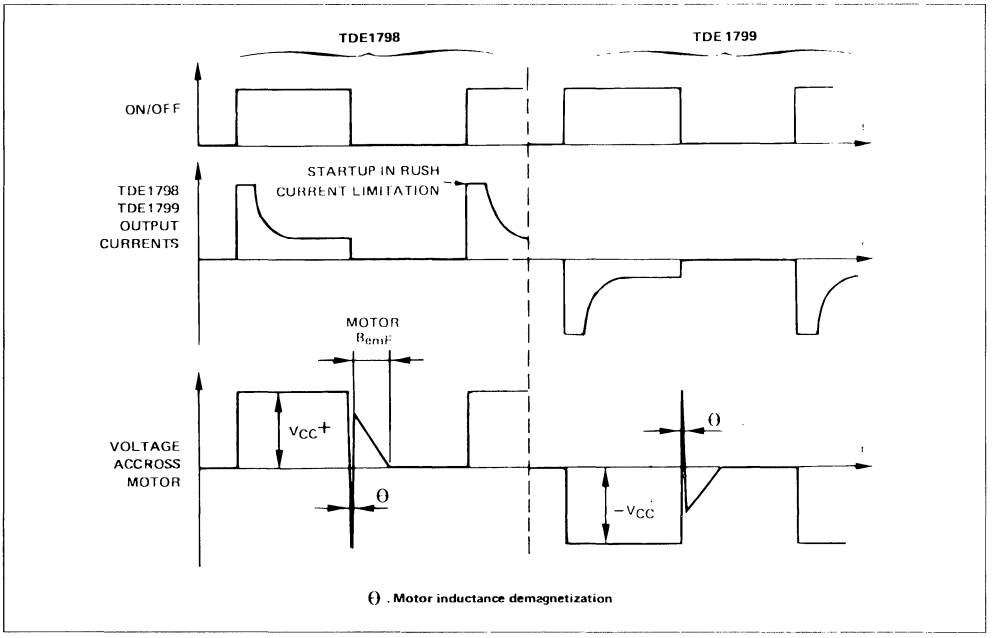
MAIN FEATURES

- $V_{CC} - V_{CC} \leq 50$ V
- Maximum output current 0.5 A
- Full protection against overloads and short-circuits
- No need of deadtime during rotation reversing
- TTL compatible inputs
- TDE1799 and TDE1798 input signals have the same reference
- No automatic restart after disjunction

CW/CCW	ON OFF	1798	1799
0	0	OFF	OFF
0	1	ON	OFF
1	1	OFF	ON
1	0	OFF	OFF

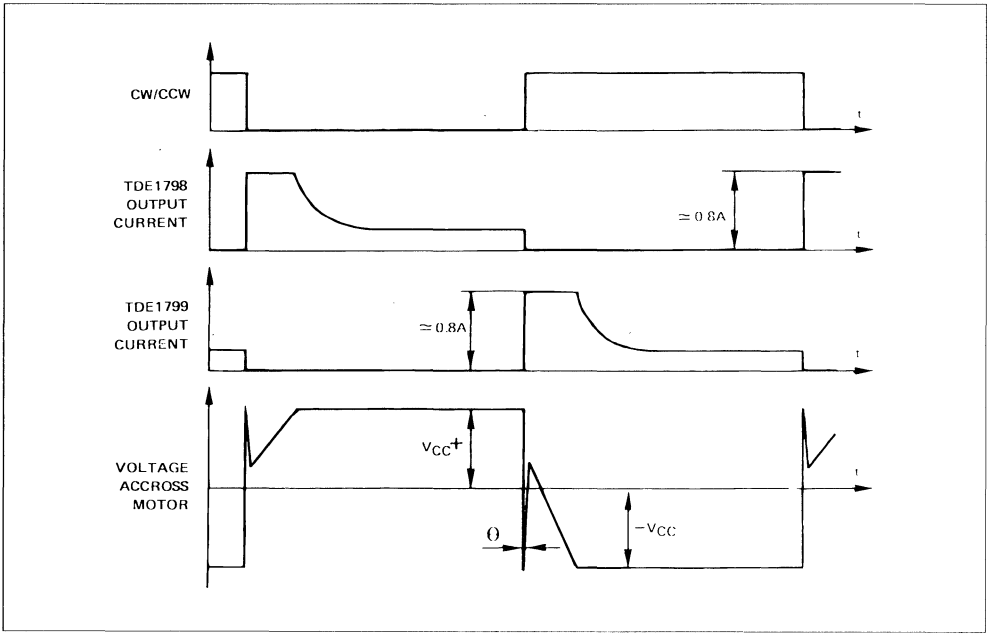


ON/OFF CYCLES

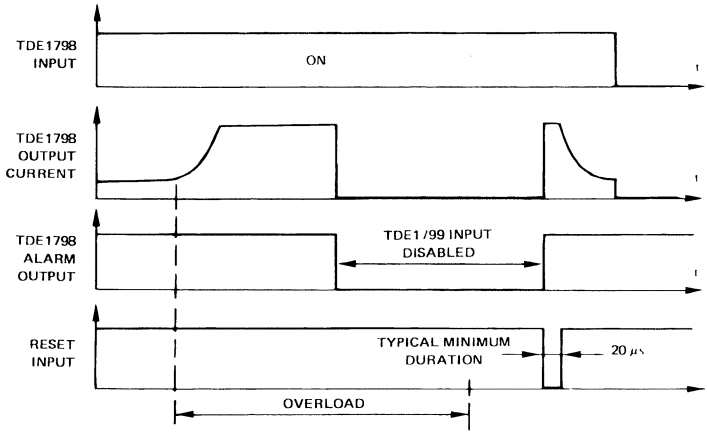


θ . Motor inductance demagnetization

ROTATION REVERSING



OVERLOAD CONDITIONS



* For instance overload during TDE1798 operation

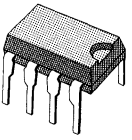
0.5 A INTELLINGENT POWER INTERFACE

ADVANCE DATA

- LOAD CONNECTED TO V_{CC}
- HIGH OUTPUT CURRENT 500mA
- SHORT CIRCUIT PROTECTION UP TO V_{CC} – 33 V
- INTERNAL THERMAL PROTECTION WITH EXTERNAL RESET AND SYNCHRONIZATION CAPABILITY
- LARGE SUPPLY VOLTAGE RANGE FROM 6 V UP 33 V
- SINK ALARM OUTPUT
- DIFFERENTIAL INPUTS FOR ANY LOGIC SIGNALS COMPATIBILITY
- INPUTS ARE OPERATIONAL WITH SIGNAL HIGHER THAN V_{CC} AND UP TO 45 V
- INPUT VOLTAGE CAN BE LOWER THAN GROUND
- OUTPUT VOLTAGE CAN BE GREATER THAN V_{CC} ($V_O \leq V_{CC}$ max.)
- OPEN LOAD DETECTION
- SHORT DURATION SHORT CIRCUIT DETECTION
- SUITABLE FOR PARALLEL DRIVING

Open load ans hort duration short-circuits may be detected through the output "status function".

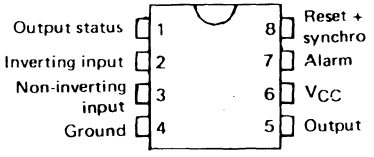
For higher output currents applications several devices can be put in parallel. In this configuration synchronous reactivation is achieved by connecting reset inputs in parallel.



MINIDIP/2

ORDER CODE : TDE1799DP

PIN CONNECTION

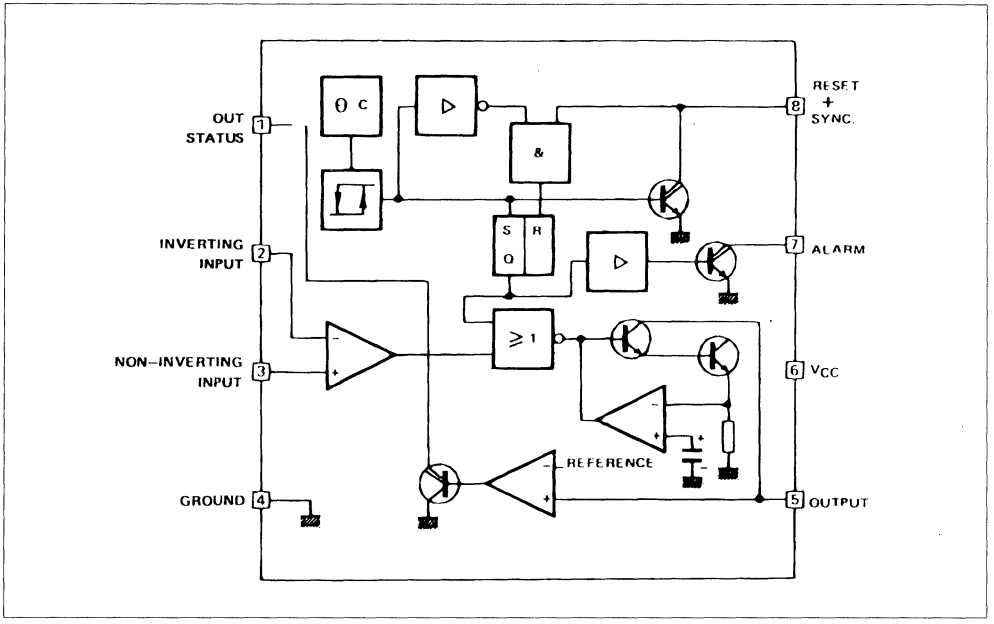


DESCRIPTION

The TDE1799 is an interface circuit delivering high currents and able to drive any kind of loads.

This device is essentially blow out proof. The output is protected from short-circuits with the positive supply or ground. In addition shut down is provided to keep the IC from overheating. If internal dissipation becomes too high, the driver will shut down to prevent excessive heating. The alarm output is activated after thermal shut down. If the reset input is high the output will alternatively switch on and off until the overload is removed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

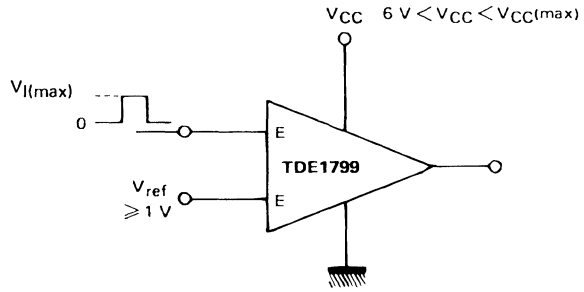
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	50	V
V_{ID}	Input Differential Voltage	50	V
V_I	Input Voltage	– 30 to + 50	V
$V_{I\,reset}$	Reset Input Voltage	V_{CC} – 50 to V_{CC} ,	V
I_O	Output Current	Internally Limited	A
I_{sink}	Alarm and Reset Outputs Sink Current	20	mA
V_{OS} V_A	Output Status Voltage Alarm Voltage	V_{CC} – 50 to V_{CC}	V
P_{tot}	Power Dissipation	Internally Limited	mW
T_{oper}	Operating Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

THERMAL DATA

$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance (note 1)	30	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance (note 1)	70	°C/W
$T_{shutdown}$	Minimum Thermal Shutdown Temperature	150	°C

Note : 1. Devices bonded on a 40 cm^2 glass-epoxy printed circuit 0.15 cm thick with 4 cm^2 of copper.

Figure 1.



The reference input can be inverting or the non-inverting one.

ELECTRICAL CHARACTERISTICS

- 25 °C ≤ T_{amb} ≤ + 85 °C, 6 V ≤ V_{CC} ≤ + 33 V, I_O ≤ 500 mA, T_j ≤ + 150 °C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage	(note 3)	–	2	50	mV
I_{CC}	Power Supply Current	T_{amb} = + 25 °C	–	3	4	mA
I_{IB}	Input Bias Current		–	15	40	µA
V_{ICR}	Common-mode Input Voltage Range	(note4)	1	–	45	V
V_I	Input Voltage Range	V_{ref} ≥ + 1 V, figure 1, note 4	– 25	–	45	V
I_{SC}	Short-Circuit Output Current	V_{CC} = 33 V, t = 10 ms, T_{amb} = 25 °C	–	700	–	mA
V_O	Output Saturation Voltage	– ($V_I^+ - V_I^-$ > 50 mV, I_O = 500 mA	–	1	1.25	V
I_{OL}	Output off Leakage Current	(V_{CC} = + 30 V, V_O = 30 V, T_j = + 85 °C)	–	50	100	µA
I_{sink}	Available Alarm Output Sink Current	V(pin 7) ≤ 2 V	6	15	–	mA
I_L	Alarm Leakage Current		–	–	100	µA
I_{RH}	Reset High Leakage Current		–	15	40	µA
$V_{th(reset)}$	Reset Threshold	(note 5)	–	1.4	–	V
I_{reset}	Reset Output Sink Current (in thermal shut down)	for V(pin8) ≤ + 0.8 V (note 6)	2	–	–	mA
I_{OSH}	Output Status High Leakage Current	(T_{amb} = + 25 °C)	–	15	100	µA
$I_{OS\ sink}$	Available Output Status Sink Current	V (pin 1) ≤ 2 V	6	15	–	mA
V_{THOS}	Output Status Reference Threshold		–	5	6	V
V_L	Alarm Voltage in Thermal Shut down	(I_{AL} = 4 mA)	–	0.7	–	V

Notes : 2. For operating at high temperature, the TDE1799 must be derated based on a + 150 °C maximum junction temperature and a junction-ambient thermal resistance of 70 °C/W.
3. The offset voltage given is the maximum value of input differential voltage required to drive the output voltage within 2 V of the ground of the supply voltage.
4. Input voltage range is independent of the supply voltage.
5. After thermal shut down, voltage required to restart.
6. When in thermal shut down the reset pin 8 draws a current.

Figure 2 : Supply Current / vs. Supply Voltage.

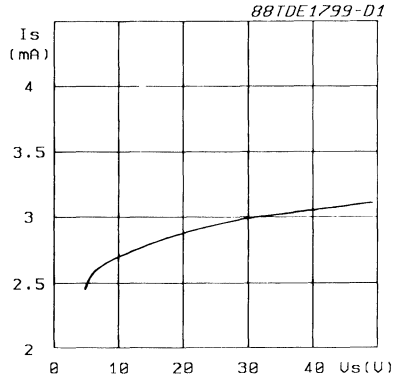


Figure 3 : Alarm Output Current and Voltage.

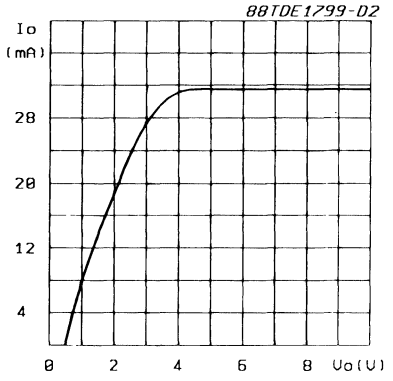


Figure 4 : Saturation Voltage / vs. Output Current.

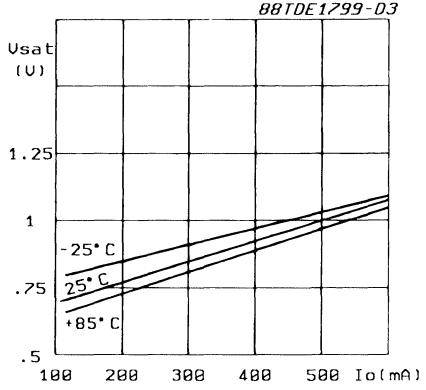


Figure 5 : Typical Application with Automatic Reset.

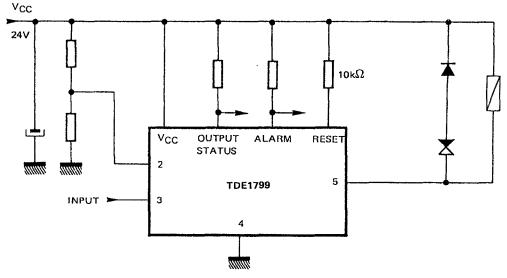


Figure 6 : Short-Circuit and Over loads Conditions Waveforms.

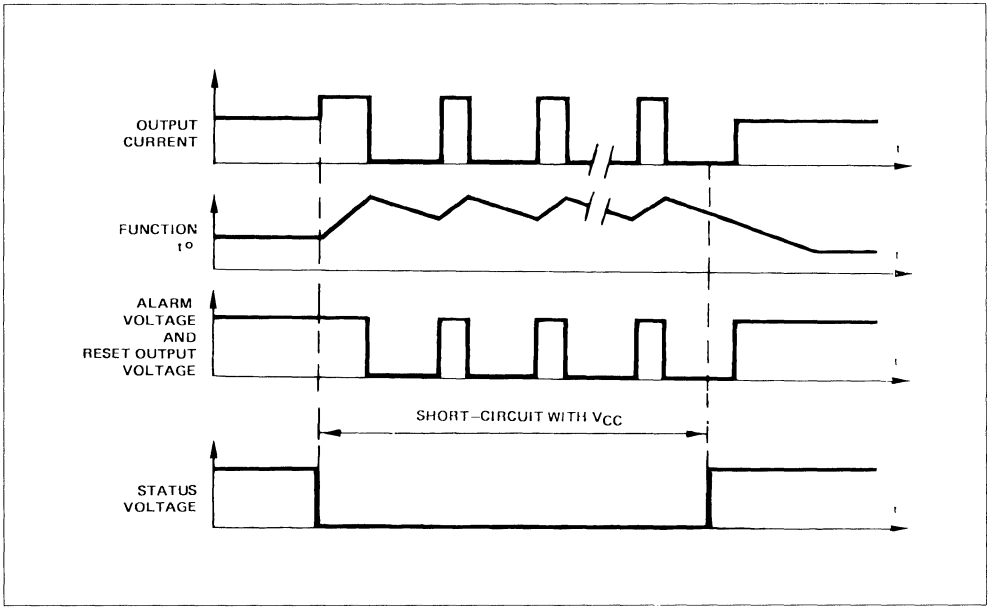


Figure 7 : Typical Application with Controlled Reset.

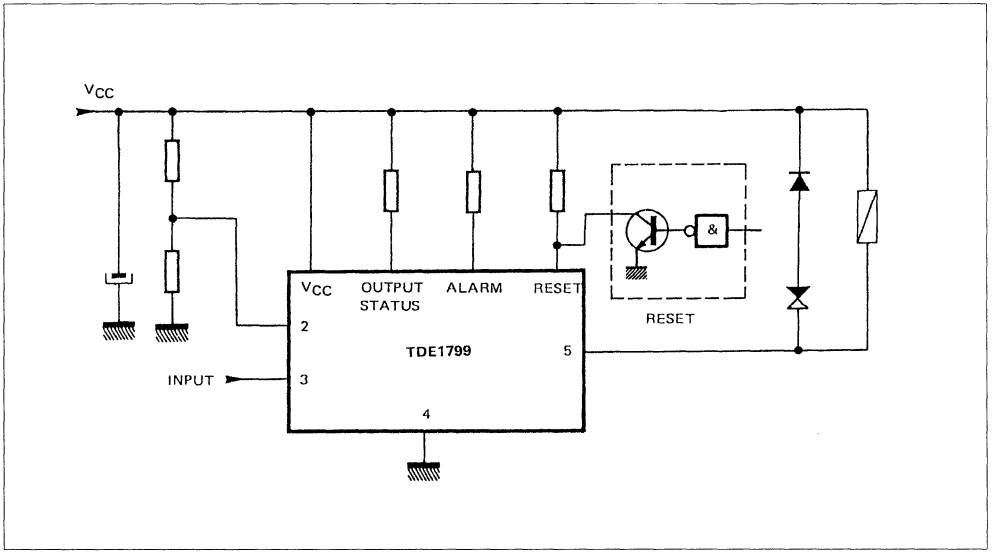


Figure 8 : Short-Circuit and Over loads Conditions Waveforms.

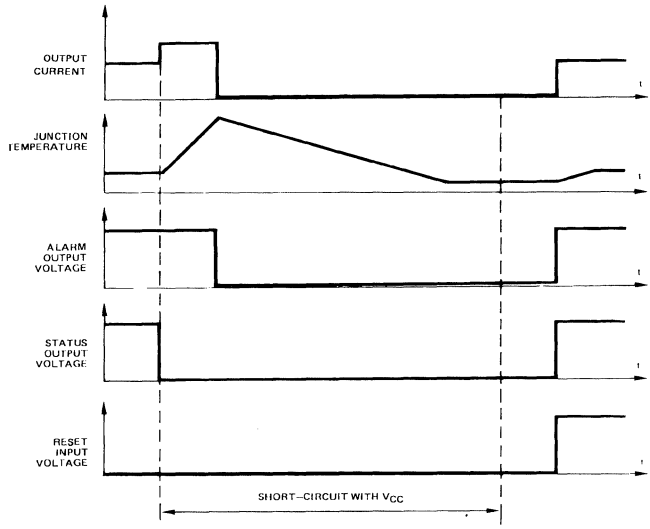
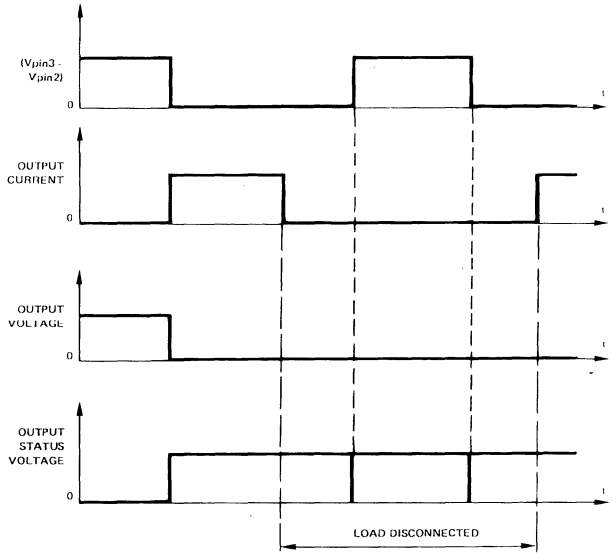
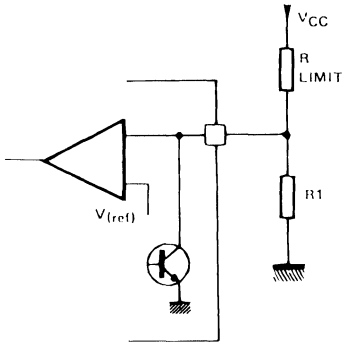


Figure 9 : Output Status Function : Open Load Detection.



Open load detection is possible during the hachured area when (Vpin 3 - Vpin 2) (Output status) 1.

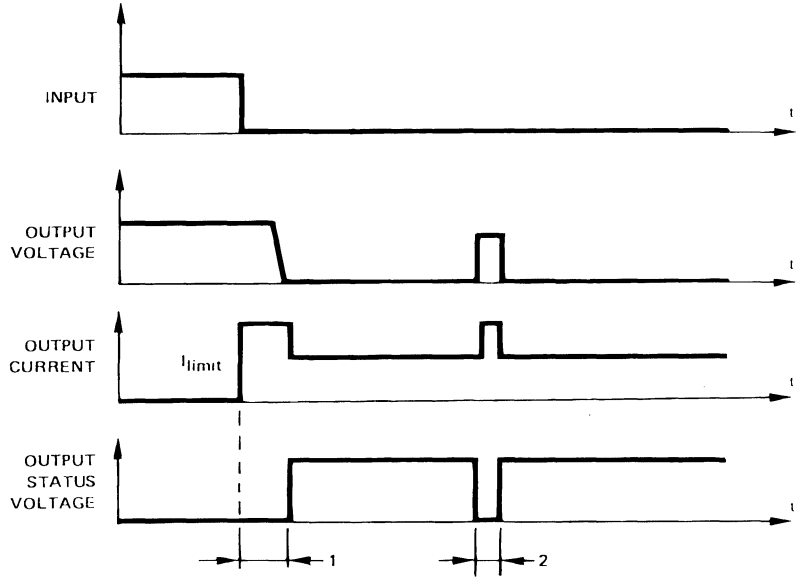
Figure 10.



$$R_1 = \frac{R_{limit} \cdot V_{ref}}{V_{CC} - V_{ref}}$$

REMARK : sometimes the user considers as an open load a load greater than R limit. In this case a resistor R1 must be connected between the output and ground.

Figure 11 : Output Status Function Short Duration / Short Circuit Detection.



(INPUT) OSV 1 → CURRENT LIMITATION

REMARK : long duration short circuit are detected by the thermal shut down.

RESET AND SYNCHRONIZATION

Recommended diagram when the outputs are in parallel. After thermal disjunction a restart is possible when all the circuits are returned in operating conditions.

Figure 12 : Synchronous Automatic Reset (Parallel or Independent Outputs).

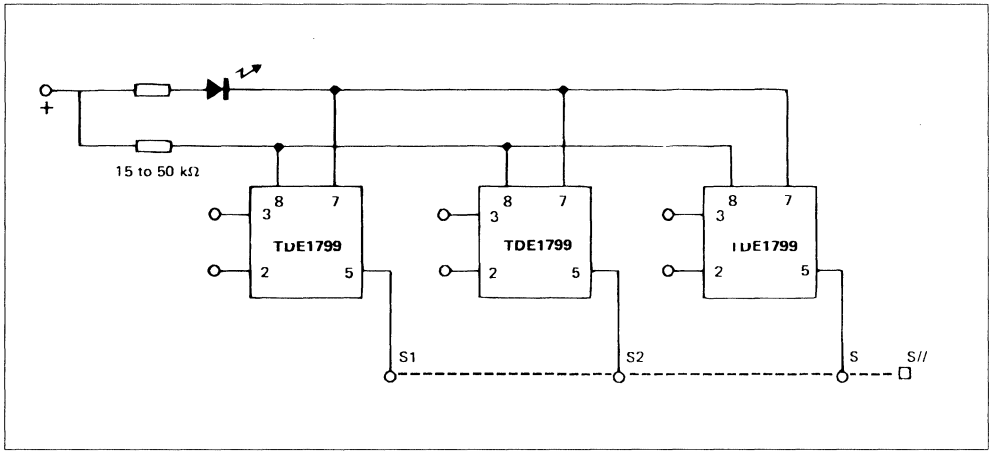
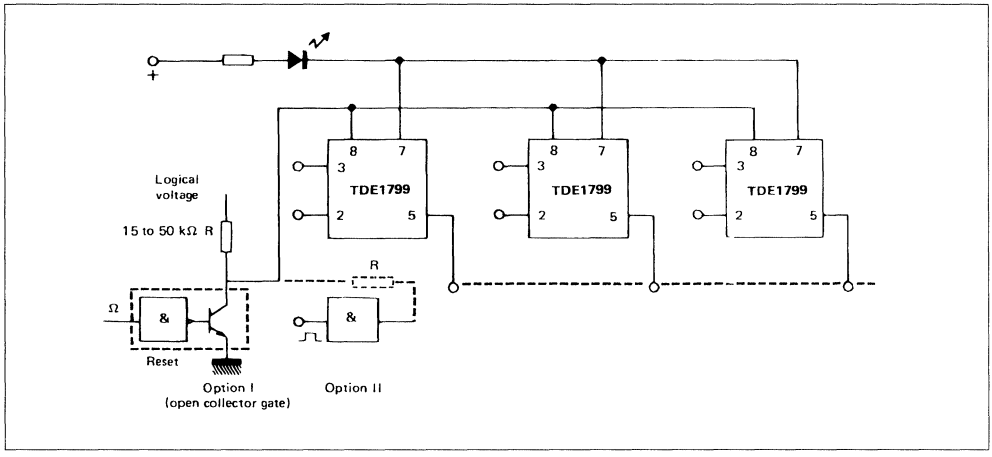


Figure 13 : Synchronous Controlled Reset (Parallel or Independent Outputs).



MAIN FEATURES

- V_{CC}^{*} V_{CC} 50 V
- Maximum output current 0.5 A
- Full protection against overloads and short circuits
- No need of deadtime during rotation reversing
- TTL compatible inputs
- TDE1799 and TDE1798 input signals have the same reference
- No automatic restart after disjunction

CW/CCW	ON OFF	1798	1799
0	0	OFF	OFF
0	1	ON	OFF
1	1	OFF	ON
1	0	OFF	OFF

Figure 14 : Two Quadrants D.C. Motor Drive.

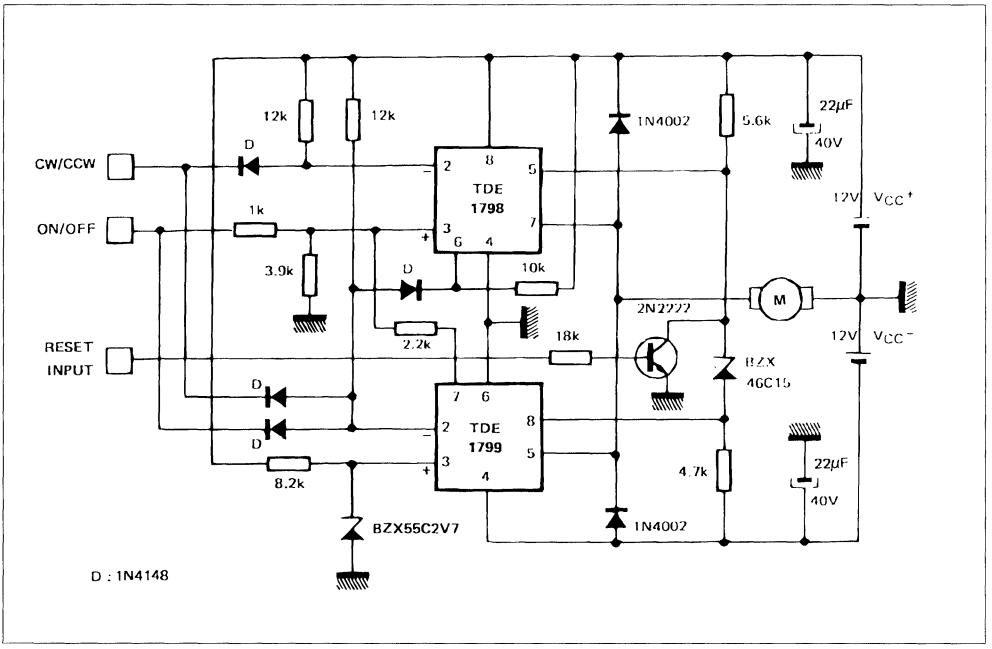
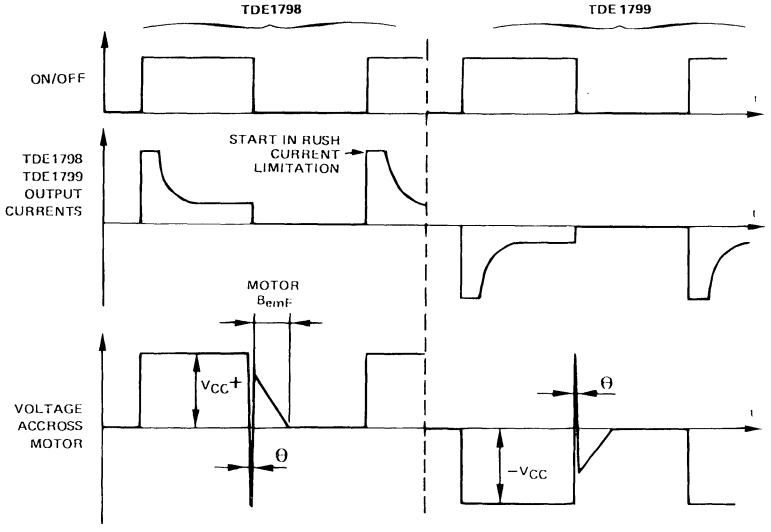


Figure 15 : ON OFF Cycles.



() Motor inductance demagnetization.

Figure 16 : Rotation Reversing.

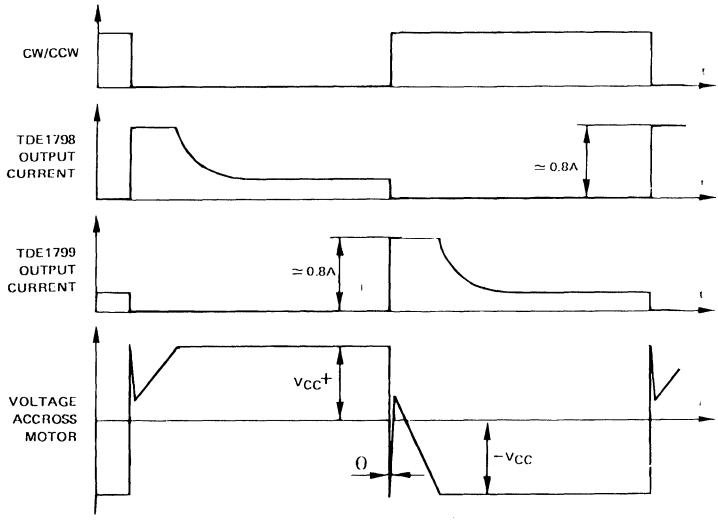
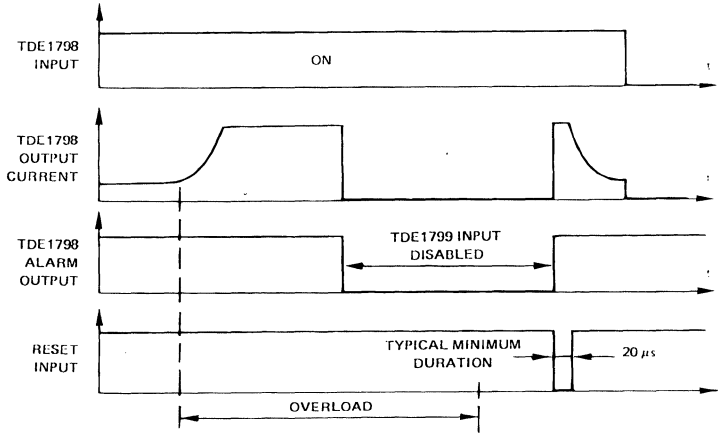


Figure 17 : Overload Conditions.

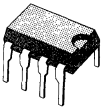


*** For instance overload during TDE1798 operation.**

INTERFACE CIRCUIT (RELAY AND LAMP DRIVER)

- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION TO GROUND
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS TO AVOID THE INTERMEDIATE OUTPUT LEVELS
- LARGE SUPPLY VOLTAGE RANGE : + 10 V TO + 30 V
- SHORT-CIRCUIT PROTECTION TO V_{CC}

MINIDIP/2



ORDER CODE : TDE3207DP

DESCRIPTION

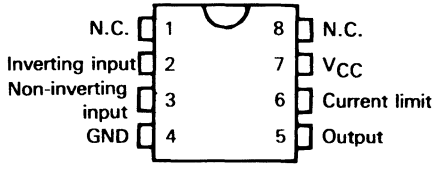
The TDE3207 is a monolithic amplifier designed for high-current and high-voltage applications, specifically to drive lamps, relays and stepping motors.

This device is essentially blow-out proof. Current limiting is available to limit the peak output current to a safe value, the adjustment only requires one external resistor. In addition, thermal shut down is provided to keep the IC from overheating. If external dissipation becomes too high, the driver will shut down to prevent excessive heating.

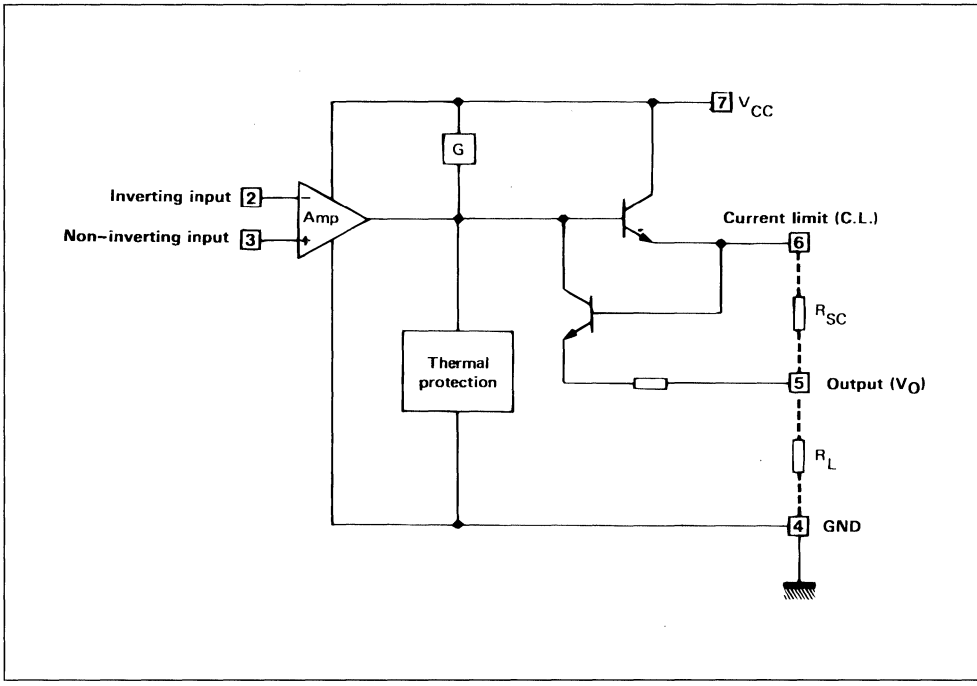
The output is also protected from short-circuits with the positive power supply.

The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies down to the single + 12 V or + 24 V used for industrial electronic systems.

PIN CONNECTION



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	36	V
V_{ID}	Differential Input Voltage	36	V
V_I	Input Voltage	36	V
I_O	Output Current	300	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Ambient Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS

- 25 °C ≤ T_{amb} ≤ + 85 °C, + 8 V ≤ V_{CC} ≤ + 30 V, I_O ≤ 150 mA, T_j ≤ + 150 °C (unless otherwise specified)

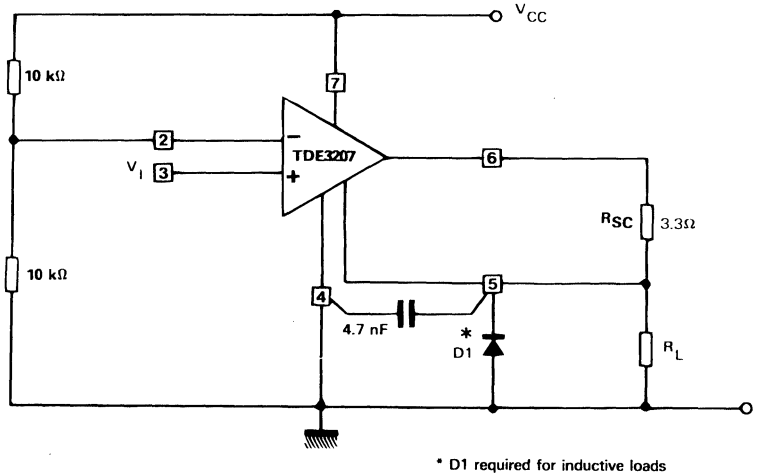
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage – (note 2)	–	2	50	mV
I_{IB}	Input Bias Current	–	0.1	1.5	µA
I_{CC}	Supply Current (V_{CC} = + 24 V, I_O = 0, T_{amb} = + 25 °C) High Level Low Level	 – –	 4 2	 10 –	mA
V_{CM}	Common–mode Input Voltage Range	2	–	V_{CC}–2	V
I_{SC}	Short–circuit Current (T_{amb} = + 25 °C, V_{CC} = + 24 V, R_{SC} = 3.3 Ω)	–	250	–	mA
V_{CC}–V_O	Output Saturation Voltage (output high) ($V_I^+ - V_I^-$) ≥ + 50 mV, I_O = 150 mA, R_{SC} = 0, T_j = + 25 °C	–	1.2	1.8	V
I_{OL}	Output Leakage Current (output low) V_O = 0 V, V_{CC} = + 24 V T_j = + 25 °C T_j = + 85 °C	 – –	 1 –	 100 500	µA
I_{OS}	Minimum Short–circuit Output Current T_{amb} = + 25 °C, V_{CC} = + 24 V, R_{SC} = ∞	–	50	–	mA

Notes : 1. For operating at high temperatures, the TDE3207 must be derated based on a + 150 °C maximum junction temperature and a junction-ambient thermal resistance of 110 °C/W.

2. The offset voltage given is the maximum value of input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.

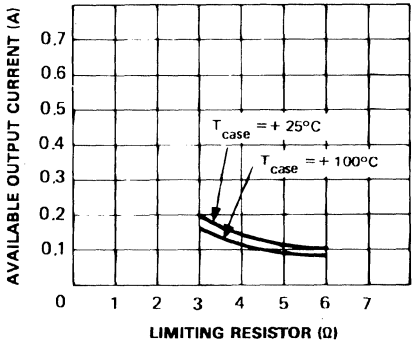
TYPICAL APPLICATIONS

BASIC CIRCUIT

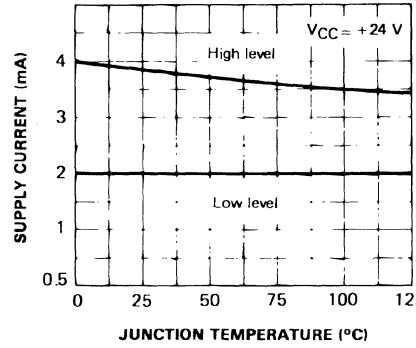


* D1 required for inductive loads

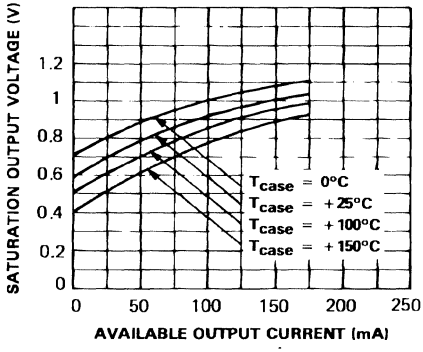
AVAILABLE OUTPUT CURRENT VERSUS LIMITING RESISTOR



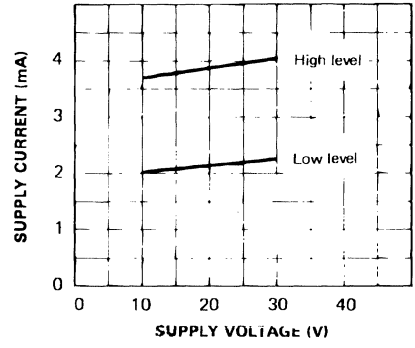
SUPPLY CURRENT VERSUS JUNCTION TEMPERATURE



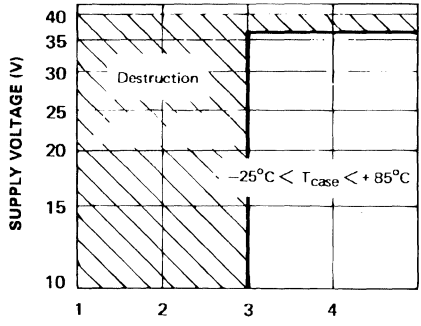
SATURATION OUTPUT VOLTAGE VERSUS CASE TEMPERATURE AND AVAILABLE OUTPUT CURRENT



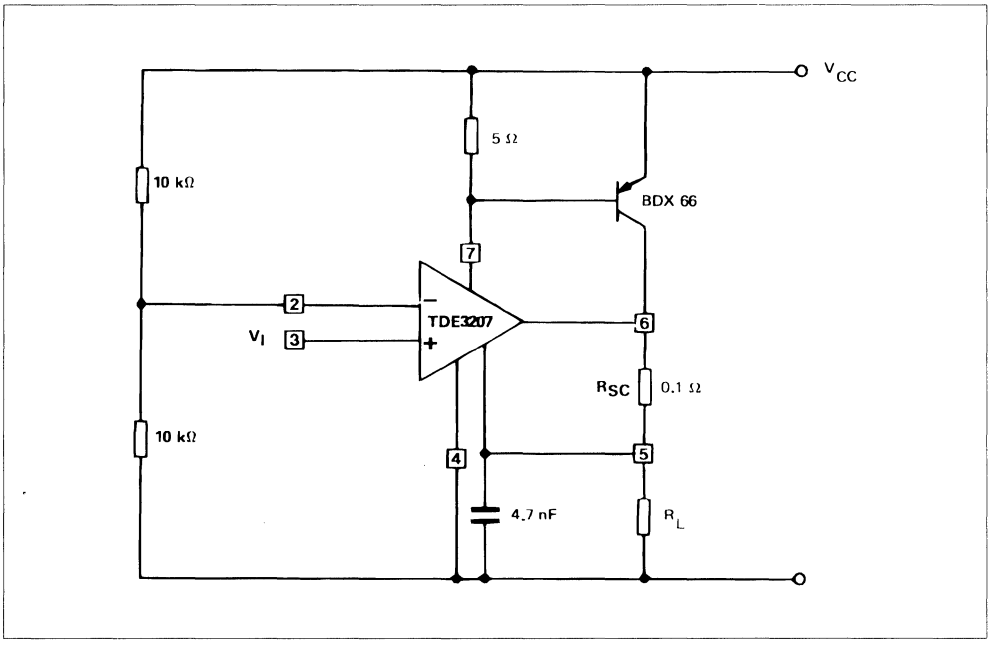
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



SUPPLY VOLTAGE vs MINIMUM LIMITING RESISTOR VALUE



OUTPUT CURRENT BOOSTING (5 A)



SGS-THOMSON MICROELECTRONICS

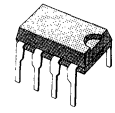
TDE3237

INTELLIGENT POWER SWITCH

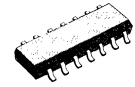
ADVANCE DATA

- HIGH OUTPUT CURRENT
- ADJUSTABLE SHORT-CIRCUIT PROTECTION
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS TO AVOID THE INTERMEDIATE OUTPUT LEVELS
- LARGE SUPPLY VOLTAGE RANGE : + 8 V TO 30 V

MINIDIP/2



SO14J



ORDER CODES : TDE3237DP (MINIDIP)
TDE3237FP (SO14J)

DESCRIPTION

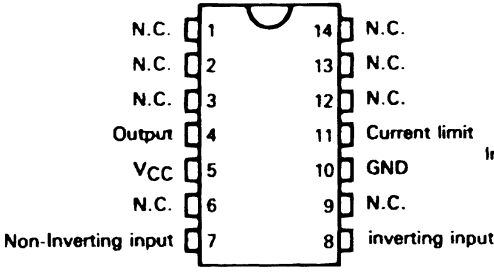
The TDE3237 is a monolithic amplifier designed for high current and high voltage applications, specially to drive lamps, relays and control of stepper motors.

This device is essentially blow-out proof. Current limiting is available to limit the peak output current to a safe value, the adjustment only requires one external resistor. In addition, thermal shut down is provided to keep the I.C. from over heating. If external dissipation becomes too great, the driver will shut down to prevent excessive heating.

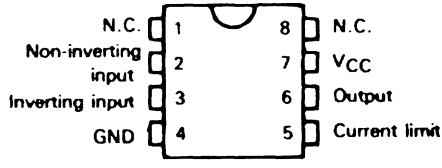
The output is also protected against short-circuits with the positive power supply.

The device operates over a wide range of supply voltages from standard ± 15 V operational amplifier supplies down to the single + 12 V or + 24 V used for industrial electronic systems.

PIN CONNECTIONS (top views)



SO14J



MINIDIP

ABSOLUTE MAXIMUM RATINGS

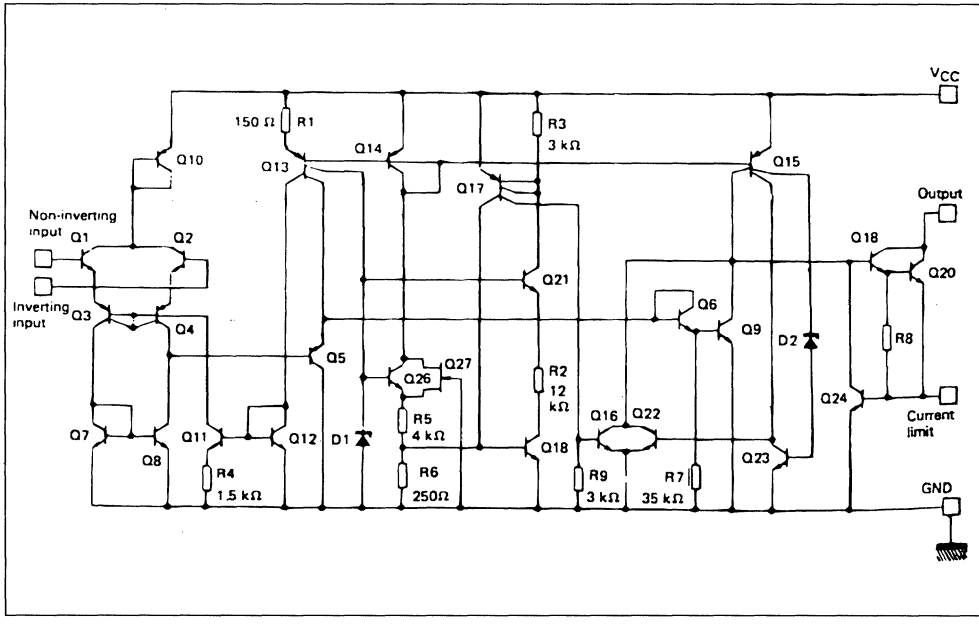
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	36	V
V_I	Input Voltage	36	V
V_{ID}	Differential Input Voltage	36	V
I_O	Output Current	500	mA
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Free–air Temperature Range	– 25 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction–case Thermal Resistance (note 1)	Minidip	50	°C/W
$R_{th(j-a)}$	Maximum Junction–ambient Thermal Resistance (note 1)	Minidip	120	°C/W
–	Junction–ceramic Substrate (case glued to substrate)	SO14	90	°C/W
–	Junction–ceramic Substrate (case glued to substrate, substrate temperature maintened constant)	SO14	65	°C/W

Note : 1. Devices bonded on 40 cm^2 glass-epoxy printed circuit 0.15 cm thick with 4 cm^2 of copper.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

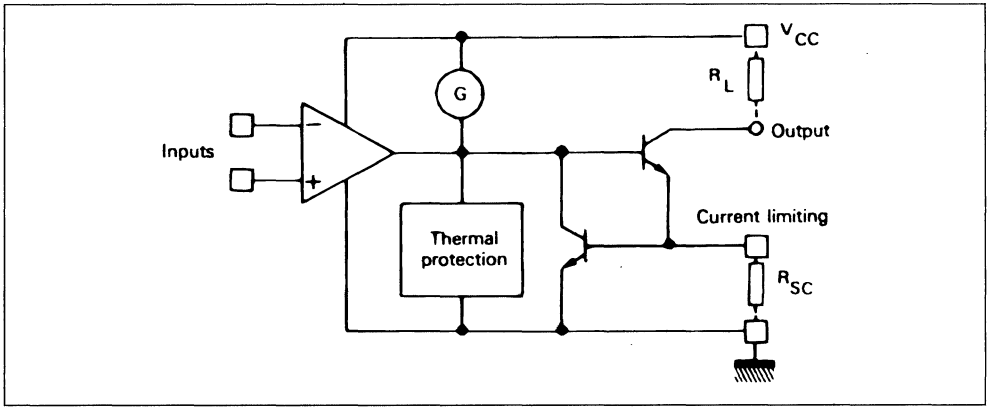
- 25 °C < T_{amb} ≤ + 85 °C, + 8 V ≤ V_{CC} ≤ 30 V, I_O ≤ 150 mA, T_j ≤150 °C (note 2) (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IO}	Input Offset Voltage (note 3)	–	2	50	mV
I_{IB}	Input Bias Current	–	0.1	1.5	µA
I_{CC}	Supply Current (V_{CC} = + 24 V, I_O = 0)	–	3	5	mA
V_{CM}	Common–mode Input Voltage Range	2	–	V_{CC} –2	V
I_{SC}	Short–circuit Current Limit (R_{SC} = 3.3 Ω, T_{case} = + 25 °C)	–	230	–	mA
V_{CC}–V_O	Output Saturation Voltage (output low) ($V_I^+ - V_I^- > 50$ mV, I_O = 150 mA, R_{SC} = 0)	–	1	1.5	V
I_{OL}	Output Leakage Current (output high) ($V_O = V_{CC}$ = + 24 V, T_{amb} = + 25 °C)	–	–	100	µA

Notes : 2. For operating at high temperatures, the TDE3237 must be derated on a 150 °C maximum junction temperature and a junction-ambient thermal resistance as showed in the thermal characteristics data base.

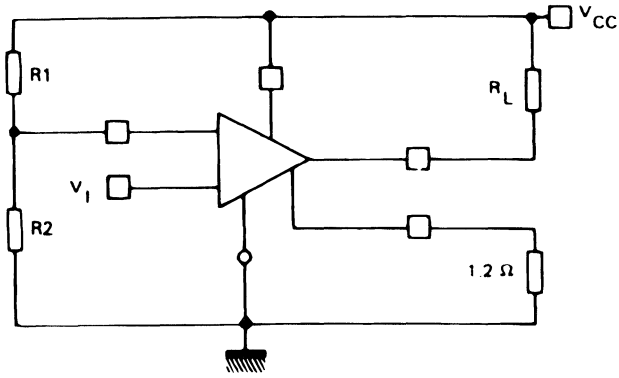
3. The offset voltage given is the maximum value of input voltage required to drive the output voltage within 2 V of the ground or the supply voltage.

SIMPLIFIED SCHEMATIC

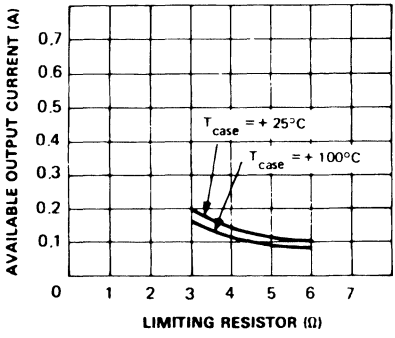


TYPICAL APPLICATION

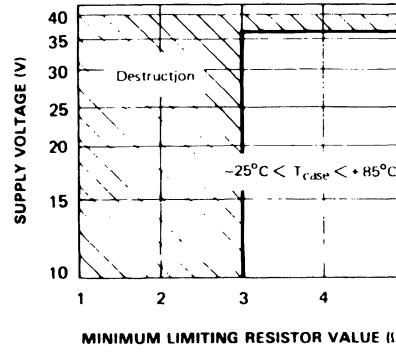
BASIC CIRCUIT



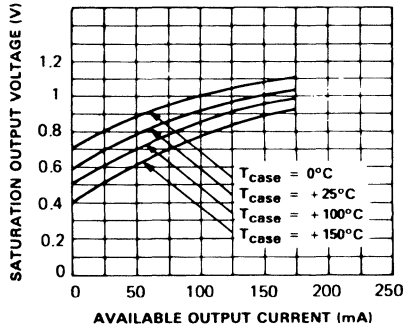
AVAILABLE OUTPUT CURRENT VERSUS LIMITING RESISTOR



SUPPLY VOLTAGE VS MINIMUM LIMITING RESISTOR VALUE



SATURATION OUTPUT VOLTAGE VERSUS CASE TEMPERATURE AND AVAILABLE OUTPUT CURRENT



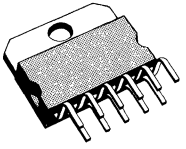
SGS-THOMSON MICROELECTRONICS

TDF1778

DUAL 2-A SOURCE DRIVER

- OUTPUT CURRENT UP TO 2.5 A
- WIDE RANGE OF SUPPLY VOLTAGES : + 8 to + 32 V
- CAN WITHSTAND OVERVOLTAGES OF AS HIGH AS 60 V BETWEEN V_{CC} AND GROUND
- INTERNAL ZENER DIODE PROVIDES FAST SWITCHING OF INDUCTIVE LOADS
- OUTPUT VOLTAGE CAN BE LOWER THAN GROUND

MULTIWATT-11



ORDER CODE : TDF1778SP

DESCRIPTION

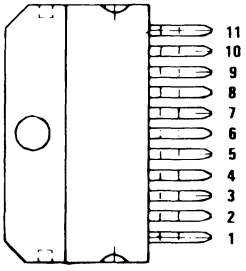
The TDF1778 is a dual source driver delivering high output currents and capable to drive any type of loads (Electrovalves, contactors, lamps).

This device is essentially blow-out proof, each output is protected against short-circuits. If internal dissipation becomes too high, drivers will shut down to prevent excessive heating. An "ALARM" output is provided to indicate the action of the thermal protection. To reactivate the power outputs, the reset input must be forced to low state.

"SENSE" information of both power outputs are ORed together and then processed internally.

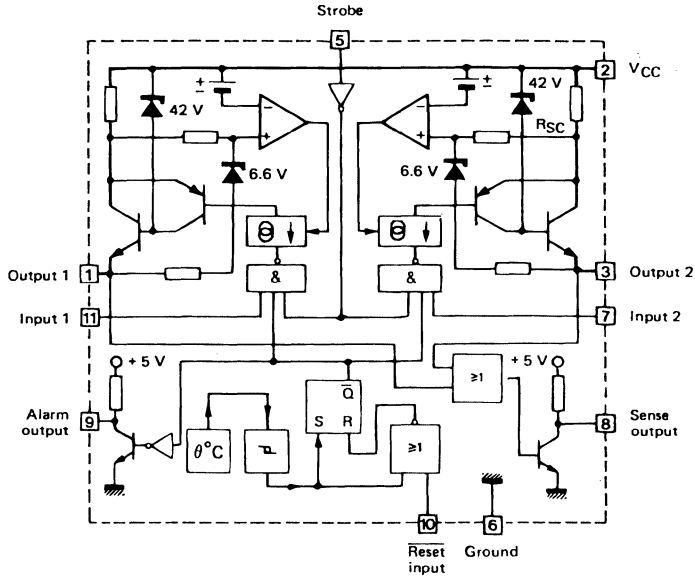
A "STROBE" input is also provided to offer the possibility of disabling the power outputs.

PIN CONNECTION



1 - Output 1
2 - VCC
3 - Output 2
4 - N.C.
5 - Strobe
6 - Ground
7 - Input 2
8 - Sense output
9 - Alarm output
10 - $\overline{\text{Reset}}$ input
11 - Input 1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	35 V (60V/10 ms)	V
V_I, V_{reset}	Input Voltage (pins 7, 10 and 11)	− 30 to + 50	V
V_{strobe}	Strobe Input Voltage	− 0.5 to V_{CC}	V
I_O	Output Current	Internally Limited	A
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Ambient Temperature Range	− 40 to + 85	°C
T_j	Junction Temperature	+ 150	°C

THERMAL DATA

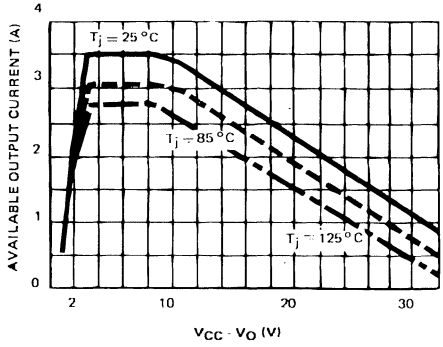
$R_{th(j-c)}$	Maximum Junction—case Thermal Resistance	3	°C/W
$R_{th(j-a)}$	Maximum Junction—ambient Thermal Resistance	40	°C/W

ELECTRICAL CHARACTERISTICS

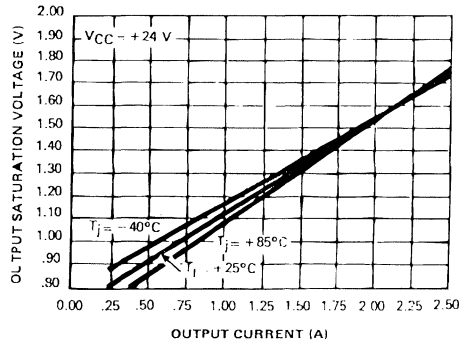
V_{CC} = + 24 V, − 40 °C < T_j < + 85 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	8	–	32	V
I_{CC}	Power Supply Current (pin 6), $I_{O1} = I_{O2}$ = 2 A	–	–	20	mA
V_{IL} V_{IH}	Logic Input Voltage (pins 7, 10, 11)	– 2	– –	0.8 –	V
V_I	Logic Input Threshold (pin 5)	–	0.8	–	V
I_{IH}	High Level Input Current (pins 7, 10, 11) V_I = + 2 V	–	20	50	µA
I_{IL}	Low Level Input Current (pins 7, 10, 11) V_I = + 0.8 V	− 5	0	+ 5	µA
V_{OH}	High Level Logic Output Voltage (pins 8, 9) I(8) = I(9) = − 30 µA	2.4	4	–	V
V_{OL}	Low Level Logic Output Voltage (pins 8, 9) I(8) = I(9) = 2 mA		–	0.4	V
$V_{CC} - V_{O1}$ $V_{CC} - V_{O2}$	Output Saturation Voltage (V(7) high, V(11) high, I_O = 2 A)	– –	1.5	1.8	V
I_{OL}	Low Level Input Current (pins 1, 3) V(7) Low, V(11) Low, V_O = 0 V	–	400	1000	µA
$V_{CC} - V_{O1}$ $V_{CC} - V_{O2}$	Switch–off Output Voltage (inductive load)	40 –	44 –	48	V
I_{O1}, I_{O2}	Available Output Current (pins 1, 3), V(7) High, V(11) High, $V_{CC} - V_O$ = 32 V, T_j = 25 °C	100	–	–	mA
I_{Oalarm}	Available "Alarm" Output Current, V(9) = + 4 V	4	8	–	mA
I_{Osense}	Available "Sense" Output Current, V(8) = + 4 V	4	8	–	mA
$I_{IHsense}$	Output Sensing High Level Input Current (pins 1, 3) V_I = + 2 V	–	1	2	mA
$V_{IHsense}$	High Level "Sense" Input Voltage (pins 1, 3)	0.8	1.9	2.5	V

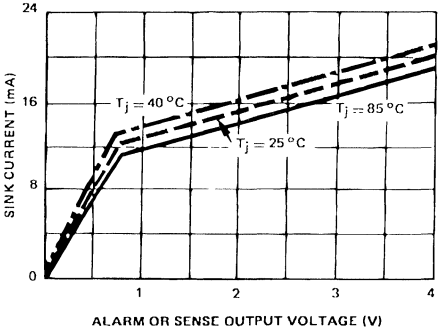
AVAILABLE OUTPUT CURRENT



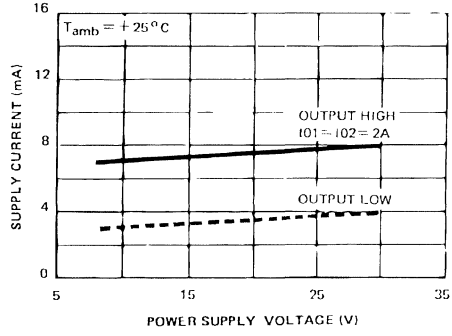
OUTPUT SATURATION VOLTAGE



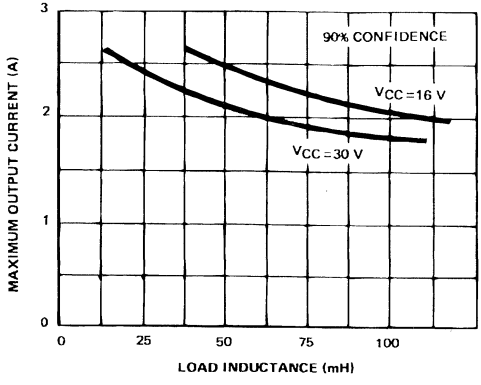
AVAILABLE ALARM OR SENSE OUTPUT CURRENTS



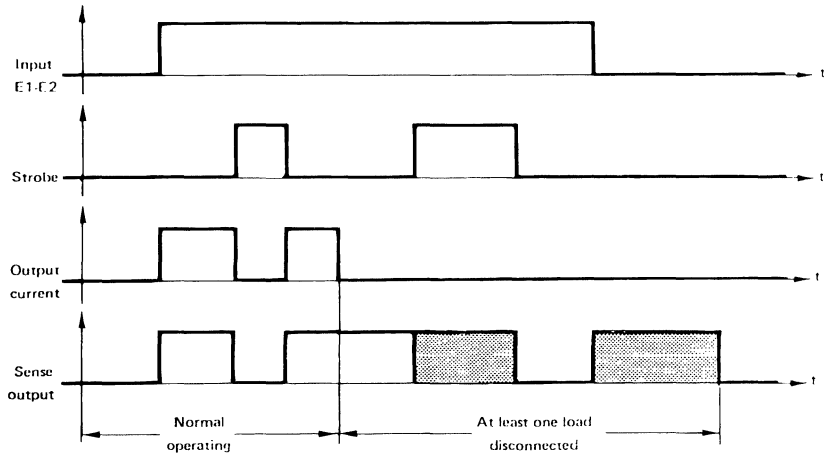
POWER SUPPLY CURRENT



MAXIMUM OUTPUT CURRENT VS LOAD INDUCTANCE



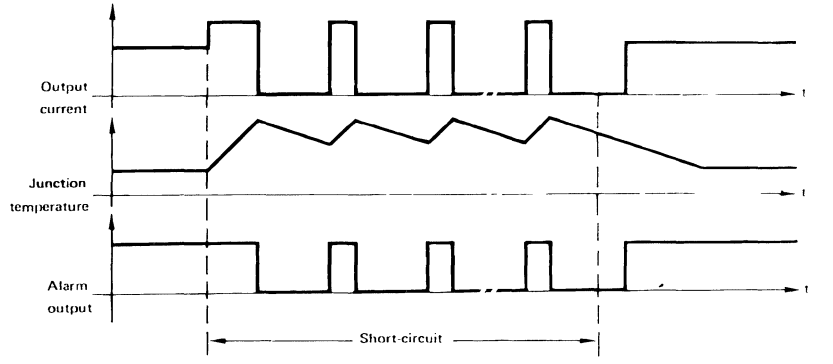
OPEN LOAD DETECTION



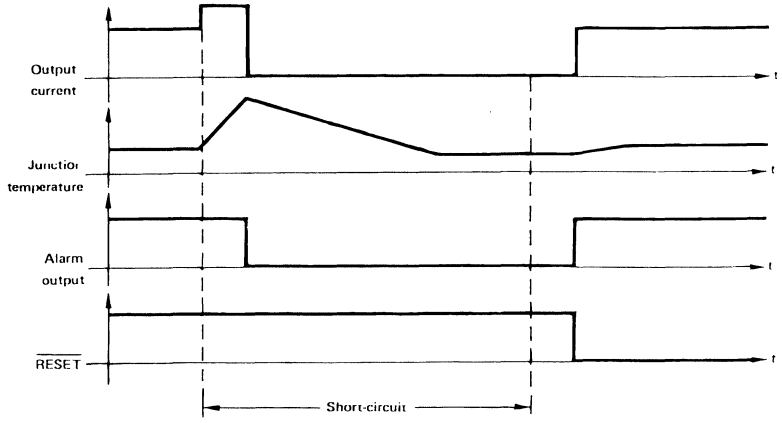
Open load detection is possible during the hachured aeras

Open load detection is possible during the hachured aeras.

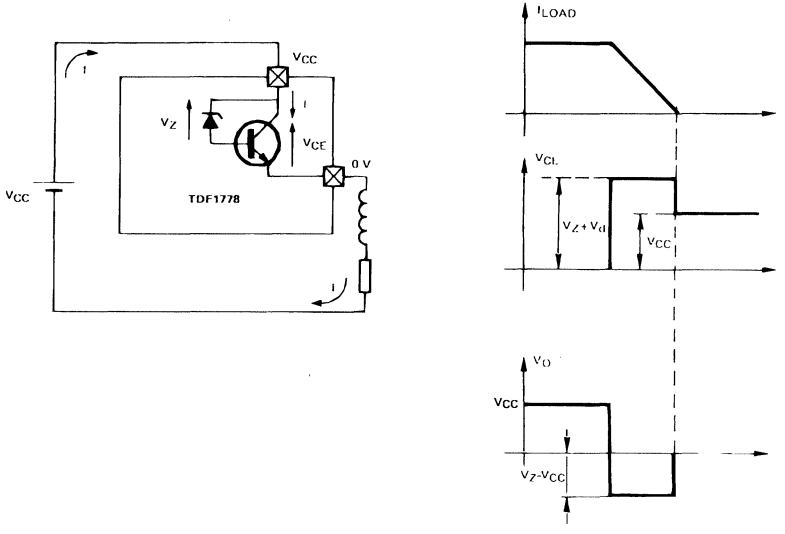
SHORT CIRCUIT CONDITIONS WAVEFORMS WITH AUTOMATIC RESET/$\overline{\text{RESET}}$ = 0



SHORT CIRCUIT WAVEFORMS WITH CONTROLLED RESET/$\overline{\text{RESET}}$ = 1

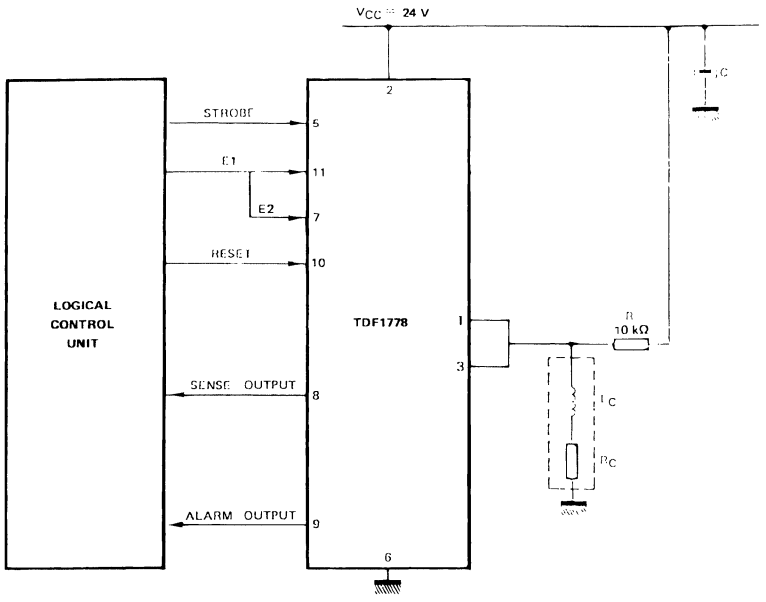


DEMAGNETIZATION UNDER INDUCTIVE LOAD



TYPICAL APPLICATION

TYPICAL APPLICATION WITH TDF1778 TWO INDUCTIVE LOADS 2 A - 24 V



Load : L_C = 80mH , R_C = 6 Ω
R_{max} = V_{CC}/2 mA

Load : L_C = 80 mH, R_C = 12 Ω
R_{max} = V_{CC}/1 mA

MAIN FEATURES

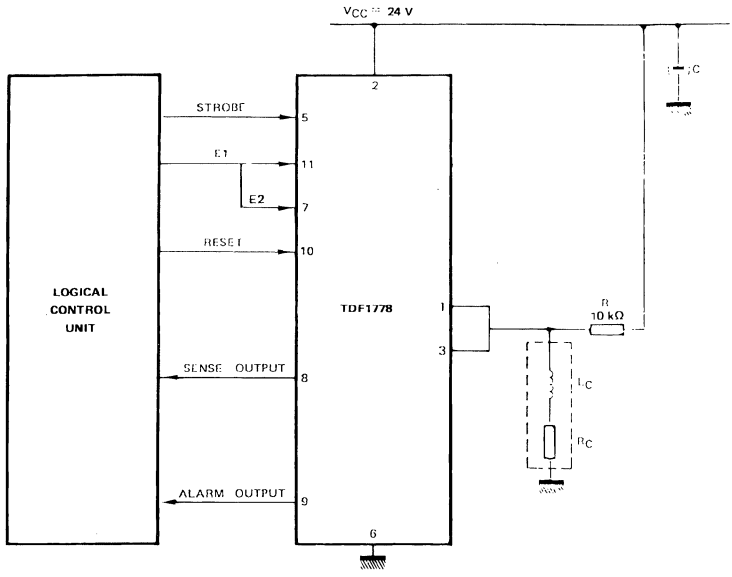
This application protected against short circuits.

The load disconnection is detected when inputs E1 and E2 are low and the sense output is high.

When thermal protection is activated the pin 9 is low.

Inputs and outputs are TTL comptable.

TDF1778 HIGH CURRENT APPLICATION WITH INDUCTIVE LOAD 24 V - 4 A



Load : L_C = 80 mH, T_C = 6 Ω
R_{max} = V_{CC}/2 mA

MAIN FEATURES

This application has the same features as the dual 2 A -12 V application.

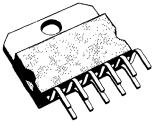
SGS-THOMSON MICROELECTRONICS

TDF1779A

DUAL 2-A SOURCE DRIVER

- OUTPUT CURRENT UP TO 2.5 A
- WIDE RANGE OF SUPPLY VOLTAGE : + 8 V TO + 26 V
- CAN WITHSTAND OVERVOLTAGES OF AS HIGH AS 60 V BETWEEN V_{CC} AND GROUND
- OUTPUT VOLTAGE CAN SWING TO LOWER THAN GROUND
- "SENSE" AND "ALARM" OUTPUTS ARE OPEN COLLECTOR OUTPUTS

MULTIWATT-11



ORDER CODE : TDE 1779ASP

DESCRIPTION

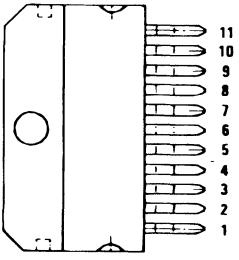
The TDF1779A is a dual source driver delivering hihg output currents and the capability to drive highly inductive loads (Electrovalves, contractors, relays...).

This device is essentially blow-out proof, each output is protected against short-circuits. If internal dissipation becomes too high, drivers will shut down to prevent excessive heating. An "ALARM" output is provided to indicate the action of the thermal protection. To reactivate the power outputs, the reset input must be forced to low state.

"SENSE" information of both power outputs are ORed together and then processed internally.

A "STROBE" input is also provided to offer the possibility of disabling the power outputs.

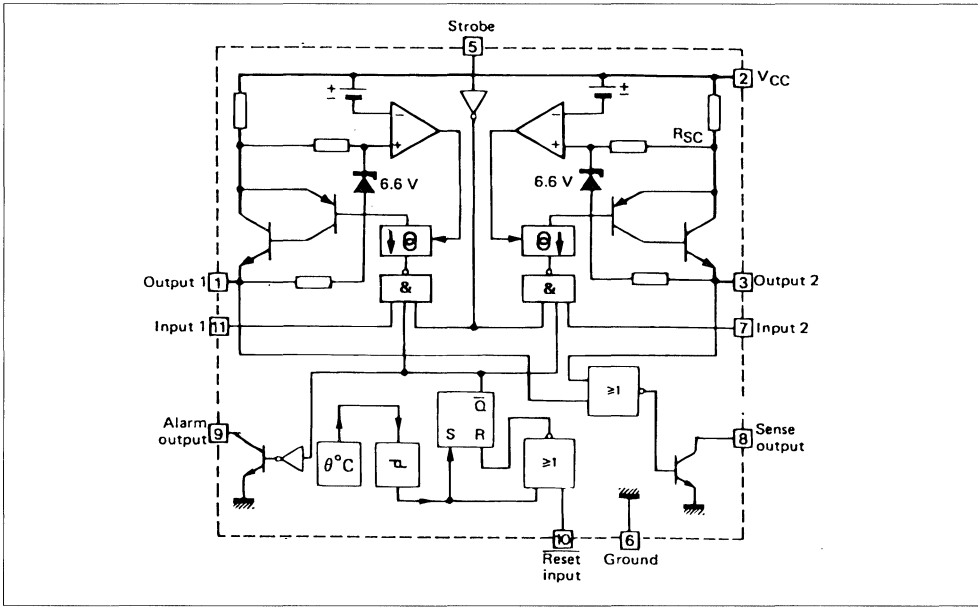
PIN CONNECTIONS



Tab is connected to pin 6

1 - Output 1
2 - V_{CC}
3 - Output 2
4 - N.C.
5 - Strobe
6 - Ground
7 - Input 2
8 - Sense output
9 - Alarm output
10 - Reset input
11 - Input 1

BLOCK DIAGRAM



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	35 V (60 V/10 ms)	V
V_I, V_{reset}	Input Voltage (Pins 7, 10 and 11)	− 30 to + 50	V
V_{strobe}	Strobe Input Voltage	− 0.5 to V_{CC}	V
I_O	Output Current	Internally Limited	A
P_{tot}	Power Dissipation	Internally Limited	W
T_{oper}	Operating Ambient temperature Range	− 40 to + 85	°C
T_j	Junction Temperature	+ 150	°C

THERMAL CHARACTERISTICS

$R_{th\ (j\text{-}c)}$	Maximum Junction-case Thermal Resistance	3	°C/W
$R_{th\ (j\text{-}a)}$	Maximum Junction-ambient Thermal Resistance	40	°C/W

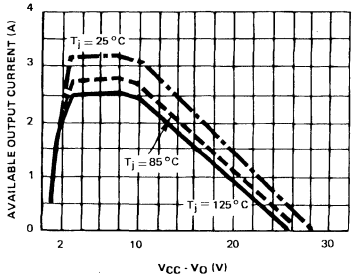
ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = + 24 V, − 40 °C < T_j < + 85 °C (unless otherwise specified)

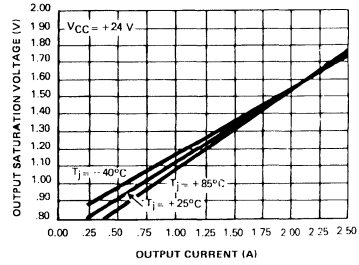
Symbol	Characteristics	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	8	-	26	V
I_{CC}	Power Supply Current (pin 6), IO1 =IO2, = 2A	-	-	20	mA
V_{IL} V_{IH}	Logic Input Voltage (pin 7,10,11)	- 2	- -	0.8 -	V
V_I	Logic Input Threshold (pin 5)	-	0.8	-	V
I_{IH}	High Level Input Current (pins 7,10,11) VI = + 2 V	-	20	50	µA
I_{IL}	Low Level Input Current (pins 7,10,11) VI = + 0.8 V	− 5	0	+ 5	µA
-	Off State Output Voltage (pins 8,9) I(8) = I(9) = 2 mA	-	-	0.4	V
V_{CC} − V01 V_{CC} − V02	Output Saturation Voltage (V(7) high, V(11) High, IO = 2A)	-	1.5	1.8	V
I_{OL}	Low Level Output Current pins 1,3) V(7) Low, V(11) Low, VO = 0 V	-	400	1000	µA
V_{CC} − V01 V_{CC} − V02	Switch-off Output Voltage (inductive load) Note 1	-	-	45	V
$I_{O}1$, I_{O2}	Available Ouptut Current (pins 1,3), V(7) high, V(11p) high, V_{CC} − V_O = 26 V, T_j = 25 °C	10	-	-	mA
$I_{O\ Alarme}$	Available "Alarme" Output Current, V(9) = + 4 V	4	8	-	mA
$I_{O\ Sense}$	Available "Sense Ouptut Current, V(8) = + 4 V	4	8	-	mA
$I_{IH\ Sense}$	Output Sensing high Level Input Current (pins 1,3) V_I = +2 V	-	1	2	mA

Note : 1. An external discharge circuit is required for inductive loads.

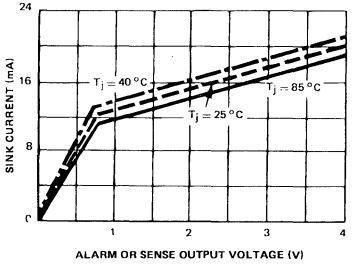
AVAILABLE OUTPUT CURRENT



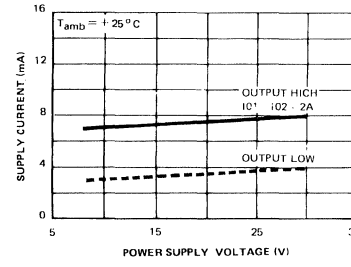
OUTPUT SATURATION VOLTAGE



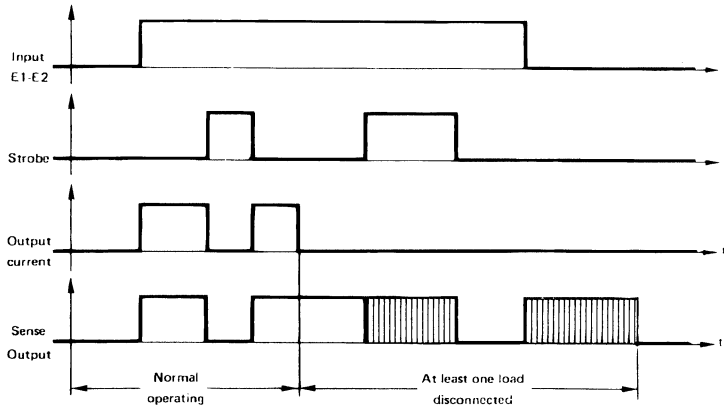
AVAILABLE ALARM OR SENSE OUTPUT CURRENTS



POWER SUPPLY CURRENT

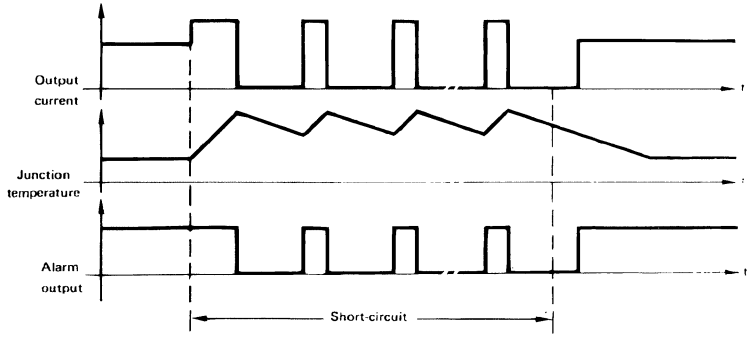


OPEN LOAD DETECTION

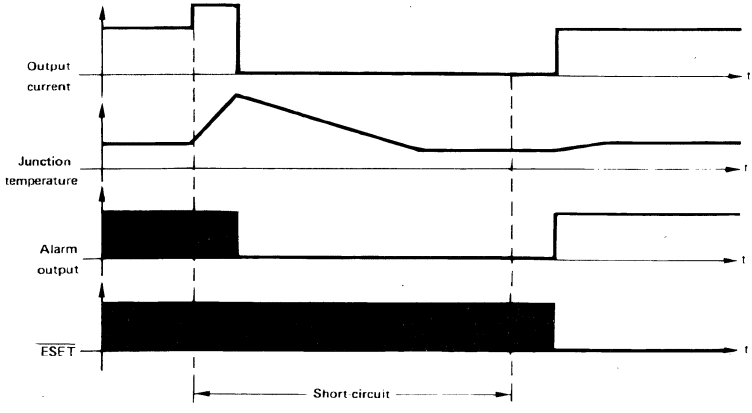


Open load detection is possible during the hachured aeras

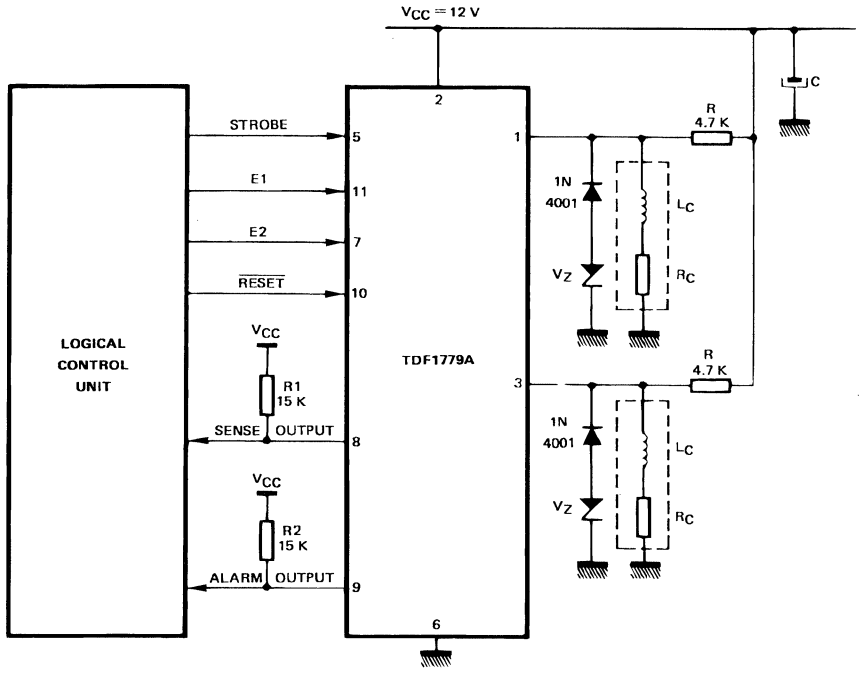
SHORT CIRCUIT CONDITIONS WAVEFORMS WITH AUTOMATIC RESET $\overline{RESET} = 0$



SHORT CIRCUIT CONDITIONS WAVEFORMS WITH CONTROLLED RESET $\overline{RESET} = 1$



TYPICAL APPLICATION WITH TDF1779A TWO LOADS 12 V - 2 A



Load : $R_C = 6\ \Omega$
The external Zener diode must dissipate the power stored in the inductance L_C.
$R_1 min = V_{CC}/4$ mA, $R_2 min = V_{CC}/4$ mA, $R max = V_{CC}/1$ mA.

MAIN FEATURES

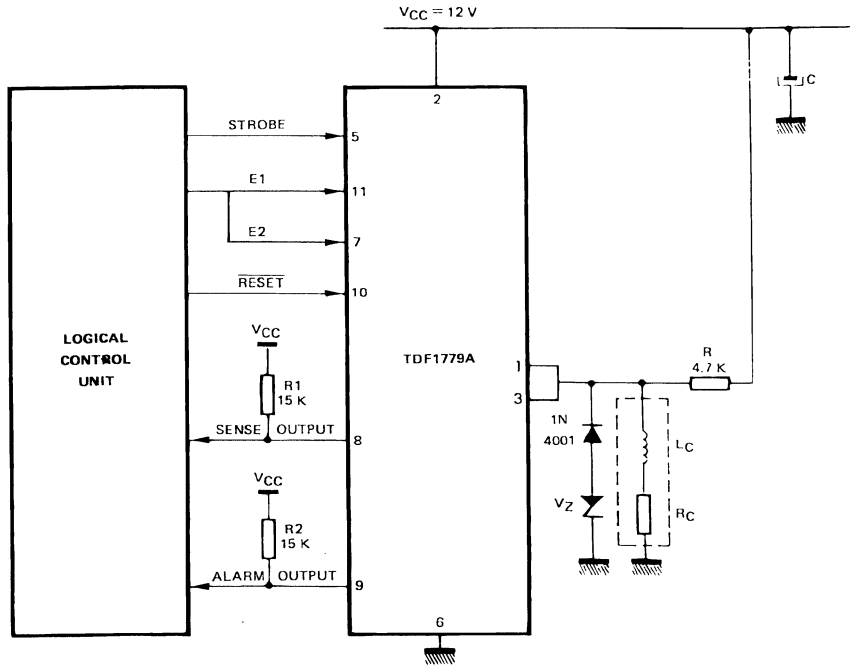
This application is protected against for short circuit and overload.

The load disconnection is detected when inputs E_1 and E_2 are low and the sense output is high.

When thermal protection is actived the pin 9 is low. Inputs are TTL compatible.

Sense output, Alarm output are open collector.

TDF1779A HIGHT CURRENT APPLICATION WITH LOAD 12 V - 4 A



Load : $R_C = 3\ \Omega$
The external Zener diode must dissipate the power stored in the inductance Lc.
$R_1 min = V_{CC}/4$ mA, $R_2 min = V_{CC}/4$ mA, $R max = V_{CC}/2$ mA.

MAIN FEATURES

This application has the same features as the dual 2 A - 12 V application.

LOW DROPOUT TRIPLE 1.5 A SINK DRIVER

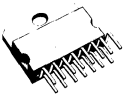
- WIDE OPERATING SUPPLY VOLTAGE RANGE 6 V TO 32 V
- LOW POWER DISSIPATION Vsat : 0.35 V ∂ 1.5 A
- SHORT-CIRCUIT AND OVERLOAD PROTECTION
- DESATURATION MONITORING WITH EXTERNALLY PROGRAMMABLE DELAY
- AJUSTABLE CURRENT LIMITATION
- TTL COMPATIBLE INPUTS
- WITHSTAND (60 V-10 ms) V_{CC} TRANSIENTS

DESCRIPTION

The TDF1783 is a monolithic triple interface circuit designed for high voltage applications. Capable to drive any type of load : inductive, resistive, capacitive.

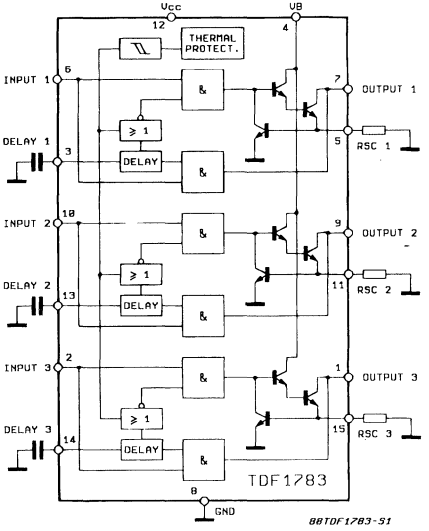
The device is particulary well protected against destructive overloads. Each output implements a current limit circuitry, a desaturation monitoring unit for the detection of overloads and short-circuits. After disjunction, corresponding output is reactivated by applying a logic low signal to the input. A common thermal protection protects the circuit from overheating.

MULTIWATT-15

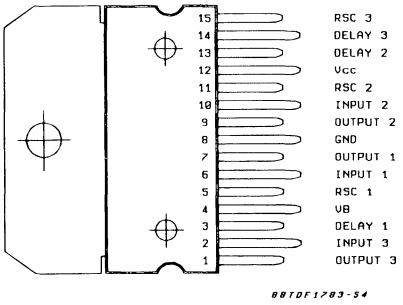


ORDER CODE : TDF1783SP

BLOCK DIAGRAM



PIN CONNECTION (front view)



1 - Output 3
2 - Input 3
3 - Delay 1
4 - VB
5 - RSC 1
6 - Input 1
7 - Output 1
8 - GND
9 - Output 2
10 - Input 2
11 - RSC 2
12 - V_{CC}
13 - Delay 2
14 - Delay 3
15 - RSC 3

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+ 35	V
Vi1 Vi2 Vi3	Input Voltages	− 30 to + 50	V
Vo_{max}	Output Voltage on pin 1, 7, 9 $I_o = 0$	50	V
Ib	Base Current (I pin 4)	300	mA
I_o	Output Current	2.5	A
P_{tot}	Total Power Dissipation	Internally Limited	W
T_{oper}	Operating Free-air Temperature Range	− 40 to + 85	°C
T_j	Junction Temperature	+ 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal resistance	3	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	40	°C/W
$T_{(shutdown)}$	Minimum Thermal Shutdown Temperature	145	°C

ELECTRICAL CHARACTERISTICS V_{CC} = + 13 V, − 40 °C ≤ T_j ≤ + 85 °C
(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		+ 6		+ 32	V
$I_{CC\ OFF}$ $I_{CC\ ON}$	Supply Current	Off On (I_o = 3•1.5 A)		2 7.5	4 10	mA
I_{ih} I_{io}	Input Current	(all inputs) V_{IH} = 2 V V_{IO} = 0.8 V		30 0	100 10	µA
V_{ih} V_{io}	Input Voltage		2		 0.8	V
V_o–V_{rsc}	Output Saturation	Voltage T_j = 85 °C I_o = 0.5 A I_b = 50 mA = 1.5 A " = 2.5 A "		 0.35	 0.20 0.45 0.90	V
V_b	Base Drive Voltage	I_b = 150 mA (3 drivers on) R_{sc} = 0.39 ohms		2		V
I_{sc}	Short Circuit Output Current,	R_{sc} = 0.39 ohms	2			A
I_{oh}	Output Leakage Current (output high)			30	100	µA
t_d	Delay Time Before Desaturation Turn-off	C = 47 nF, V_{CC} = 13 V	4	10	30	ms
I_o	Available Output Current	R_{sc} = 0.39 ohms	1.5			A
t_r	Minimum Reset Signal Duration	C = 47 nF		20		ms

Figure 1 : Maximum Admissible Power Dissipation.

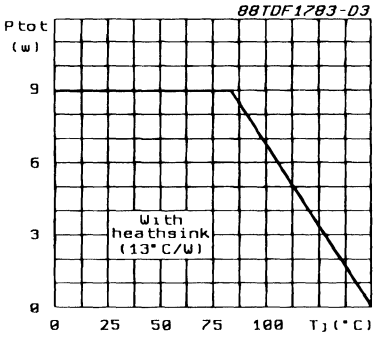


Figure 2 : Safe Operating Area : Desaturation Monitoring Maximum Programmable Delay Versus V_{CC}.

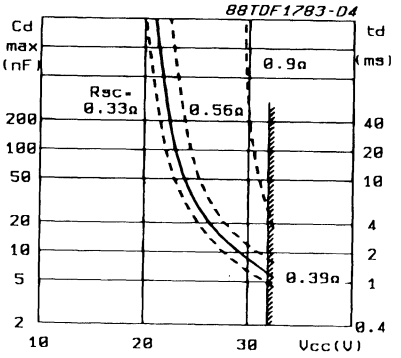


Figure 3 : Output Saturation Voltage Versus Output Current.

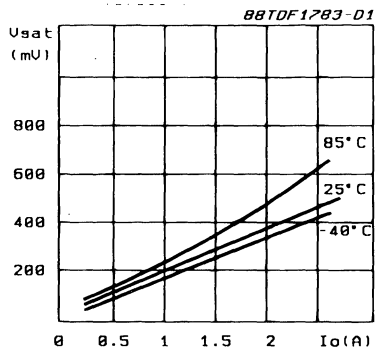
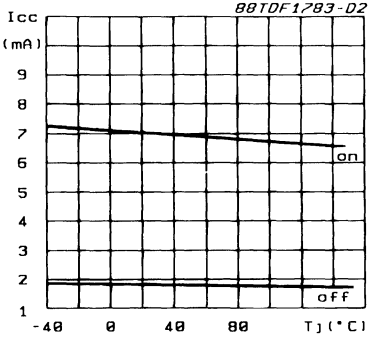
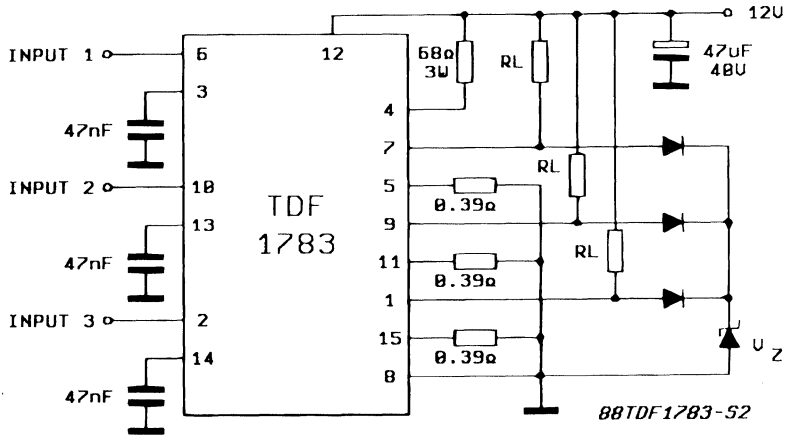


Figure 4 : Supply Current Versus Temperature.



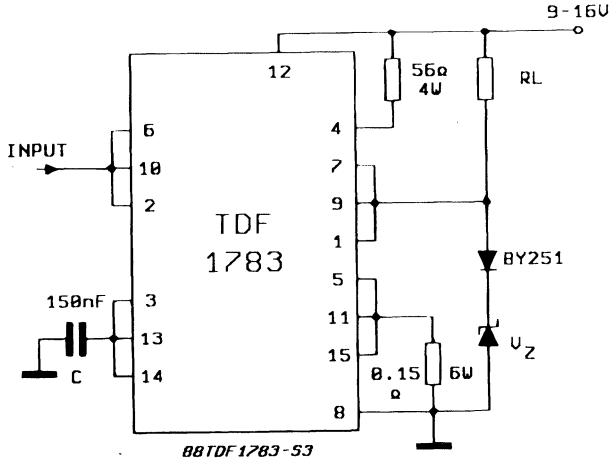
APPLICATIONS

Figure 5 : Typical Application ; Triple 1.5 A Driver.



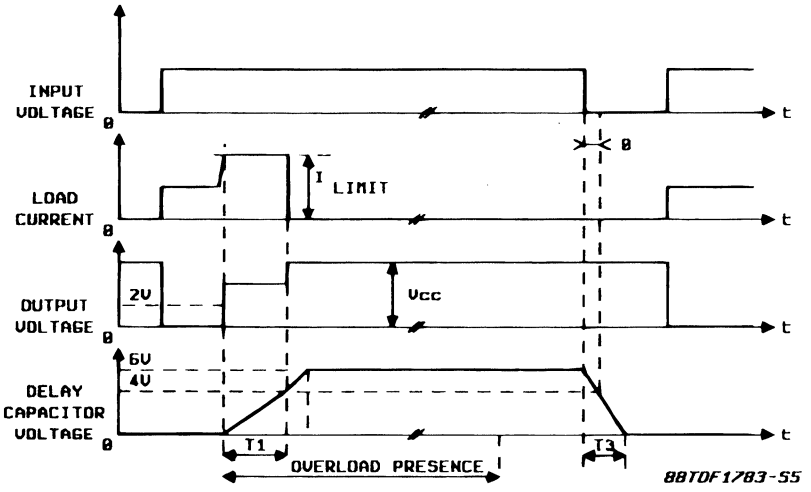
$V_{CC\ max} < V_Z \leq V_{O\ max}$

Figure 6 : Paralell Driving of Loads ; One 6 Amp. Driver.



$V_{CC\ max} < V_Z \leq V_{Z\ max}$

Figure 7 : Operating Waveforms Under Overloads Conditions.

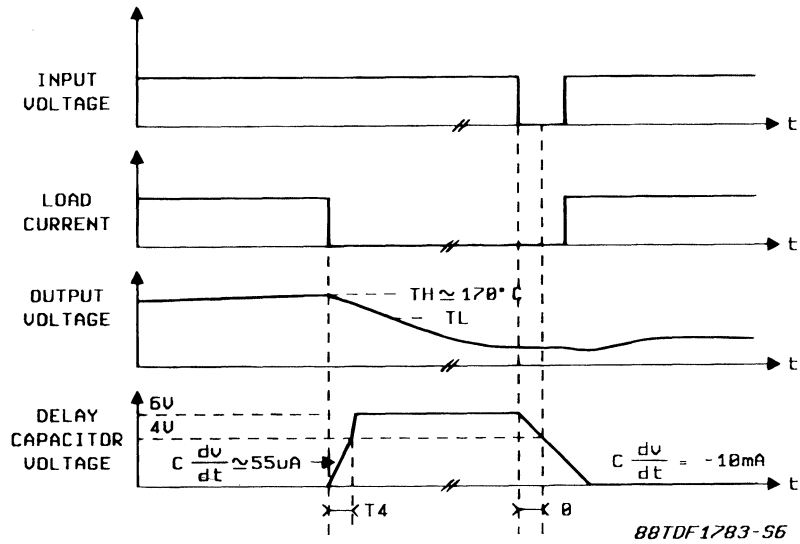


θ : MINIMUM RESET SIGNAL DURATION (θ ≈ 10 µs typ)

$\frac{Cdv}{dt}$ = 20 µA (T_1) ; $\frac{Cdv}{dt}$ = – 10 mA (T3) (typical values)

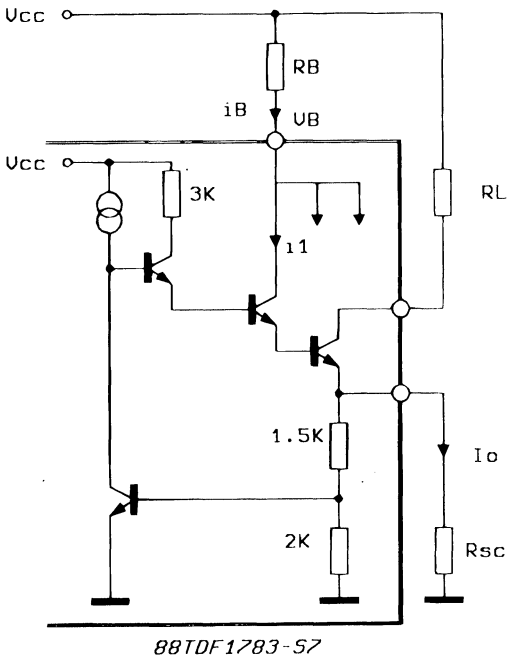
The sequence discribed above will be repeted as long as overload conditions will remain.

Figure 8 : Thermal Shutdown.



The thermal protection turns off the 3 outputs simultaneously (TH - T_L ≈ 30 °C is the thermal hysteresis). Any erratic restarts will be avoided when T_4 is shorter than the duration given by the thermal hysteresis.

Figure 9 : Output Stage and Current Limitation.



* Rsc calculation

$T_j = 150\,°C$; $V_{BE} \approx 460\,mV$

$(R_{sc}\ I_o) \cdot \frac{2}{3.5} = V_{BE}$ $\Rightarrow$ $R_{sc} \cdot I_o = 0.805\ V$

* R_B calculation

$R_B = \frac{V_{cc} - V_B}{3 \cdot i_1}$ ($V_B \approx 2\ V$, $i_1 = 50\ \mu A$ at $I_o = 1.5\ A$)

POWER DISSIPATION OF THE TDF 1783

$P = (V_{cc} \cdot I_{cc}) + n\,(V_{ce\ sat} \cdot I_o) + i_B\,(V_B - RSC \cdot I_o)$
n : number of conducting outputs
$V_{ce\ sat} = V_o - V_{RSC}$
$R_{SC} \cdot I_o = V_{RSC}$

PROTECTION AGAINST ELECTROSTATIC DISCHARGES

The inputs are designed to operate from – 30 to + 50 V. This characteristic, useful in an industrial context, guarantee an electrostatic discharge protection up to 200 V.

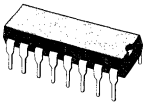
Usual cautions have to be taken to protect delay and input pins against parasitic discharges. Other pins are protected up to 2 KV.

TEA3717

STEPPER MOTOR DRIVER

- HALF-STEP AND FULL-STEP MODE
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL 5 TO 1000 mA
- WIDE VOLTAGE RANGE 10 TO 45 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CAN BE SELECTED IN STEPS OR VARIED CONTINUOUSLY

POWERDIP 12 + 2 + 2

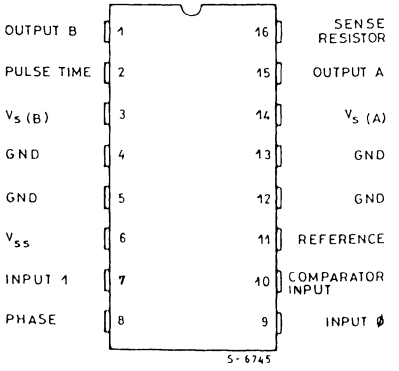


ORDER CODE : TEA3717DP

DESCRIPTION

The TEA3717 is a bipolar monolithic integrated circuit intended to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEA3717 and a few external components form a complete control and drive unit for LS-TTL or microprocessor-controlled stepper motor systems.

CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

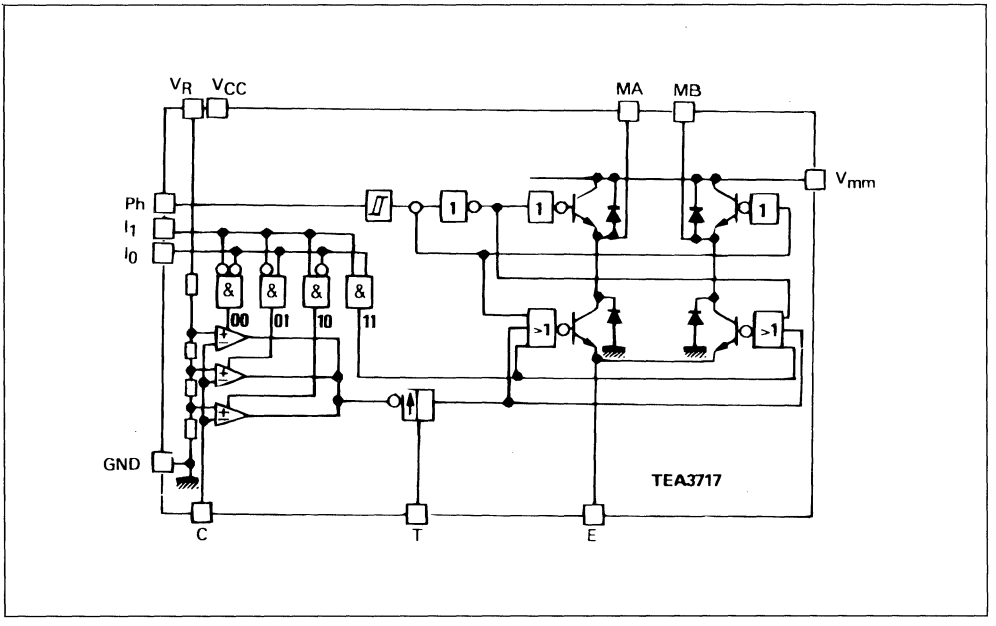
Symbol	Parameter	Value	Unit
V_{mm}	Power Supply Voltage (pins 14, 3)	45	V
V_{CC}	Logic Supply Voltage (pin 6)	7	V
	Input Voltage		V
V_{in}	Logic Inputs	− 0.5 to 6	
V_{in}	Analog Inputs	V_{CC}	
V_V	Reference Input	15	
	Input Current		mA
I_{in}	Logic Inputs	− 10	
I_{in}	Analog Inputs	− 10	
I_O	Output Current	± 1	A
T_j	Junction Temperature	+ 150	°C
T_{stg}	Storage Temperature Range	− 55 to + 150	°C
T_{oper}	Operating Ambiant Temperature Range	0 to + 70	°C

THERMAL DATA

$R_{th\ (j\text{-}c)}$	Maximum Junction-pins Thermal Resistance	11	°C/W
$R_{th\ (j\text{-}a)}$	Maximum Junction-ambient Thermal Resistance	45*	°C/W

* Soldered on a 35 mm thick 20 cm^3 PC board copper area

SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{mm}	Supply Voltage	10	–	40	V
I_o	Output Current	0.020	–	0.8	A
T_{amb}	Ambient Temperature	0	–	70	°C
t_r	Rise Time, Logic Inputs	–	–	2	µs
t_f	Fall Time, Logic Inputs	–	–	2	µs

ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V, ± 5 %, V_{mm} = + 10 V to + 40 V, T_{amb} = 0 °C to + 70 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	–	–	25	mA
V_{IH}	High Level Input Voltage - Logic Inputs	2.0	–	–	V
V_{IL}	Low Level Input Voltage - Logic Inputs	–	–	0.8	V
I_{IH}	High Level Input Current - Logic Input (V_I = + 2.4 V)	–	–	20	µA
I_{IL}	Low Level Input Current - Logic Inputs (V_I = + 0.4 V)	– 0.4	–	–	mA
V_{CH} V_{CM} V_{CL}	Comparator Threshold Voltage (V_R = + 5.0 V), I_0 = 0, I_1 = 0 I_0 = 1, I_1 = 0 I_0 = 0, I_1 = 1	390 230 65	420 250 80	440 270 90	mV
I_{CO}	Comparator Input Current	– 20	–	20	µA
I_{off}	Output Leakage Current (I_0 = 1, I_1 = 1) T_{amb} = + 25 °C T_{amb} = + 70 °C, V_S = 40 V, V_{SS} = 5 V	 – –	 – 100	 100 200	µA
V_{sat}	Total Saturation Voltage Drop (I_o = 500 mA)	–	–	4.0	V
P_{tot}	Total Power Dissipation I_o = 500 mA, f_s = 30 kHz I_o = 800 mA, f_s = 30 kHz	 – –	 1.8 3.7	 2.3 –	W
t_{off}	Cut off Time (see figure 1 and 2, V_{mm} = + 10 V, t_{on} ≥ 5 µs)	25	30	35	µs
t_d	Turn off Delay (see figure 1 and 2, T_{amb} = + 25 °C, dVC/dt ≥ 50 mV/µs)	–	1.6		µs

Figure 1 (see note).

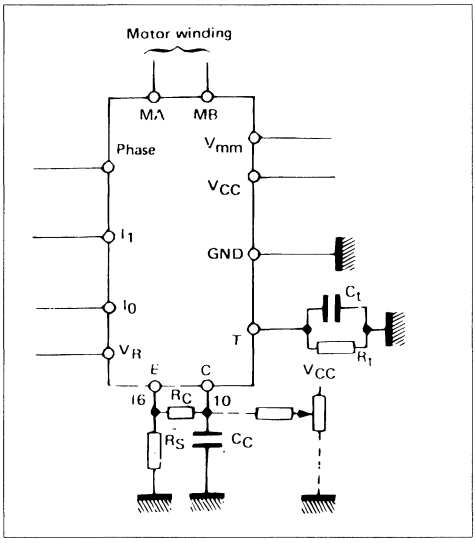
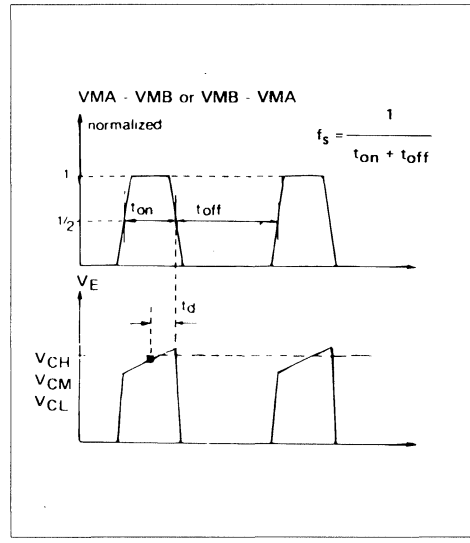


Figure 2.



FUNCTIONAL DESCRIPTION

The circuit is intented to drive a bipolar constant current through one motor winding. The constant current is generated through switch mode regulation.

There is a choice of three different current levels with the two logic inputs I_0 and I_1. The current can also be switched off completely.

INPUT LOGIC

If any of the logic inputs is left open, the circuit will treat it as a high level input.

I_0	I_1	Current Level
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	Maximum Current

PHASE – This input determines the direction of current flow in the winding, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift. High level on the PHASE-input causes the motor current flow from M_A through the winding to M_B.

Note : R_S = 1 Ω, inductance free
R_C = 1 kΩ
C_C = 820 pF, ceramic
R_t = 56 kΩ
C_t = 820 pF, ceramic

I_0 and I_1 – The current level in the motor winding is selected with these inputs. The values of the different current levels are determined by the reference voltage V_R together with the value of the sensing resistor R_S.

CURRENT SENSOR

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_0 and I_1. The motor current flows through the sensing resistor R_S. When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator output goes high, which triggers the pulse generator and its output goes high during a fixed pulse time (t_{off}), thus switching off the power feed to the motor winding, and causing the motor current to decrease during t_{off}.

SINGLE-PULSE GENERATOR

The pulse generator is a monostable triggered on the positive going edge of the comparator output.

The monostable output is high during the pulse time, t_{off}, which is determined by the timing components R_t and C_t.

$$t_{off} = 0.69 \cdot R_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.

If a new trigger signal should occur during t_{off}, it is ignored.

OUTPUT STAGE

The output stage contains four Darlington transistors and four diodes, connected in an H-bridge. The two sinking transistors are used to switch the power-supplied to the motor winding, thus driving a constant current through the winding.

It should be noted however, that it is not permitted to short circuit the outputs.

V_{CC}, V_{mm}, V_R

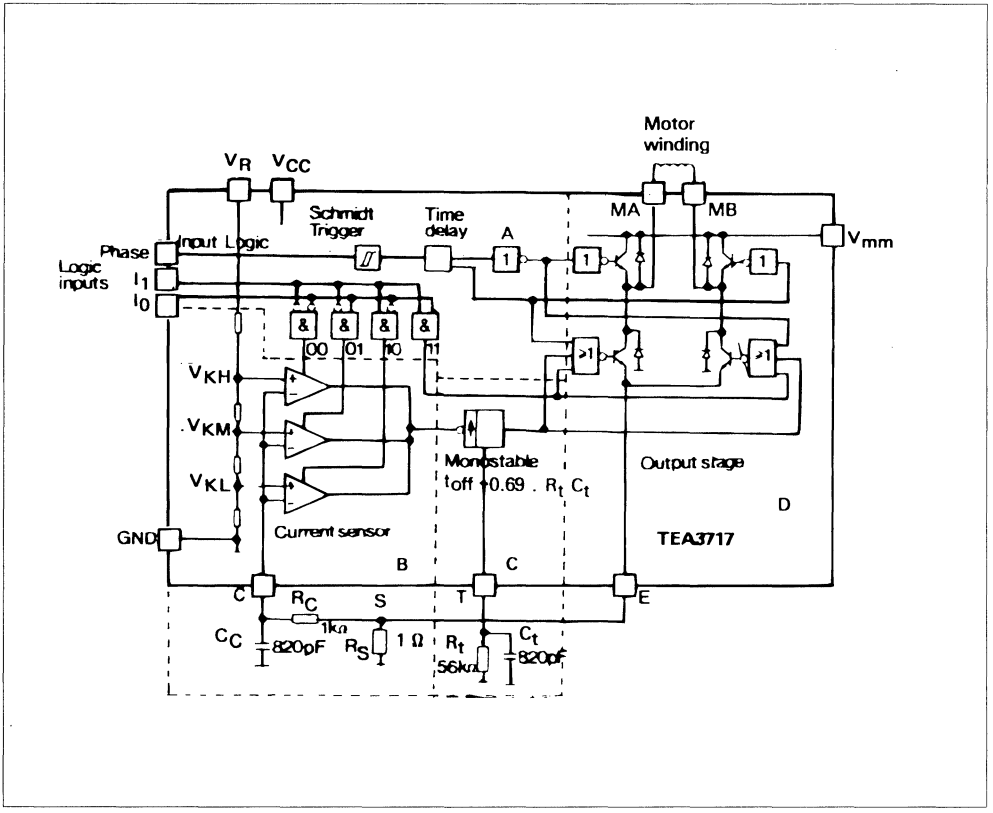
The circuit will stand any order of turn-on or turn-off of the supply voltages V_{SS} and V_S. Normal dV/dt values are then assumed.

Preferably, V_R should be tracking V_{CC} during power-on and power-off.

ANALOG CONTROL

The current levels can be varied continuously either if V_R is varied or with a circuit varying the voltage fed into the comparator terminal (see fig.1).

Figure 3.



Functional blocks
A. TTL compatible input logic
B. Current sensor
C. Single-pulse generator (monostable)
D. Output stage with protection diodes.

Figure 4 : Typical Sink Saturation Voltage vs Output Current.

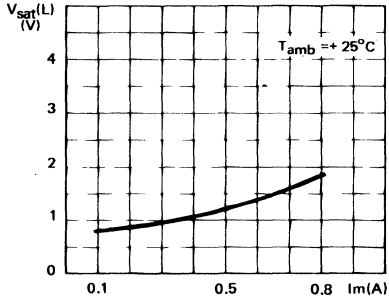


Figure 5 : Typical Source Saturation Voltage vs Output Current.

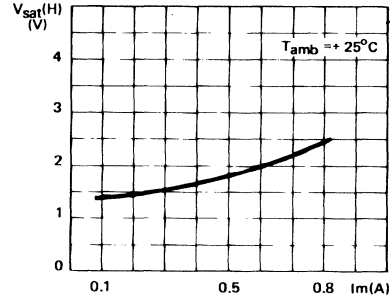
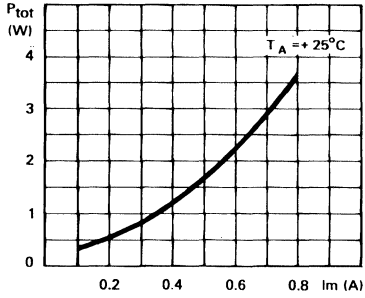


Figure 6 : Typical Power Losses vs Output Current.



TYPICAL APPLICATION

Figure 7 : Serial Printer Carriage Drive.

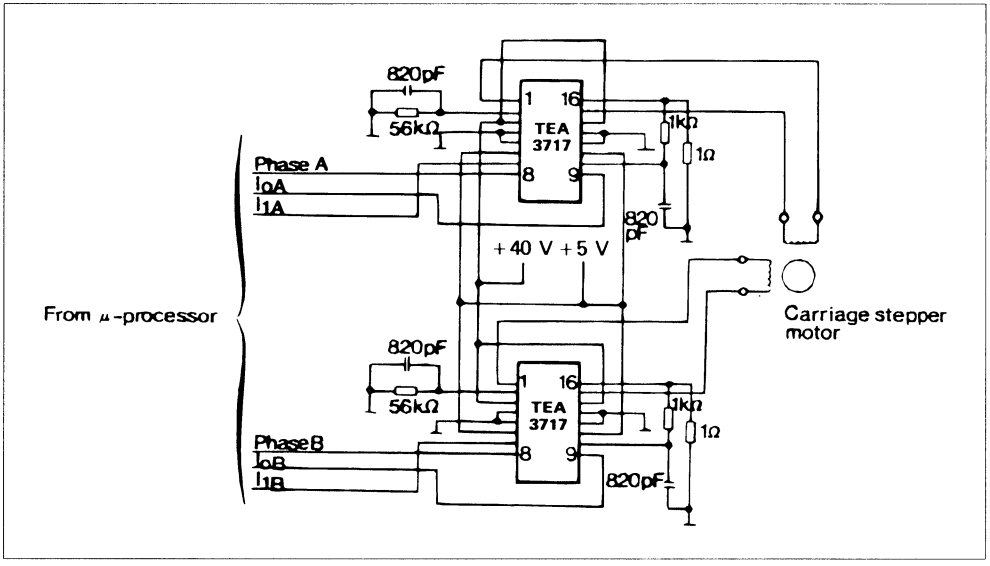
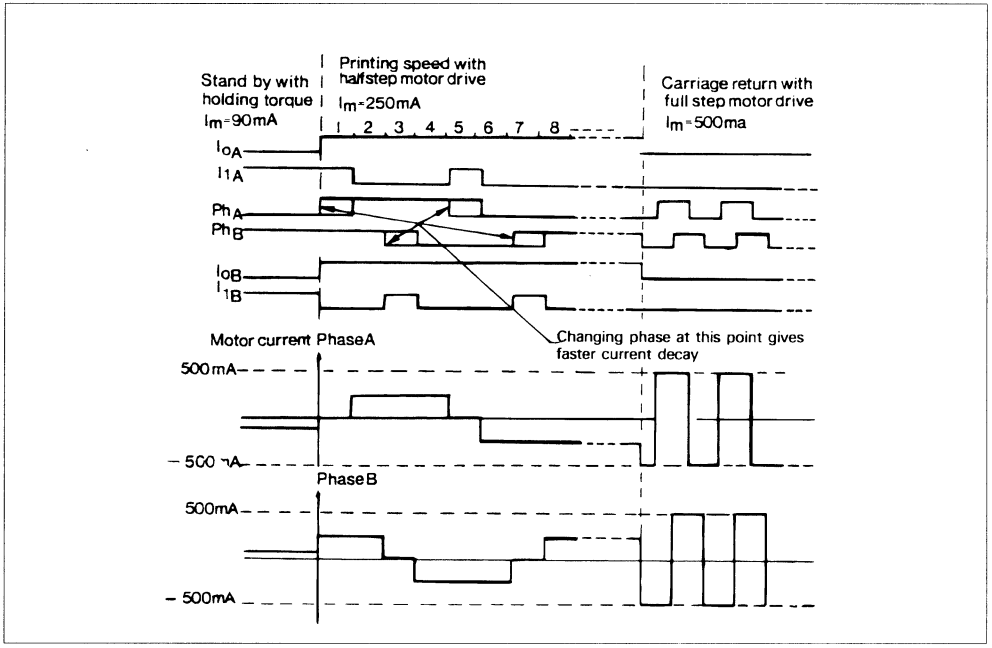


Figure 8 : Principal Operating Sequence.



SGS-THOMSON MICROELECTRONICS

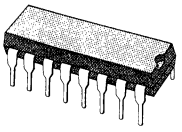
TEA3718
TEA3718S

STEPPER MOTOR DRIVER

ADVANCE DATA

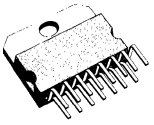
- HALF-STEP AND FULL-STEP MODE
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL 5 TO 1500 mA
- WIDE VOLTAGE RANGE 10 TO 50 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CAN BE SELECTED IN STEPS OR VARIED CONTINUOUSLY
- THERMAL OVERLOAD PROTECTION
- ALARM OUTPUT (TEA3718SP) OR PRE-ALARM OUTPUT (TEA3718SSP)

POWERDIP 12 + 2 + 2



ORDER CODES : TEA3718DP
TEA3718SDP

MULTIWATT-15



ORDER CODES : TEA3718SP
TEA3718SSP

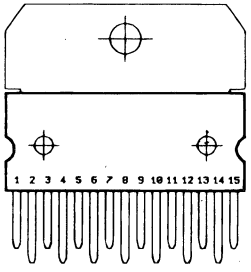
DESCRIPTION

The TEA3718 and TEA3718S are bipolar monolithic integrated circuits intended to control and drive the current in one winding of a bipolar stepper motor. The circuits consist of an LS-TTL compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEA3718 or TEA3718S and a few external components form a complete control and drive unit for LS-TTL or microprocessor-controlled stepper motor systems.

PIN CONNECTIONS (top views)

TEA3718

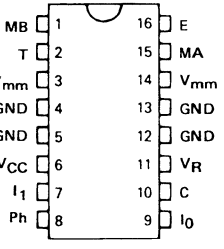
1 - V_{CC}
2 - I_1
3 - Ph
4 - I_0
5 - C
6 - V_{ref}
7 - ALARM OUT
8 - GND
9 - NC
10 - V_{mm}
11 - T
12 - MA
13 - E
14 - MB
15 - V_{mm}



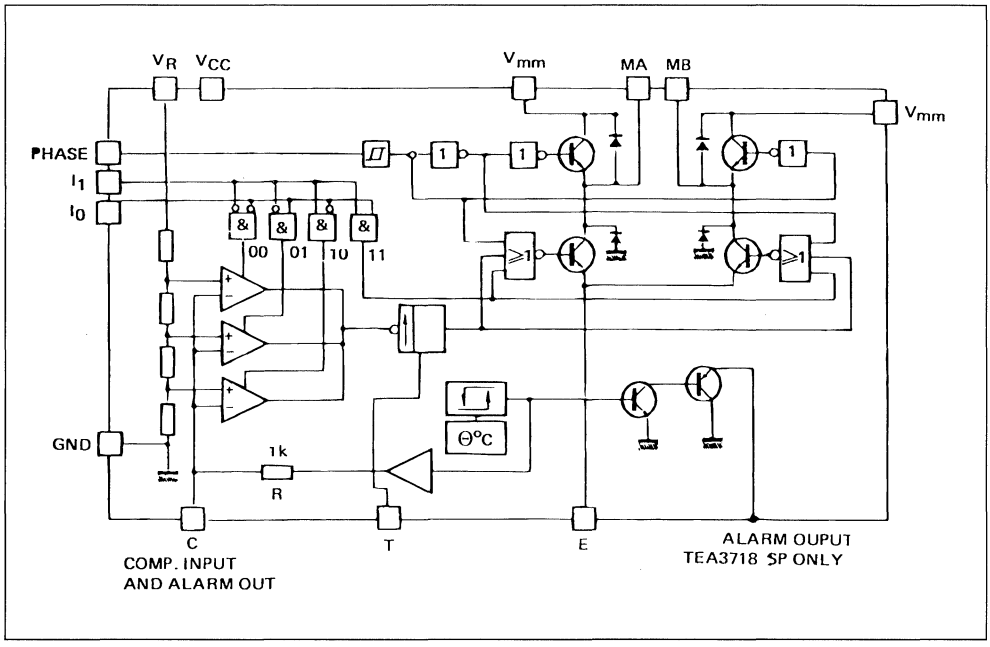
TEA3718S

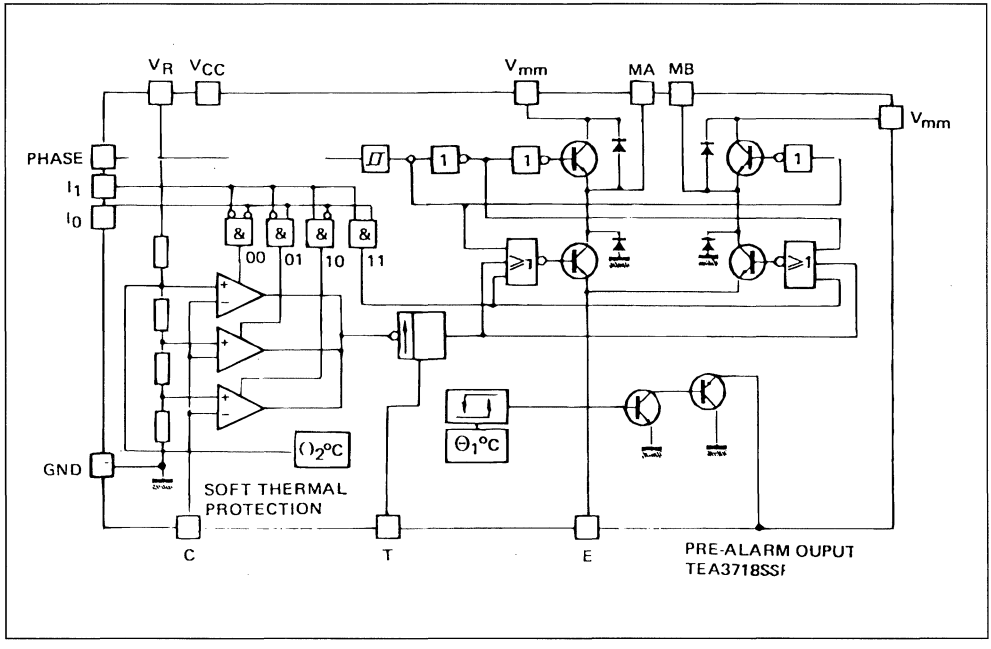
1 - V_{CC}
2 - I_1
3 - Ph
4 - I_0
5 - C
6 - V_{ref}
7 - PRE-ALARM OUT
8 - GND
9 - NC
10 - V_{mm}
11 - T
12 - MA
13 - E
14 - MB.
15 - V_{mm}

TEA3718
TEA3718S



BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7	V
V_{mm}		50	V
V_I	Input Voltage		V
	Logic Inputs	6	
	Analog Inputs	V_{CC}	
	Reference Input	15	
I_I	Input Current		mA
	Logic Inputs	− 10	
	Analog Inputs	− 10	
I_O	Output Current	± 1.5	A
T_j	Junction Temperature	+150	°C
T_{oper}	Operating Ambient Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature Range	− 55 to + 150	°C

THERMAL DATA

$R_{th\ (j\text{-}c)}$	Maximum Junction-case Thermal Resistance		°C/W
	Powerdip	11	
	Multiwatt	3	
$R_{th\ (j\text{-}a)}$	Maximum Junction-ambient Thermal Resistance		°C/W
	Powerdip	45*	
	Multiwatt	40	

* Soldered on a 35 µm thick 20 cm^2 PC board copper area.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{mm}	Supply Voltage	10	–	45	V
I_m	Output Current	0.020	–	1.2	A
T_{amb}	Ambient Temperature	0		70	°C
t_r	Rise Time Logic Inputs	–	–	2	µs
t_f	Fall Time Logic Inputs	–	–	2	µs

MAXIMUM POWER DISSIPATION

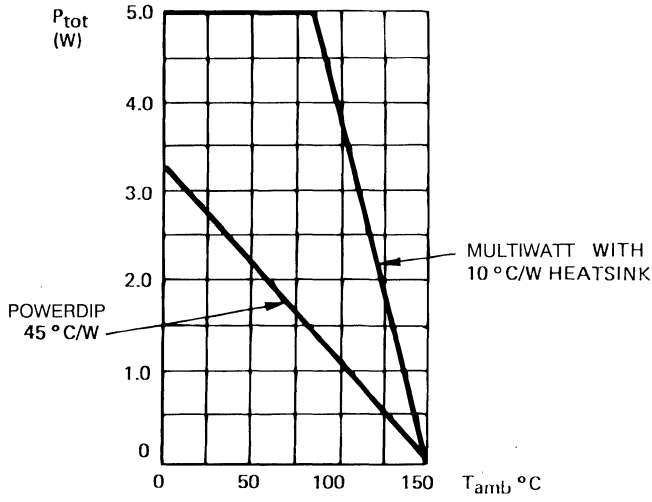
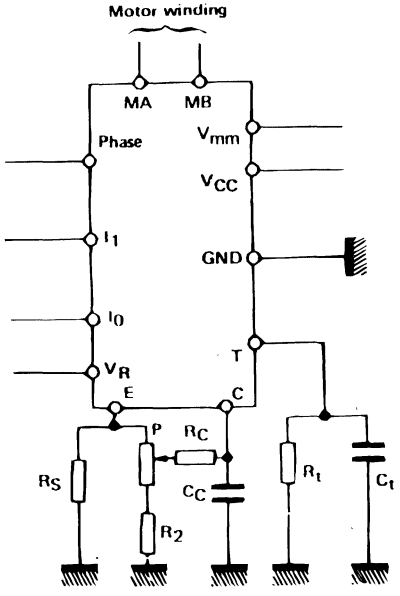


Figure 1.

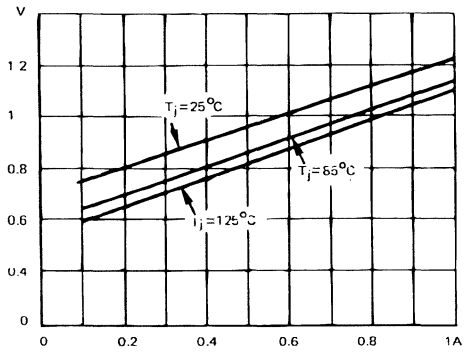


R_S = 1 Ω INDUCTANCE FREE
R_C = 470 Ω
C_C = 820 pF CERAMIC
R_t = 56 kΩ
C_t = 820 pF CERAMIC
P = 500 Ω
R_2 = 1 K

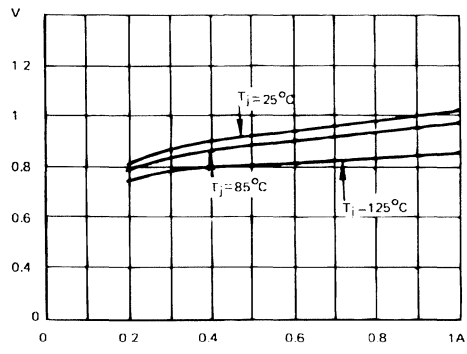
ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V, ± 5 %, V_{mm} = + 10 V to + 45 V, T_{amb} = 0 °C to + 70 °C (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
I_{CC}	Supply Current		–	–	25	mA
V_{IH}	High Level Input Voltage - Logic Inputs		2	–	–	V
V_{IL}	Low Level Input Voltage - Logic Inputs		–	–	0.8	V
I_{IH}	High Level Input Current - Logic Inputs (V_I = + 2.4 V)		–	–	20	µA
I_{IL}	Low Level Input Current - Logic Inputs (V_I = + 0.4 V)		– 0.4	–	–	mA
V_{CH}	Comparator Threshold Voltage (V_R = + 5 V)	I_O = 0, I_1 = 0	390	420	440	mV
V_{CM}		I_O = 0, I_1 = 0	230	250	270	
V_{CL}		I_O = 0, I_1 = 1	65	80	90	
I_{CO}	Comparator Input Current		– 20	–	20	µA
I_{off}	Output Leakage Current (I_O = 1, I_1 = 1, T_{amb} = + 25 °C)		–	–	100	µA
V_{sat}	Total Saturation Voltage Drop (I_m = 1 A)	Powerdip	–	–	2.8	V
		Multiwatt	–	–	3.2	
P_{tot}	Total Power Dissipation - I_m = 1 A, f_s = 30 kHz		–	3.1	3.6	W
t_{off}	Cut off Time (see figure 1 and 2, V_{mm} = + 10 V, V_{ton} > 5 µS)		25	30	35	µs
t_d	Turn off Delay (see figure 1 and 2, T_{amb} = + 25 °C, dVC/dt > 50 mV/µS)		–	1.6	–	µs
V_{sat}	Alarm Output Saturation Voltage - I_O = 2 mA (only CB-501 package)		–	0.8	–	V
I_{ref}	Reference Input Current, V_R = 5 V		–	0.4	1	mA
	Source Diode Transistor Pair					
V_{sat}	Saturation Voltage (Powerdip)	I_m = 0.5 A	–	1.05	1.2	V
		I_m = 1 A	–	1.35	1.5	
	(Multiwatt)	I_m = 0.5 A	–	–	1.3	V
		I_m = 1 A	–	–	1.7	
V_f	Diode Forward Voltage	I_f = 0.5 A	–	1.1	1.5	V
		I_f = 1 A	–	1.25	1.7	
I_{sub}	Substrate Leakage Current	I_f = 1 A	–	–	5	mA
	Sink Diode Transistor Pair					
V_{sat}	Saturation Voltage (Powerdip)	I_m = 0.5 A	–	1	1.2	V
		I_m = 1 A	–	1.2	1.3	
	(Multiwatt)	I_m = 0.5 A	–	–	1.3	V
		I_m = 1 A	–	–	1.5	
V_f	Diode Forward Voltage	I_f = 0.5 A	–	1	1.4	V
		I_f = 1 A	–	1.1	1.5	

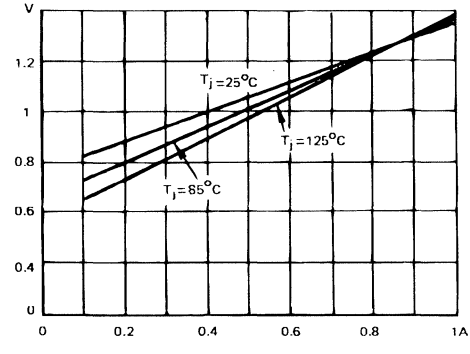
SINK DRIVER $V_{CE\ sat}$ VS I_{OUT} and T_j



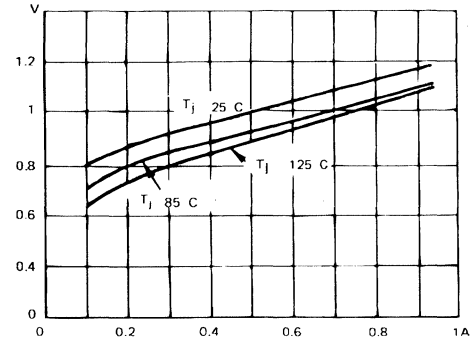
LOWER DIODE V_F VS I_{OUT} and T_J



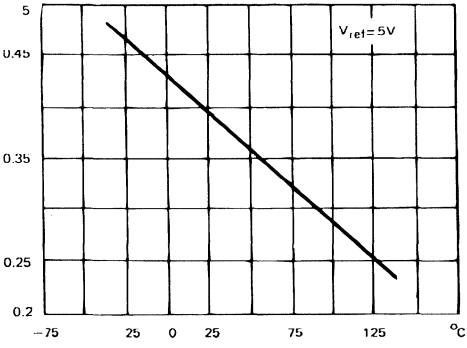
SOURCE DRIVER $V_{CE\ sat}$ VS I_{OUT} and T_j



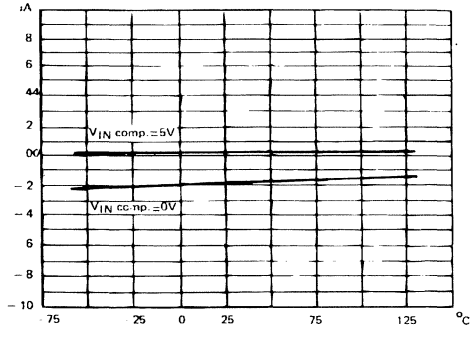
UPPER DIODE V_F VS I_{OUT} and T_j



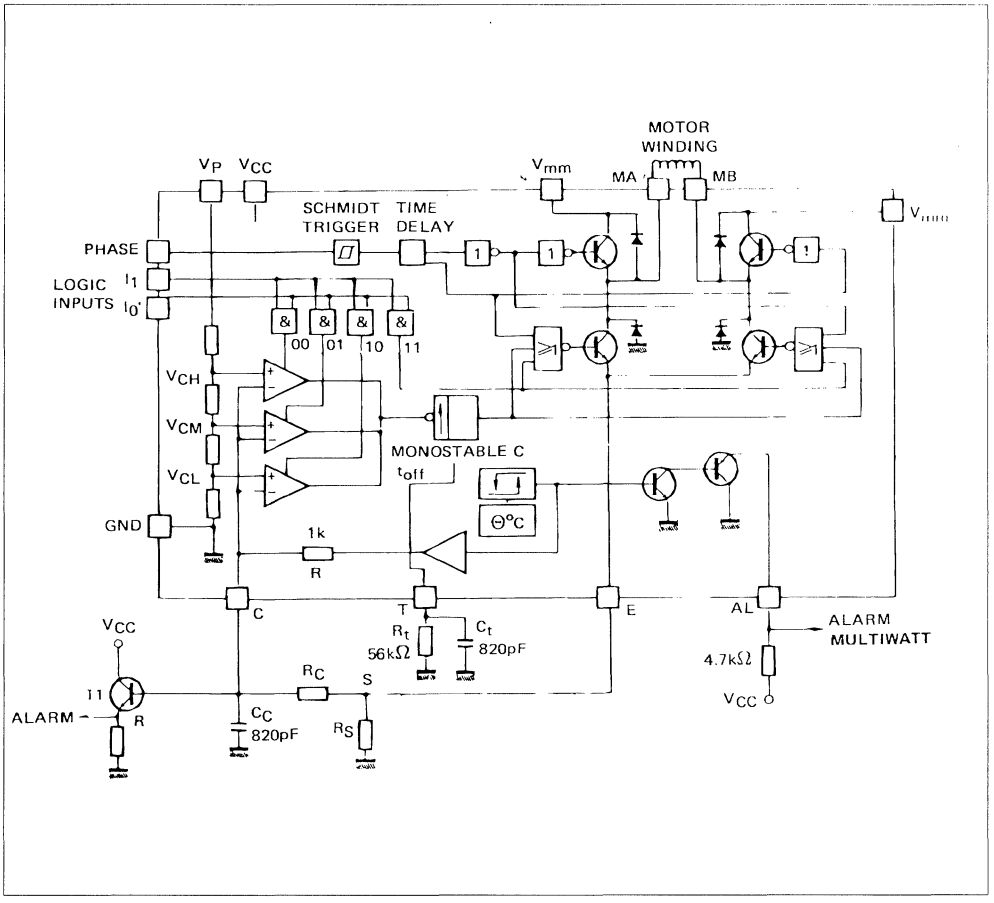
I_{ref} VS JUNCTION TEMPERATURE



COMPARATOR INPUT CURRENT VS T_j and V_C

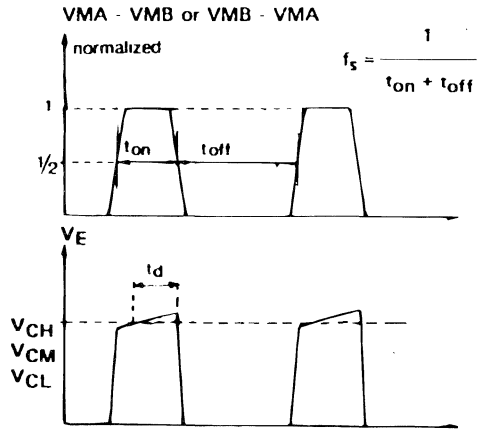


FUNCTIONAL BLOCKS



Note : T1 and R.can be omitted if MOS logic is used.

Figure 2.



FUNCTIONAL DESCRIPTION

The circuit is intented to drive a bipolar constant current through one motor winding. The constant current is generated through switch mode regulation.

There is a choice of three different current levels with the two logic inputs I_0 and I_1. The current can also be switched off completely.

INPUT LOGIC

If any of the logic inputs is left open, the circuit will treat it as a high level input.

I_0	I_1	Current Level
H	H	No Current
L	H	Low Current
H	L	Medium Current
L	L	Maximum Current

PHASE - This input determines the direction of current flow in the winding, depending on the motor connections. The signal is fed through a Schmidt-trigger for noise immunity, and through a time delay in order to guarantee that no short-circuit occurs in the output stage during phase-shift. High level on the PHASE input causes the motor current flow from M_A through the winding to M_B.

I_0 and I_1 - The current level in the motor winding is selected with these inputs. The values of the different current levels are determined by the reference voltage V_R together with the value of the sensing resistor R_S.

CURRENT SENSOR

This part contains a current sensing resistor (R_S), a low pass filter (R_C, C_C) and three comparators. Only one comparator is active at a time. It is activated by the input logic according to the current level chosen with signals I_0 and I_1. The motor current flows through the sensing resistor R_S. When the current has increased so that the voltage across R_S becomes higher than the reference voltage on the other comparator input, the comparator output goes high, which triggers the pulse generator and its output goes high during a fixed pulse time (t_{off}), thus switching off the power feed to the motor winding, and causing the motor current to decrease during t_{off}.

SINGLE-PULSE GENERATOR

The pulse generator is a monostable triggered on the positive going edge of the comparator output. The monostable output is high during the pulse time, t_{off}, which is determined by the timing components R_t and C_t.

$$t_{off} = 0.69 \cdot P_t C_t$$

The single pulse switches off the power feed to the motor winding, causing the winding current to decrease during t_{off}.

If a new trigger signal should occur during t_{off}, it is ignored.

OUTPUT STAGE

The output stage contains four Darlington transistors and four diodes, connected in an H-bridge. The two sinking transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.

It should be noted however, that it is not permitted to short circuit the outputs.

V_{CC}, V_{mm}, V_R

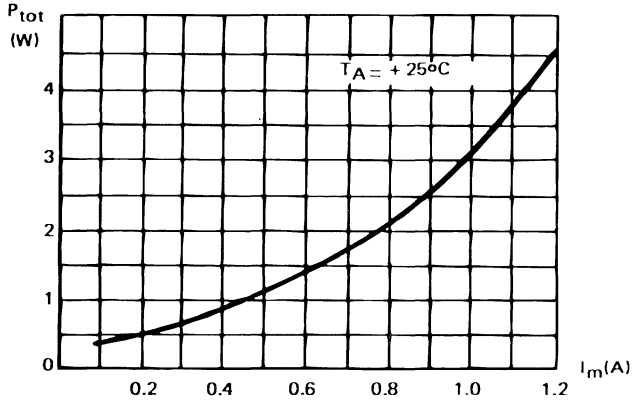
The circuit will stand any order of turn-on or turn-off the supply voltages V_{CC} and V_{mm}. Normal dV/dt values are then assumed.

Preferably, V_R should be tracking V_{CC} during power-on and power-off if V_{mm} is established.

ANALOG CONTROL

The current levels can be varied continuously if V_R is varied or with a circuit varying the voltage on the comparator terminal.

POWER LOSSES V_S OUTPUT CURRENT



ALARM OUTPUTS (TEA3718)

When an alarm condition occurs part of the V_{CC} supply voltage (dividing bridge R - R_C) is fed to the comparators input pin.

On alarm condition the comparator input voltage V_C will become higher than V_{ch}, thus switching off the output stage. A circuit may monitor the voltage V_C to detect the action of the thermal protection (fig. A)

For MW package the alarm output goes low if an alarm condition occurs (fig. B).

Figure A : Alarm Detection For Dil Package.

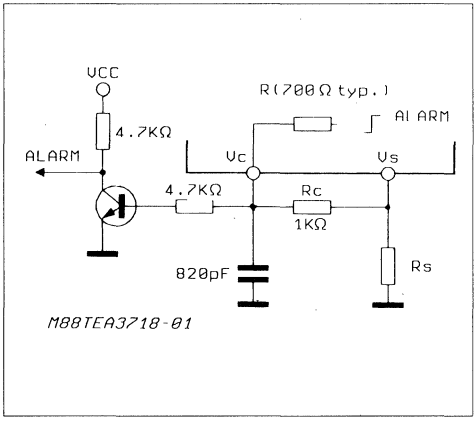
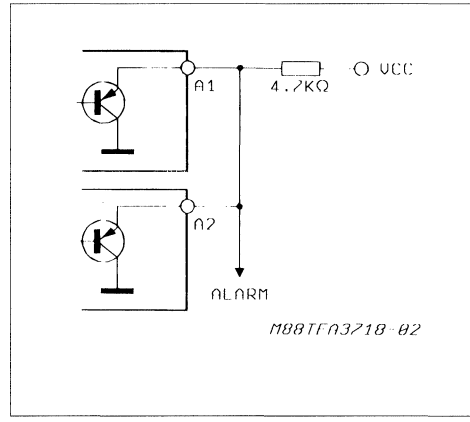


Figure B : Common Detection For Several Multiwatt Packages.



Depending of the RC value, the behaviour of the circuit is different on alarm condition :

1) RC > 80 Ω
   The output stage is switched off.
2) RC < 60 Ω (see figures C and D)
   The current I_{MM} in the winding is reduced according to the approximate formula :

$$I_{MM} = \frac{V_{TH}}{R_S} - \frac{V_{CC}}{R + R_C} \cdot \frac{R_C}{R_S}$$

with : V_{TH} = Threshold of the comparator (V_{CH}, V_{CM} or V_{CL})
R = 700 Ω (typical).

Figure C : (typical curve) Current Reduction In The Motor On Alarm Condition.

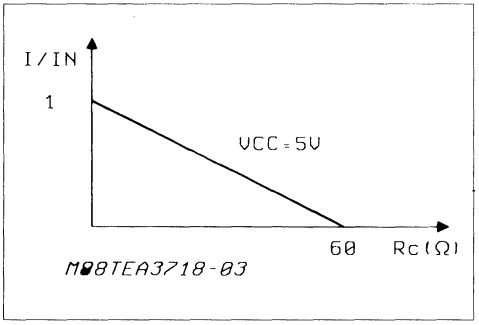
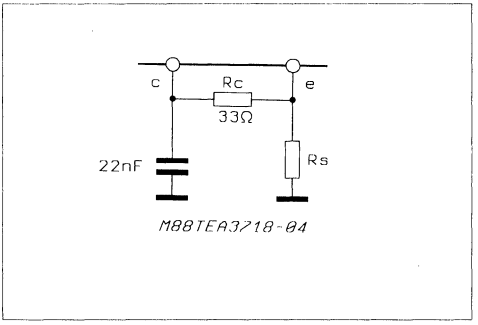


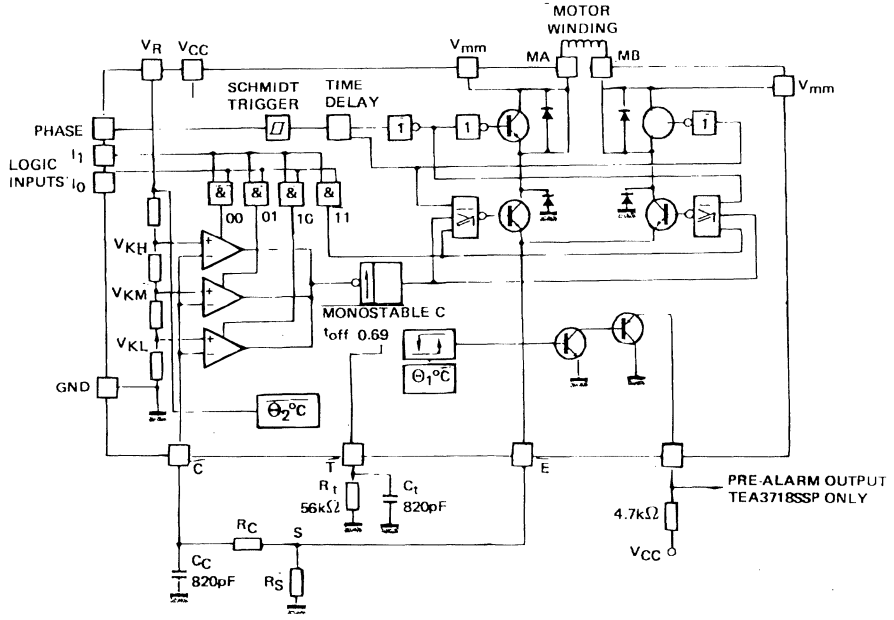
Figure D : (V_{ref} 5V)Block Diagram For Half Current On Alarm Condition.



Notes : 1. Resistance values given here are for the V_{ch} threshold. They should be adjusted using other comparators threshold or other V_{ref} value.

PRE-ALARM OUTPUT (TEA3718SSP)

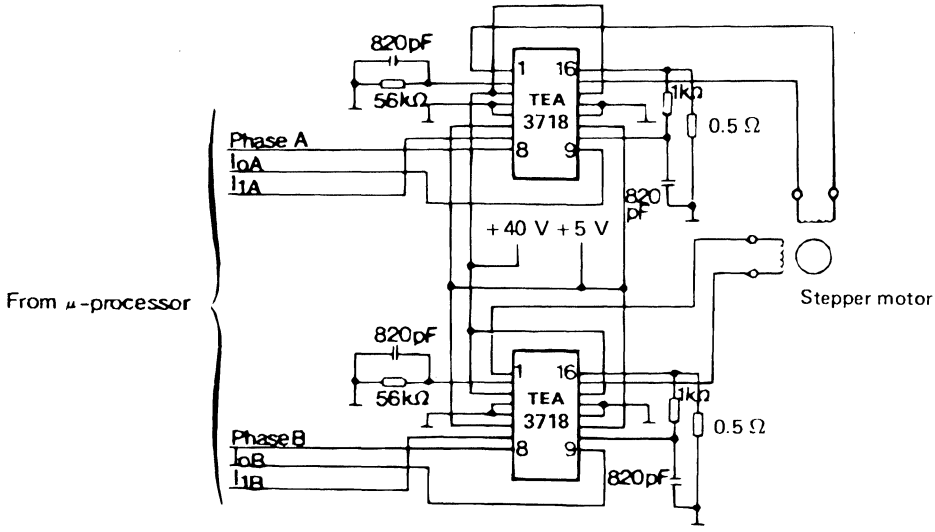
TEA3718S



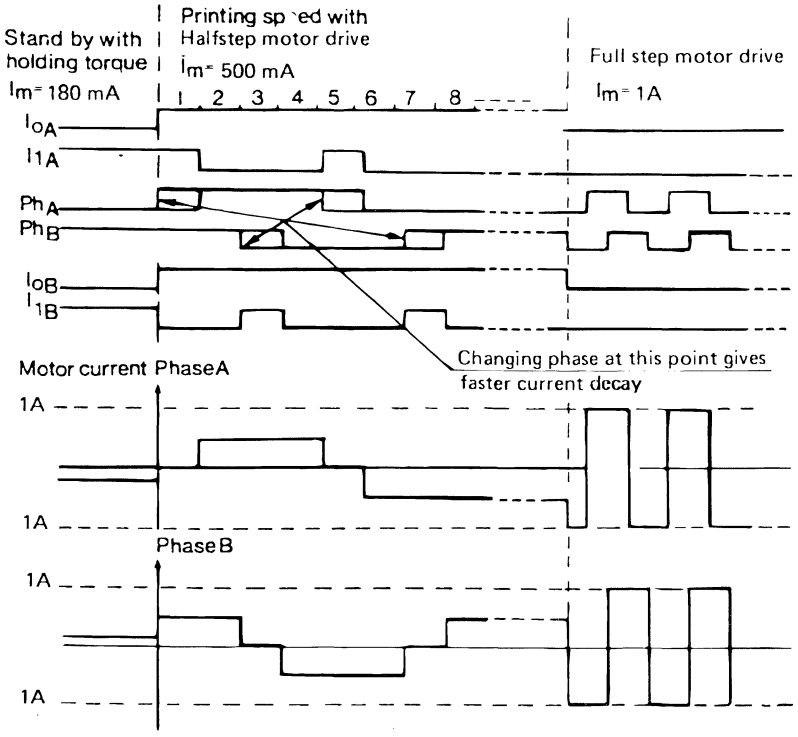
2. When changing R_C C_C should be adjusted to keep the same R_C C_C value.

- Pré-alarm output becomes low when junction temperature reaches θ1 (θ1 typ = 170 °C).

TYPICAL APPLICATION



PRINCIPAL OPERATING SEQUENCE



APPLICATION NOTES

MOTOR SELECTION

Some stepper motors are not designed for continuous operation at maximum current. As the circuit drives a constant current through the motor, its temperature might increase exceedingly both at low and high speed operation.

Also, some stepper motors have such high core losses that they are not suited for switch mode current regulation.

UNUSED INPUTS

Unused inputs should be connected to proper voltage levels in order to get the highest noise immunity.

INTERFERENCE

As the circuit operates with switch mode current regulation, interference generation problems might arise in some applications. A good measure might then be to decouple the circuit with a 15 nF ceramic capacitor, located near the package between power line V_{mm} and ground.

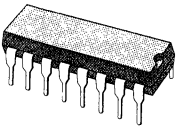
The ground lead between R_S, C_C and circuit GND should be kept as short as possible. This applies also to the lead between the sensing resistor R_S and point S, see FUNCTIONAL BLOCKS.

SGS-THOMSON
MICROELECTRONICS

TEF3718
TEF3718S

STEPPER MOTOR DRIVER

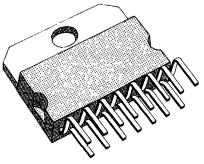
- HALF AND FULL-STEP MODES
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL : 5 TO 1500 mA
- WIDE VOLTAGE RANGE : 10 TO 50 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CAN BE SELECTED IN STEPS OR VARIED CONTINUOUSLY
- THERMAL OVERLOAD PROTECTION
- ALARM OUTPUT (TEF3718SP) OR PREA-LARM OUTPUT (TEF3718SSP)



POWERDIP 12 + 2 + 2

ORDER CODE :

TEF3718DP TEF3718SDP



MULTIWATT 15

ORDER CODE :

TEF3718SP TEF3718SSP

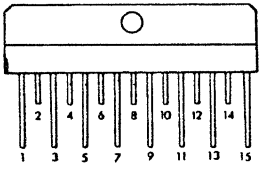
DESCRIPTION

The TEF3718 and TEF3718S are bipolar monolithic integrated circuits intended to control and drive the current in one widing of a bipolar stepper motor. The circuits consists of an LS-TLL - compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two TEF3718 or TEF3718S and a few external components form a complete control and drive unit for LS-TTL or microprocessor controlled stepper motor systems.

PIN CONNECTON

TEF3718

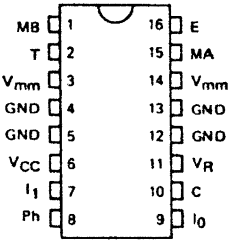
1 - V_{CC}
2 - I_1
3 - Ph
4 - I_O
5 - C
6 - V_{ref}
7 - ALARM OUT
8 - GND
9 - NC
10 - V_{mm}
11 - T
12 - MA
13 - E
14 - MB
15 - V_{mm}



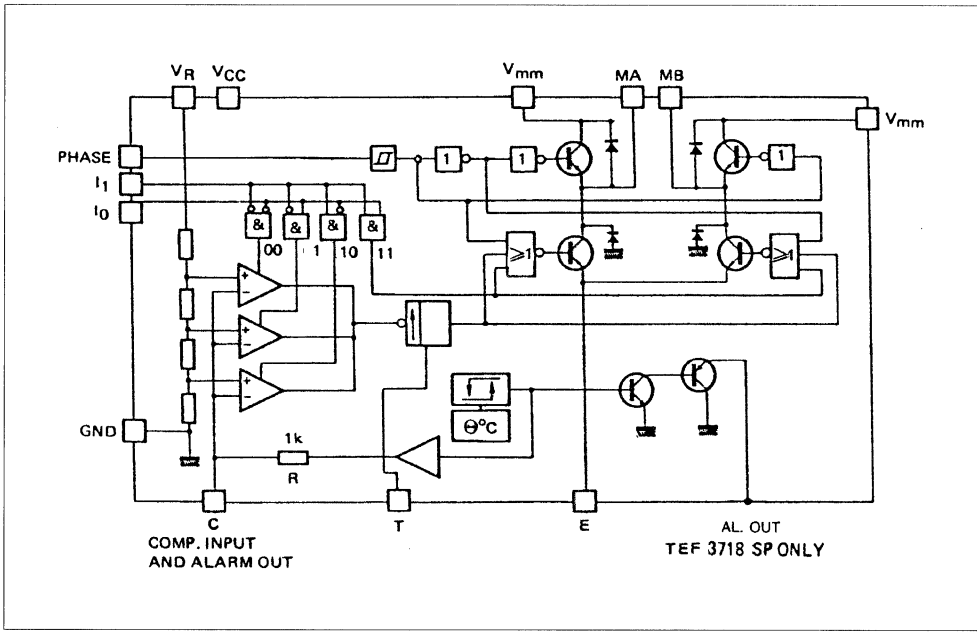
TEF3718S

1 - V_{CC}
2 - I_1
3 - Ph
4 - I_O
5 - C
6 - V_{ref}
7 - PRE-ALARM OUT
8 - GND
9 - NC
10 - V_{mm}
11 - T
12 - MA
13 - E
14 - MB
15 - V_{mm}

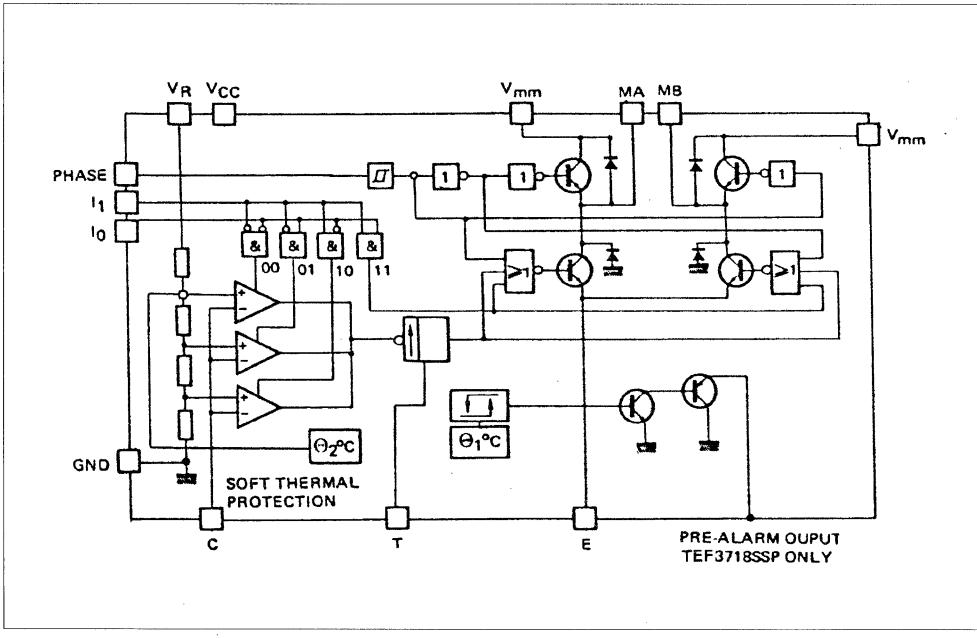
TEF3718
TEF3718S



BLOCK DIAGRAM (TEF3718)



BLOCK DIAGRAM (TEF3718S)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC} V_{MM}	Supply Voltage	7 50	V
V_I	Input Voltage : Logic Inputs Analog Inputs Reference Input	 6 V_{CC} 15	V
I_I	Input Current : Logic Inputs Analog Inputs	 10 10	mA
I_O	Output Current	± 1.5	A
T_j	Junction Temperature	+ 150	C
T_{oper}	Operating Ambient Temperature Range	– 40 to + 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Maximum Junction-case Thermal Resistance	POWERDIP MULTIW	11 3	°C/W
$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	POWERDIP MULTIW	45 (*) 40	°C/W

(*) Soldered on a 35 µm thick 20 cm^2 PC board cooper area.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC} V_{MM}	Supply Voltage	4.75 10	5 –	5.25 45	V
I_m	Output Current	0.020	–	1.2	A
T_{amb}	Ambient Temperature	– 40	–	85	°C
t_r	Rise Time Logic Inputs	–	–	2	µs
t_f	Fall Time Logic Inputs	–	–	2	µs

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V ± 5 %. V_{MM} = – 10 V to + 45 V. T_{amb} = – 40 C to + 85 °C (Unless otherwise specified)

Symbol	Characteristics			Min.	Typ.	Max.	Unit
I_{CC}	Supply Current					25	mA
V_{IH}	High Level Input Voltage Logic Input			2			V
V_{IL}	Low Level Input Voltage Input					0.7	V
I_{IH}	High Level Input Current Logic Input (V_I = 2.4 V)					20	µA
I_{IL}	Low Level Input Current Logic Input (V_I = 0.4 V)			0.4			µA
V_{CH} V_{CM} V_{CL}	Comparator Treshold Voltage (V_R = + 5 V)		I_O = 0 I_1 = 0 I_O = 1 I_1 = 0 I_O = 0 I_1 = 1	390 230 65	420 250 80	440 270 90	mV
I_{CO}	Comparator Input Current			- 20		20	µA
I_{off}	Output Leakage Current (I_O 1, I1 = 1)					100	µA
V_{sat}	Total Saturation Voltage Drop (I_m = 1 A,)		POWERDIP MULTIWATT			2.9 3.3	V
P_{tot}	Total Power Dissipation (I_m = 1 A, f_s = 30 kHz)				3.1	3.6	W
t_{off}	Cutt off Time (see figures 1 and 2 V_{mm} = + 10 V, $V_{ton} \leq$ 5 µs)			25	30	35	µs
t_d	Turn off Delay (see figures 1 and 2, T_{amb} =+ 25 °C dVC/dt ≤ 50 mV/µs)				1.6		µs
V_{sat}	Alarm Output Saturation Voltage I_O = 2 mA				0.8		V
I_{ref}	Reference Input Current, V_R = 5 V				0.4	1	mA
V_{sat}	Source Diode Transistor Pair	MULTIWATT	I_m = 0.5 A I_m = 1 A			1.35 1.75	mA
	Saturation Voltage	POWERDIP	I_m = 0.5 A I_m = 1 A			1.25 1.55	
V_f	Diode Forward Voltage		I_f = 0.5 A I_f = 1 A			1.5 1.7	
I_{sub}	Substrate Leakage Current		I_f = 1 A			10	
	Sink Diode Transistor Pair	MULTIWATT	I_m = 0.5 A I_m = 1 A			1.35 1.55	
V_{sat}	Saturation Voltage	POWERDIP	I_m = 0.5 A I_m = 1 A			1.25 1.35	
V_f	Diode Forward Voltage		I_f = 0.5 A I_f = 1 A			1.5 1.8	

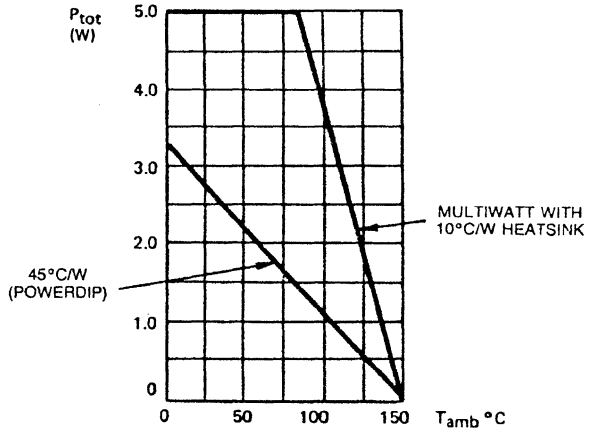
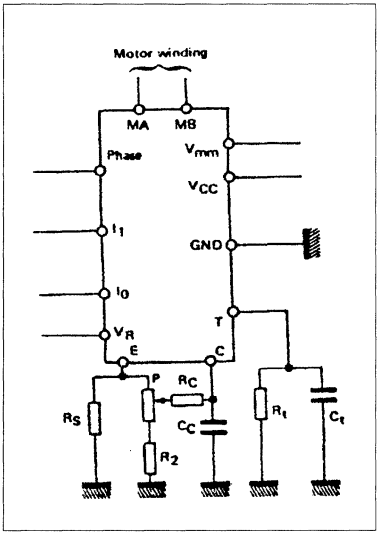
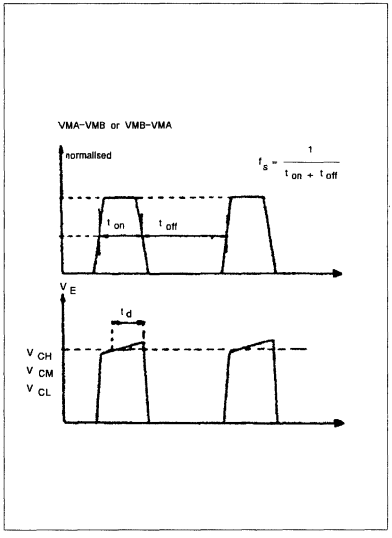


Figure 1.



R_S = 1 Ω inductance free
R_C = 470 Ω
C_C = 820 pF ceramic
R_t = 56 kΩ
C_t = 820 pF ceramic
P = 500 Ω
R_2 = 1 K

Figure 2.



SUPPLY VOLTAGE SUPERVISORS

- POWER-ON RESET GENERATOR
- AUTOMATIC RESET GENERATION AFTER VOLTAGE DROP
- WIDE SUPPLY VOLTAGE RANGE ... 3 V TO 18 V
- PRECISION VOLTAGE SENSOR
- TEMPERATURE-COMPENSATED VOLTAGE REFERENCE
- TRUE AND COMPLEMENT RESET OUTPUTS
- EXTERNALLY ADJUSTABLE PULSE WIDTH

DESCRIPTION

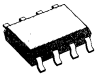
The TL7700A series are monolithic integrated circuit supply voltage supervisors specifically designed for use as reset controllers in microcomputer and microprocessor systems. During power-up the device tests the supply voltage and keeps the RESET and $\overline{\text{RESET}}$ outputs active (high and low, respectively) as long as the supply voltage has not reached its nominal voltage value. Taking $\overline{\text{RESIN}}$ low has the same effect. To ensure that the microcomputer system has reset, the TL7700A then initiates an internal time delay that delays the return of the reset outputs to their inactive states. Since the time delay for most microcomputers and microprocessors is in the order of several machine cycles, the device internal time delay is determined by an external time delay is determined by an external capacitor connected to the C_T input (pin 3).

$t_d = 1.3 \times 10^4 \times C_T$

Where : C_T is in farads (F) and t_d in seconds (s). In addition, when the supply voltage drops below the nominal value, the outputs will be active until the supply voltage returns to the nominal value. An external capacitor (typically 0.1 µF) must be connected to the REF output (pin 1) to reduce the influence of fast transients in the supply voltage.

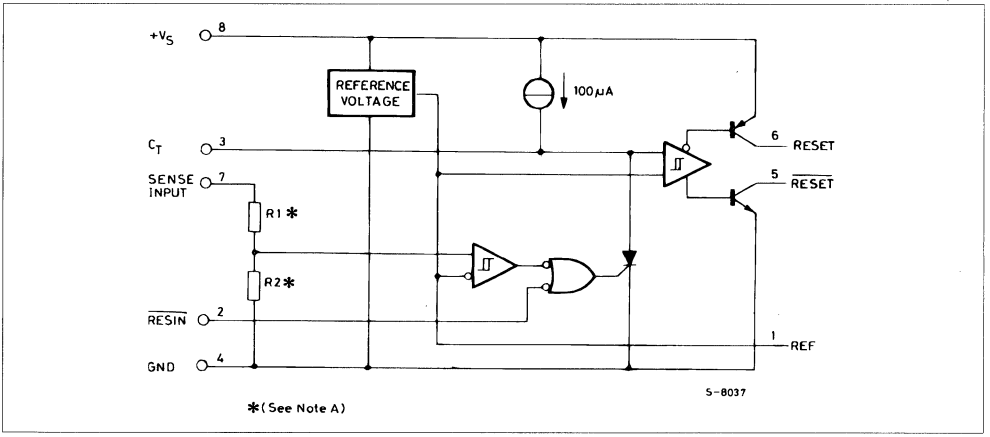
The TL7700AI series is characterized for operation from – 25°C to 85°C ; the TL7700AC series is characterized from 0°C to 70°C.

Plastic Minidip



SO-8 J

BLOCK DIAGRAM



* TL7702A R1 = 0Ω, R2 = open ; TL7705A R1 = 7.8 KΩ, R2 = 10 KΩ ; TL7709A R1 = 19.7 KΩ, R2 = 10 KΩ ; TL7712A R1 = 32.7 KΩ, R2 = 10 KΩ ; TL7715A R1 = 43.4 KΩ, R2 = 10 KΩ.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage, V_{CC} (see note 1)	20	V
V_i	Input Voltage Range at $\overline{RESIN}$	– 0.3 to 20	V
V_i	Input Voltage at SENSE : TL7702A (see note 2) TL7705A TL7709A TL7712A TL7715A	– 0.3 to 6 – 0.3 to 10 – 0.3 to 15 – 0.3 to 20 – 0.3 to 20	V V V V V
I_{OH}	High-level Output Current at RESET	– 30	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$	30	mA
T_{amb}	Operating Free-air Temperature Range : TL77XXAI TL77XXAC	– 25 to 85 0 to 70	°C °C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

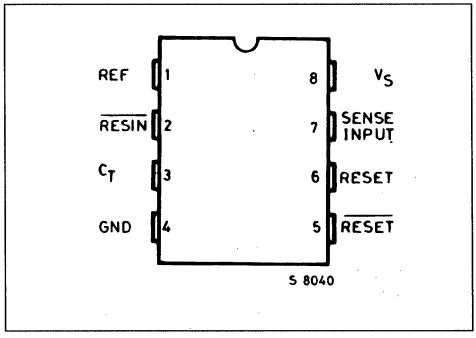
Notes : 1. All voltage values are with respect to the network ground terminal.
2. For the TL7700A, the voltage applied to the SENSE terminal must never exceed V_S.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Max.	Unit
V_S	Supply Voltage		3.6	18	V
V_{IH}	High-level Input Voltage at RESIN		2		V
V_{IL}	Low-level Input Voltage at RESIN			0.6	V
V_i	Voltage at Sense Input	TL7702A	0	See Note 3	V
		TL7705A	0	10	
		TL7709A	0	15	
		TL7712A	0	20	
		TL7715A	0	20	
I_{OH}	High-level Output Current at RESET			– 16	mA
I_{OL}	Low-level Output Current at $\overline{RESET}$			16	mA
T_{amb}	Operating Free-air Temperature Range	TL77 - AI	– 25	85	°C
		TL77 - AC	0	70	

Note : 3. For proper operation of the TL7702A, the voltage applied to the SENSE terminal should not exceed V_S – 1 V or 6 V, whichever is less.

CONNECTION DIAGRAM AND ORDER CODE



Temperature Range	Plastic Minidip	SO-8
Commercial 0 to 70 °C	TL77XXACP	TL77XXACD
Industrial – 40 to 85 °C	TL77XXAIP	TL77XXAID

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	120	°C/W

ELECTRICAL CHARACTERISTICS these specifications unless otherwise specified, apply for : T_{amb} = – 25 to 85 °C (TLXXAI) ; T_{amb} = 0 to 70 °C (TL77XXAC)

Symbol	Parameter		Test Conditions (1)	Min.	Typ.	Max.	Unit
V_{OH}	High-level Output Voltage at RESET		I_{OH} = – 16 mA	V_S–1.5			V
V_{OL}	Low-Level Output Voltage at $\overline{RESET}$		I_{OL} = 16 mA			0.4	V
V_{ref}	Reference Voltage		T_{amb} = 25 °C	2.48	2.53	2.58	V
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C	2.48	2.53	2.58	V
		TL7705A		4.5	4.55	4.6	
		TL7709A		7.5	7.6	7.7	
		TL7712A		10.6	10.8	11.0	
		TL7715A		13.2	13.5	13.8	
V_T	Threshold Voltage at SENSE Input	TL7702A	V_S = 3.6 V to 18 V	2.45	2.53	2.58	V
		TL7705A		4.45	4.55	4.6	
		TL7709A		7.4	7.6	7.7	
		TL7712A		10.4	10.8	11.0	
		TL7715A		13.0	13.5	13.8	
V_{T+}, V_{T-}	Hysteresis (2) at SENSE Input	TL7702A	V_S = 3.6 V to 18 V T_{amb} = 25 °C		10		mV
		TL7705A			15		
		TL7709A			20		
		TL7712A			35		
		TL7715A			45		
I_I	Input Current at $\overline{RESIN}$ Input		V_i = 2.4 V to V_S			20	µA
			V_I = 0.4 V			– 100	
I_I	Input Current at SENSE Input	TL7702A	$V_{ref} < V_i < V_S$ –1.5 V		0.5	2	
I_{OH}	High-level Output Current at $\overline{RESET}$		V_O = 18 V			50	
I_{OL}	Low-level Output Current at RESET		V_O = 0 V			– 50	
I_S	Supply Current		All Inputs and out. open		1.8	3.3	mA

Notes : 1. All characteristics are measured with C = 0.1 µF from Pin 1 to GND, and with C = 0.1 µF from Pin 3 to GND.
2. Hysteresis is the difference between the positive going input threshold voltage. V_{T+}, and the negative going input threshold voltage, V_{T-}.

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{pi}	Pulse Width at SENSE Input	$V_{ih} = V_{ityp} + 0.04 \times V_i$ $V_{iL} = V_{ityp} - 0.04 \times V_i$	0.9			µs
t_{pi}	Pulse Width at $\overline{RESIN}$ Input		0.4			µs
t_{po}	Pulse Width at Output	$C_f = 0.1$ µF	0.65	1.3	2.6	ms
t_{pdHL}	Propagation Delay Time from $\overline{RESIN}$ to $\overline{RESET}$	$C_L = 100$ pF $V_S = 5$ V $R_L = 4.7$ KΩ			1	µs
$t_{r/f}$	Rise/Falltime at $\overline{RESET}$ and $\overline{RESET}$	$C_L = 10$ pF $V_S = 5$ V $R_L = 4.7$ KΩ			1	µs

Figure 1 : Multiple Power Supply System Reset Generation.

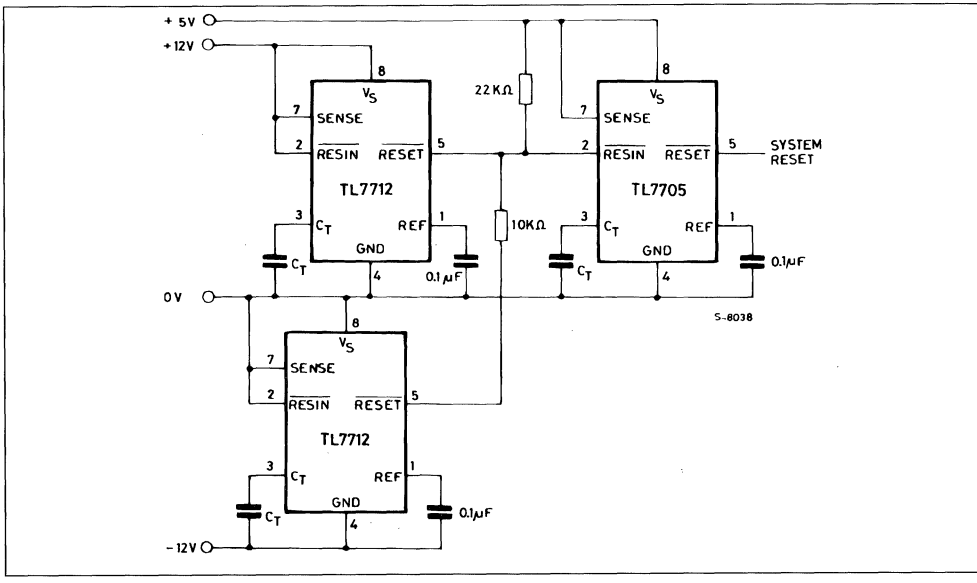
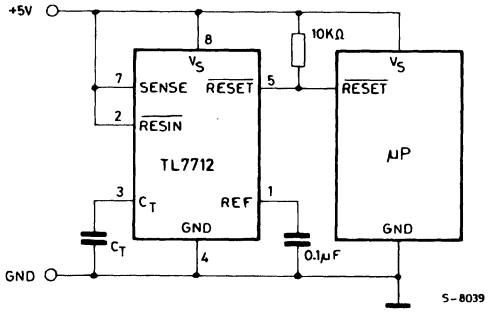


Figure 2 : Reset Controller for µP.

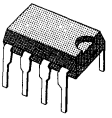


SGS-THOMSON MICROELECTRONICS

TS271

CMOS SINGLE OPERATIONAL AMPLIFIERS

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{set}
- VERY LARGE I_{set} RANGE
- PIN COMPATIBLE TO SINGLE OPERATIONAL AMPLIFIER (UA776)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



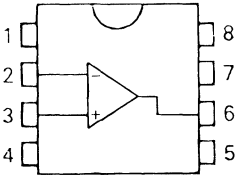
N
DIP8
(Plastic Package)

J
CERDIP8
(Cerdip Package)

D
SO8
(Plastic Micropackage)

(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS271-01

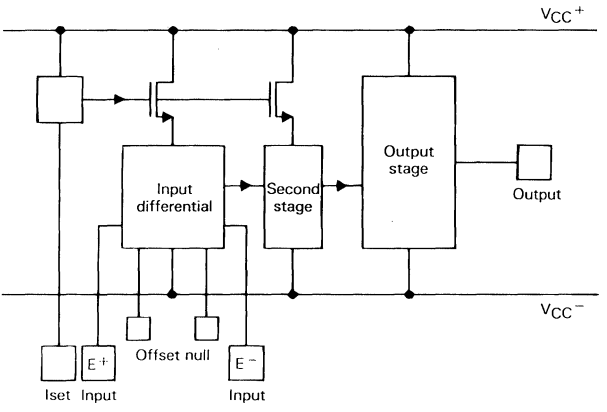
1 – Offset null 1
2 – Inverting input
3 – Non-inverting input
4 – V_{CC}^-
5 – Offset null 2
6 – Output
7 – V_{CC}^+
8 – I_{set}

DESCRIPTION

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.
The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and the consumption can be minimized according to the needed speed. These devices are specified for the following I_{set} current values : 1.5 µA, 25 µA, 130 µA.

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

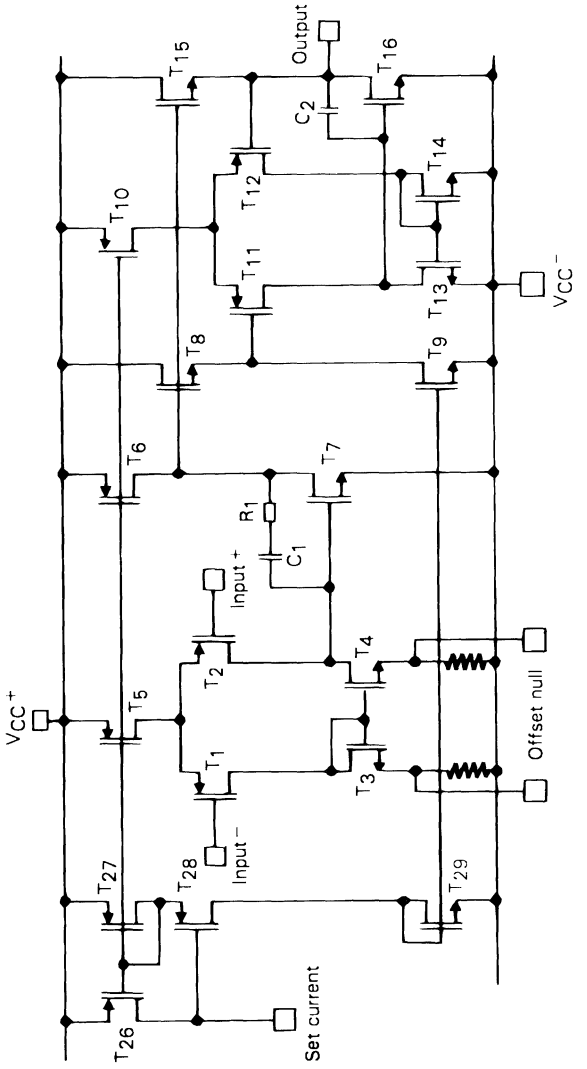
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	12	V
V_{id}	Differential Input Voltage (note 2)	± 12	V
V_i	Input Voltage (note 3)	- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature TS271C TS271I TS271M	 0 to 70 - 40 to 105 - 55 to 125	°C
T_{stg}	Storage Temperature	- 65 to 150	°C
I_{set}	I_{set} Range	1 to 200	µA

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

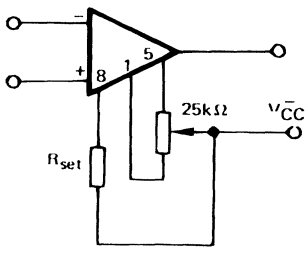
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common-mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM



E88TS271-03

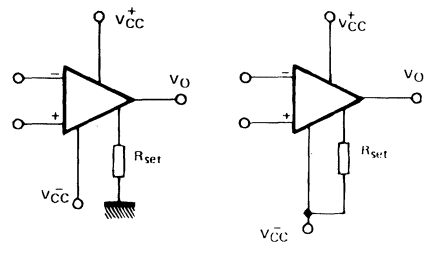
OFFSET VOLTAGE NULL CIRCUIT



E88TS271-04

OFFSET COMPENSATION GUARANTEED FOR TS271BCX (I_{set} > 25 µA), TS271ACX (I_{set} > 90 µA)

RESISTOR BIASING

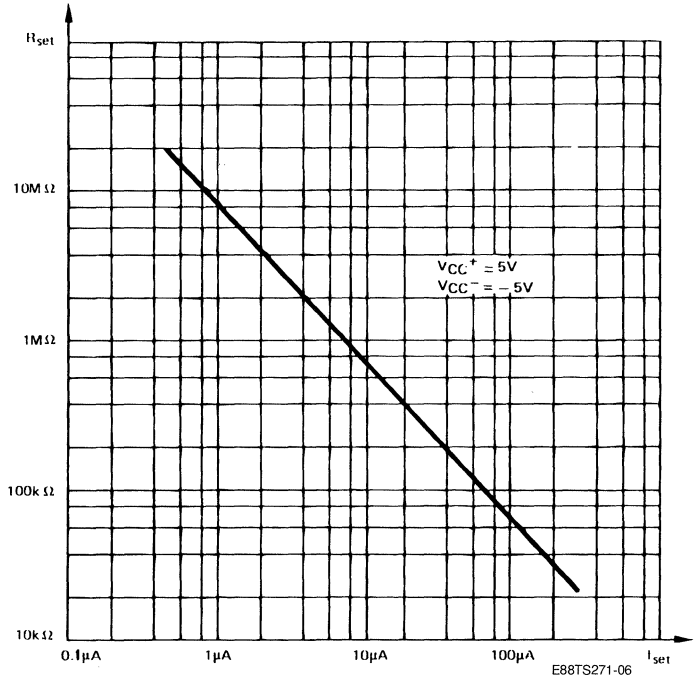


E88TS271-05

R_{set} CONNECTED TO GROUND

R_{set} CONNECTED TO V_{CC}^- (R_{set} VALUE : SEE FIG. 1)

Figure 1 : R_{set} Connected to V_{CC}^-.



E88TS271-06

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 1.5 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 mΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 1 mΩ $T_{min} < T < T_{max}$	30 20	100		30 20	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V, V_i = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 10 pF C_L = 100 pF		 35 10			 35 10		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 40 70			 40 70		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S = 10 Ω		70			70		nV/√Hz

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 25 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100KΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 100 KΩ $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_V = 40 dB R_L = 100 KΩ C_L = 100 pF fin = 100 KHz		0.7			0.7		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V, V_i = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 KΩ C_L = 10 pF C_L = 100 pF		 50 30			 50 30		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 30 50			 30 50		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S =10 Ω		38			38		nV/√Hz

Note : 1. Low output voltage is less than 50mV.

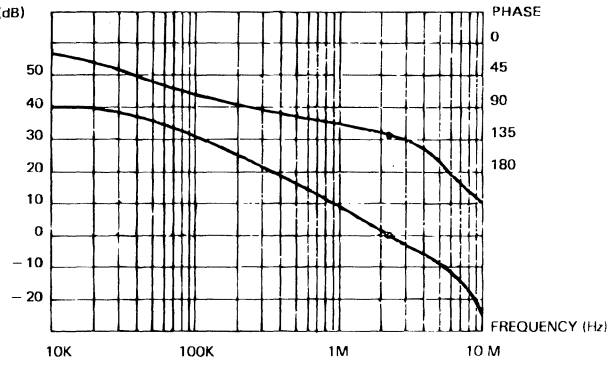
ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 130 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 KΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 KΩ C_L = 100 pF fin = 200 KHz		2.3			2.3		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V, V_i = 5 V $T_{min} < T < T_{max}$		800	1300 1400		800	1300 1500	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		4.5			4.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 KΩ C_L = 10 pF C_L = 100 pF		 56 56			 56 56		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 30 30			 30 30		%
V_n	Input Equivalent Noise Voltage F =1 KHz R_S = 10 Ω		30			30		nV/√Hz

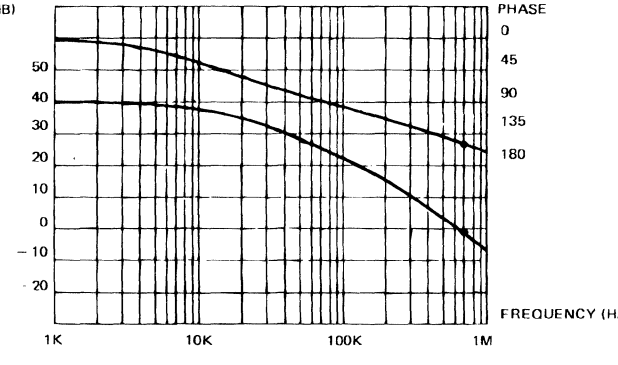
Note : 1. Low output voltage is less than 50mV.

I_{set} = 130 µA



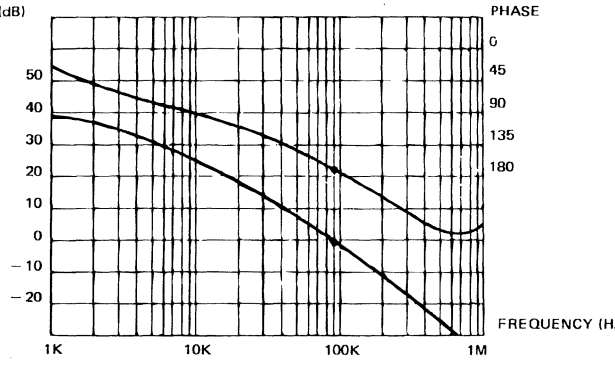
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} ± 5 V, R_L = 10 KΩ, C_L = 100 pF, T_{amb} = 25 °C E88TS271-07

I_{set} = 25 µA



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} ± 5 V, R_L = 100 KΩ, C_L = 100 pF, T_{amb} = 25 °C E88TS271-08

I_{set} = 1.5 µA



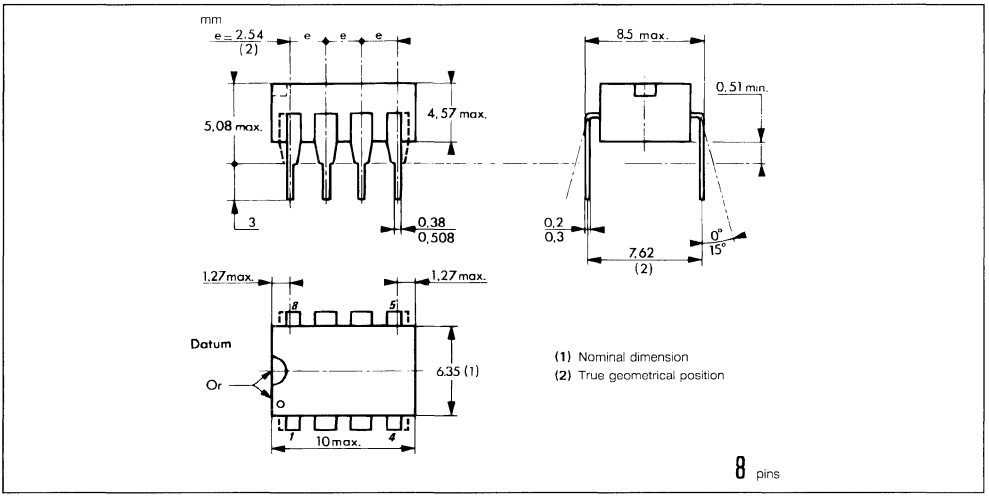
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} ± 5 V, R_L = 1 MΩ, C_L = 100 pF, T_{amb} = 25°C E88TS271-09

ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS271C	0 to + 70	•	•	
TS271AC	0 to + 70	•	•	
TS271BC	0 to + 70	•	•	
TS271I	- 40 to + 105	•	•	
TS271M	- 55 to + 125			•
TS271AI	- 40 to + 105	•	•	
TS271AM	- 55 to + 125			•
TS271BI	- 40 to + 105	•	•	
TS271BM	- 55 to + 125			•
Examples : TS271 ACN, TS271 CD				

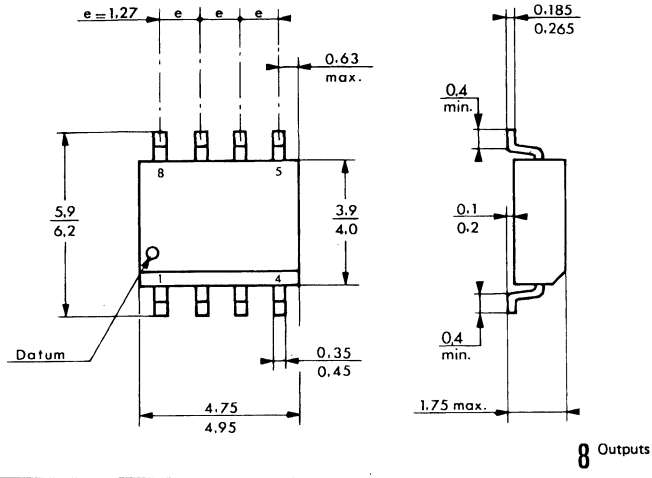
PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

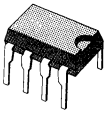
8 PINS – PLASTIC MICROPACKAGE SO



TS272
TS27M2/TS27L2

CMOS DUAL OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITANCE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS272
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD DUAL OPERATIONAL AMPLIFIERS (TL082 - LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



N
DIP8
(Plastic package)

J
CERDIP8
(Cerdip package)

D
SO8
(Plastic micropackage)

(Order Codes at the end of the Data sheet)

DESCRIPTION

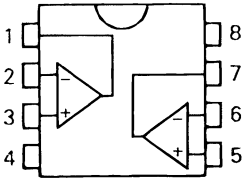
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- I_{CC} = **10 µA** per amplifier : TS27L2 (Low bias versions)
- I_{CC} = **150 µA** per amplifier : TS27M2 (Medium bias versions)
- I_{CC} = **1 mA** per amplifier : TS272 (High bias versions)

The input impedance is similar to the J-FET input impedance. Very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

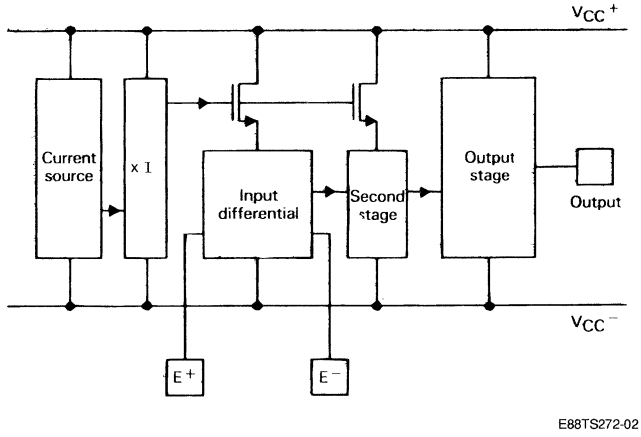
PIN CONNECTIONS (top view)



E88TS272-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

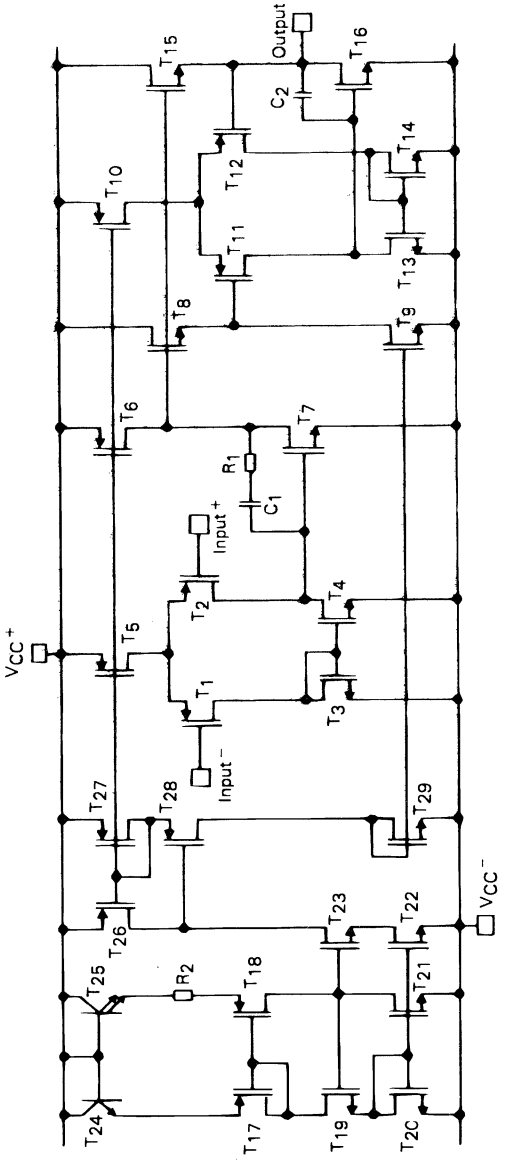
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		− 0.3 to 12	V
T_{oper}	Operating Free-air Temperature			°C
		TS272C	0 to 70	
		TS272I	− 40 to 105	
		TS272M	− 55 to 125	
		TS27M2C	0 to 70	
		TS27M2I	− 40 to 105	
		TS27M2M	− 55 to 125	
		TS27L2C	0 to 70	
		TS27L2I	− 40 to 105	
		TS27L2M	− 55 to 125	
T_{stg}	Storage Temperature		− 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal respect to the terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (For 1/2 TS27×2)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS272

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} —

Symbol	Parameter	TS272C			TS272I/TS272M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS272 $T_{min} < T < T_{max}$ TS272A $T_{min} < T < T_{max}$ TS272B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	 8.2 8.1	 8.4		 8.2 8	 8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	 10 7	 15		 10 6	 15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 kΩ C_L = 100 pF Fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_O = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_O = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = – 10 mV, V_O = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} –

Symbol	Parameter	TS27M2C			TS27M2I/TS27M2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M2 $T_{min.} < T < T_{max}$ TS27M2A $T_{min} < T < T_{max}$ TS27M2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	 8.7 8.6	 8.9		 8.7 8.5	 8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	 30 20	 50		 30 10	 50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF Fin = 100 KHz		1			1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

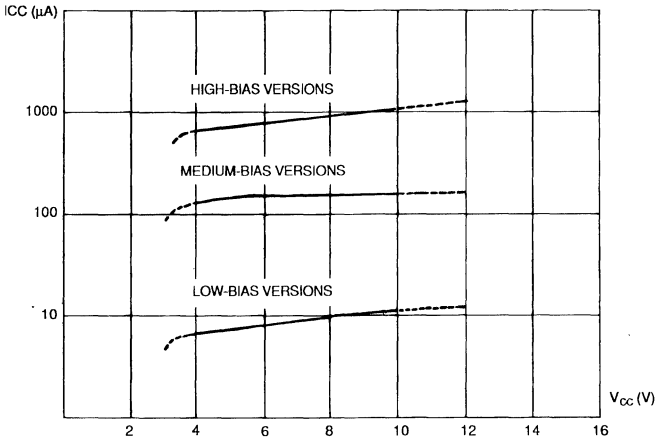
Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27L2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} —

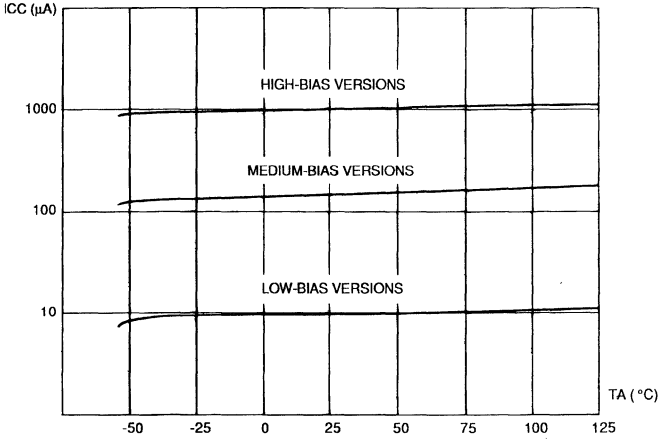
Symbol	Parameter	TS27L2C			TS27L2I/TS27L2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L2 $T_{min} < T < T_{max}$ TS27L2A $T_{min} < T < T_{max}$ TS27L2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	 8.8 8.7	 9		 8.8 8.6	 9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 1 MΩ V_i = 5 V $T_{min} < T < T_{max}$	 60 45	 100		 60 40	 100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF Fin = 100 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25\ °C$, NO LOAD

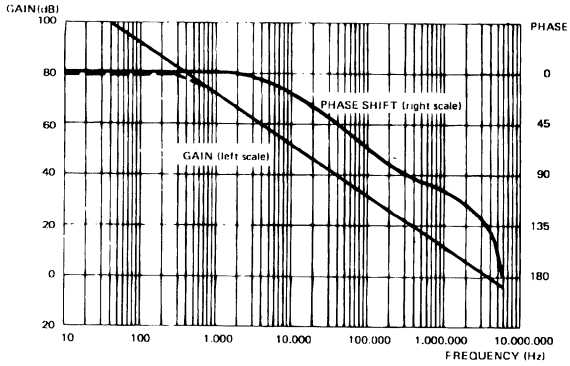
E88TS272-04



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10\ V$, $V_{IC} = 5\ V$, $V_O = 5\ V$, NO LOAD

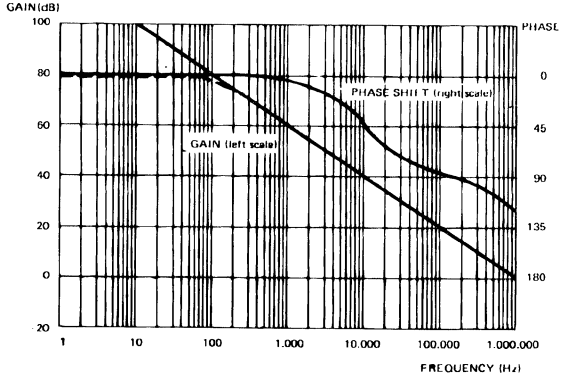
E88TS272-05

TS272



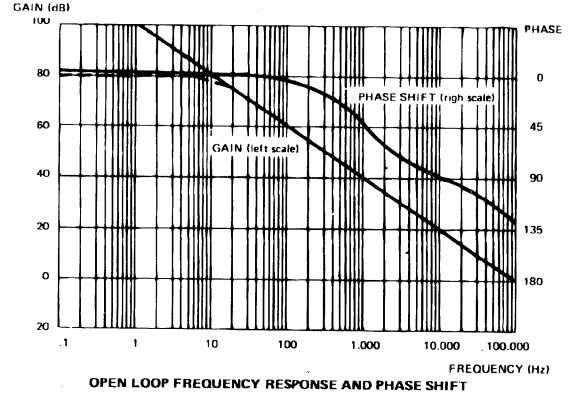
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-06

TS27M2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-07

TS27L2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-08

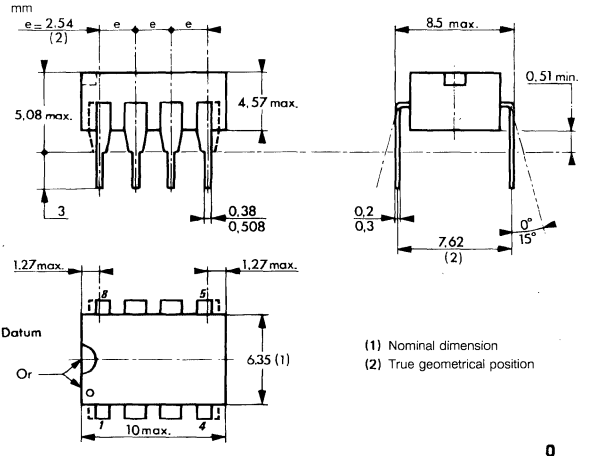
ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS272C	0 to 70	•	•	
TS272AC	0 to 70	•	•	
TS272BC	0 to 70	•	•	
TS272I	– 40 to 105	•	•	
TS272M	– 55 to 125			•
TS27M2C	0 to 70	•	•	
TS27M2AC	0 to 70	•	•	
TS27M2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27M2M	– 55 to 125			•
TS27L2C	0 to 70	•	•	
TS27L2AC	0 to 70	•	•	
TS27L2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27L2M	– 55 to 125			•
TS272AI	– 40 to 105	•	•	
TS272BI	– 40 to 105	•	•	
TS272AM	– 55 to 125			•
TS272BM	– 55 to 125			•
TS27M2AI	– 40 to 105	•	•	
TS27M2BI	– 40 to 105	•	•	
TS27L2AI	– 40 to 105	•	•	
TS27L2BI	– 40 to 105	•	•	
TS27M2AM	– 55 to 125			•
TS27M2BM	– 55 to 125			•
TS27L2AM	– 55 to 125			•
TS27L2BM	– 55 to 125			•

Examples : TS27L2ACN, TS272CD

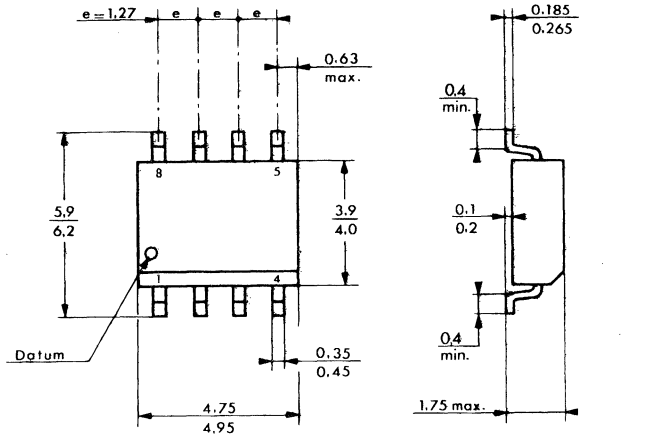
PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

8 PINS - PLASTIC MICROPACKAGE SO

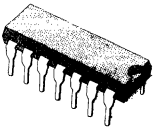


SGS-THOMSON MICROELECTRONICS

TS274
TS27M4/TS27L4

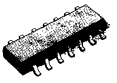
CMOS QUAD OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS274
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD QUAD OPERATIONAL AMPLIFIERS (TL084-LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



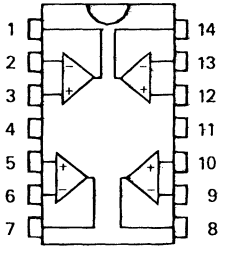
N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)
(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS274-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^+
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^-
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

DESCRIPTION

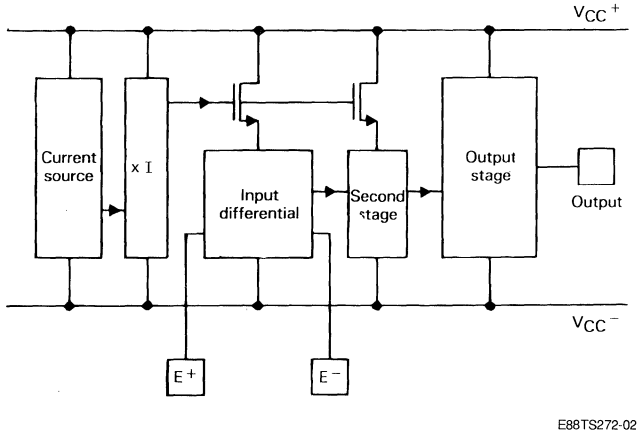
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- I_{CC} = **10 µA** per amplifier : TS27L4 (Low bias versions)
- I_{CC} = **150 µA** per amplifier : TS27M4 (Medium bias versions)
- I_{CC} = **1 mA** per amplifier : TS274 (High bias versions)

The input impedance is similar to the J-FET input impedance : very high input inpedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

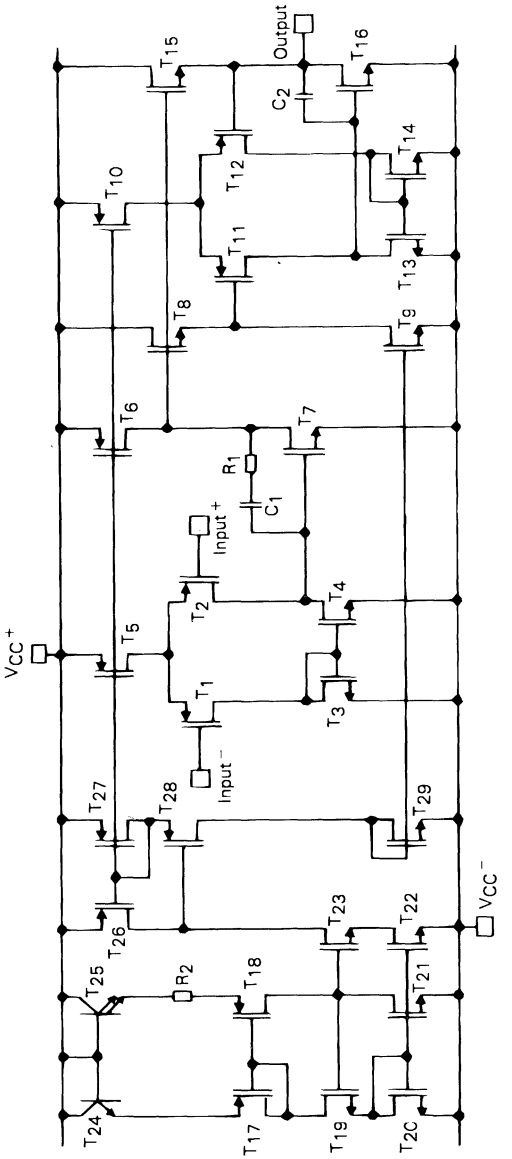
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature			°C
		TS274C	0 to 70	
		TS274I	- 40 to 105	
		TS274M	- 55 to 125	
		TS27M4C	0 to 70	
		TS27M4I	- 40 to 105	
		TS27M4M	- 55 to 125	
		TS27L4C	0 to 70	
		TS27L4I	- 40 to 105	
		TS27L4M	- 55 to 125	
T_{stg}	Storage Temperature		- 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (for 1/4 TS27 x 4)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS274

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS274C			TS274I/TS274M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS274 $T_{min} < T < T_{max}$ TS274A $T_{min} < T < T_{max}$ TS274B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 10 kΩ V_i = 5 V $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_V = 40 dB R_L = 10 kΩ C_L = 100 pF fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS27M4C			TS27M4I/TS27M4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M4 $T_{min} < T < T_{max}$ TS27M4A $T_{min} < T < T_{max}$ TS27M4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	 8.7 8.6	 8.9		 8.7 8.5	 8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	 30 20	 50		 30 10	 50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF f_{in} = 100 KHz		1			1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
$S_{V\,O}$	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{01}/V_{02}	Cross Talk Attenuation		120			120		dB

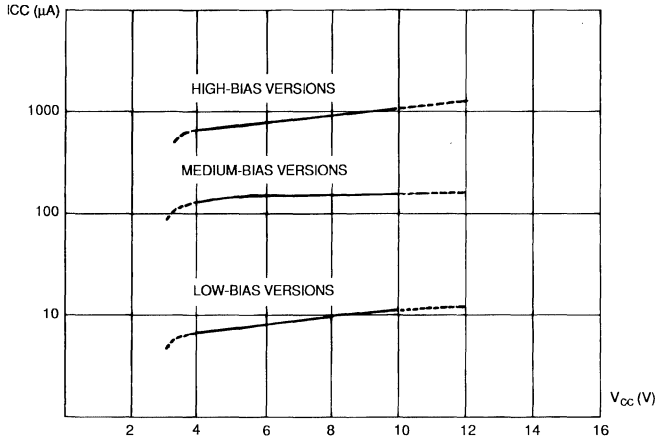
Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27L4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

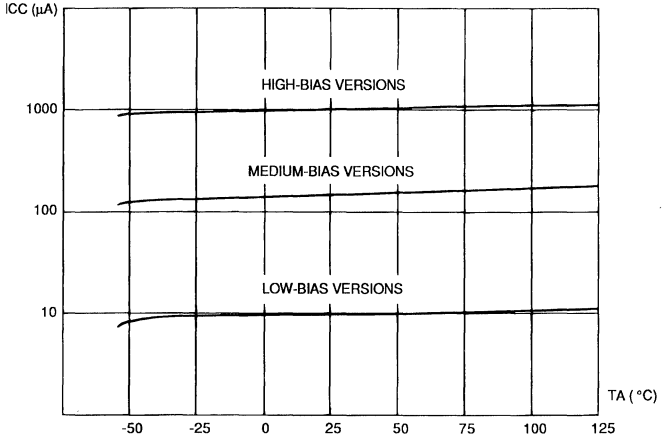
Symbol	Parameter	TS27L4C			TS27L4I/TS27L4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L4 $T_{min} < T < T_{max}$ TS27L4A $T_{min} < T < T_{max}$ TS27L4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	60 45	100		60 40	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
V_{O1} / V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25$ °C, NO LOAD

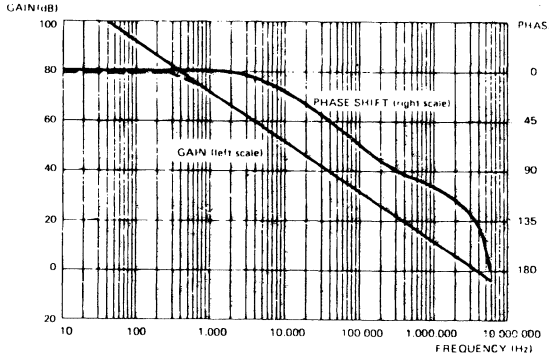
E88TS274-02



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10$ V, $V_{IC} = 5$ V, $V_O = 5$ V, NO LOAD

E88TS274-03

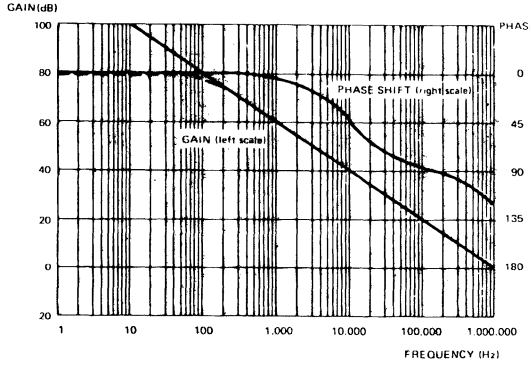
TS274



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-04

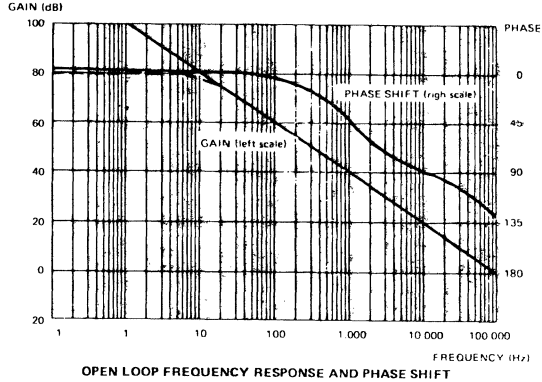
TS27M4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25 °C

E88TS274-05

TS27L4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-06

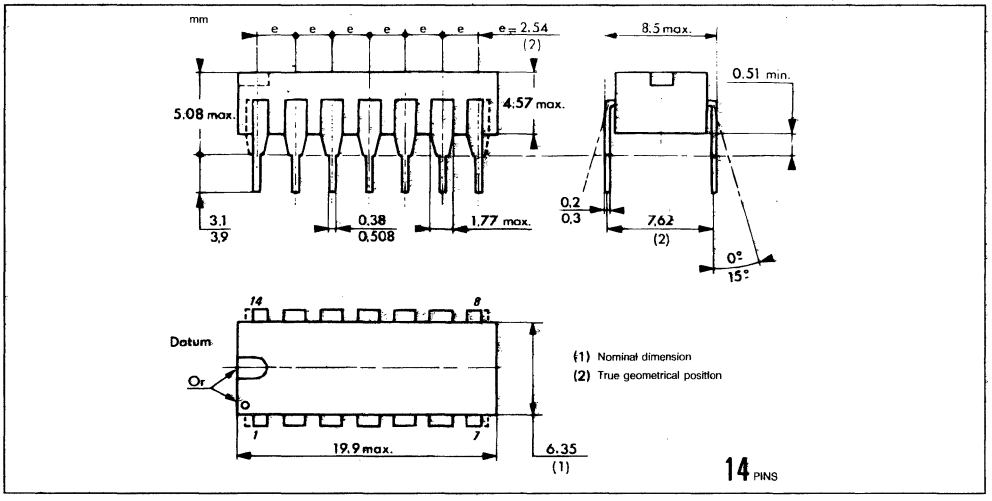
ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS274C	0 to + 70	•	•	
TS274AC	0 to + 70	•	•	
TS274BC	0 to + 70	•	•	
TS274I	- 40 to + 105	•	•	
TS274M	- 55 to + 125			•
TS27M4C	0 to + 70	•	•	
TS27M4AC	0 to + 70	•	•	
TS27M4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27M4M	- 55 to + 125			•
TS27L4C	0 to + 70	•	•	
TS27L4AC	0 to + 70	•	•	
TS27L4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27L4M	- 55 to + 125			•
TS27M4AI	- 40 to + 105	•	•	
TS27M4AM	- 55 to + 125			•
TS27M4BI	- 40 to + 105	•	•	
TS27M4BM	- 55 to + 125			•
TS27L4AI	- 40 to + 105	•	•	
TS27L4AM	- 55 to + 125			•
TS27L4BI	- 40 to + 105	•	•	
TS27L4BM	- 55 to ± 125			•

Examples : TS27L4ACN, TS274CD

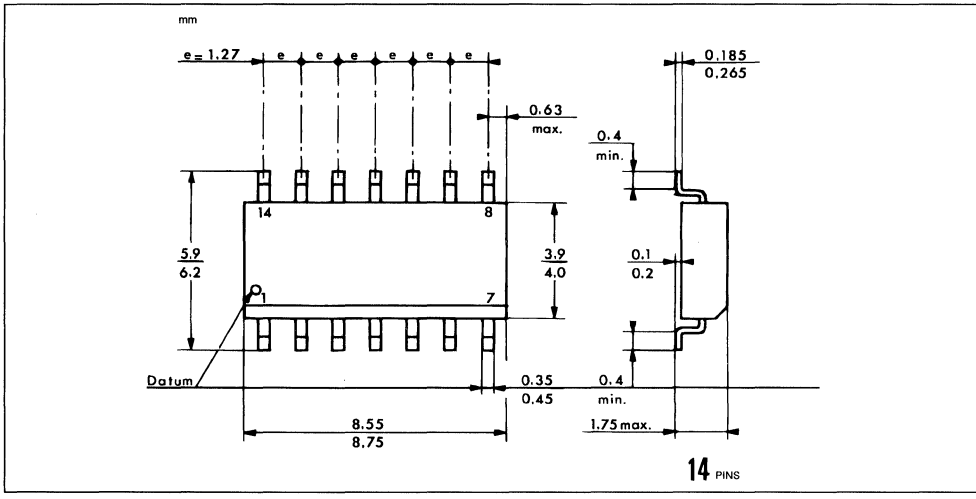
PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



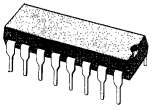
PACKAGE MECHANICAL DATA (continued)

14 PINS - PLASTIC MICROPACKAGE SO



CONTROL CIRCUIT FOR FAST SWITCHING TRANSISTORS

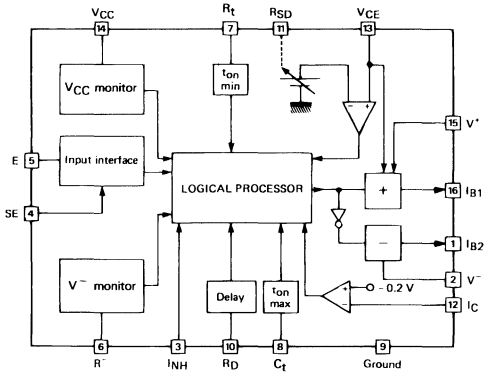
- DIRECT DRIVE OF THE SWITCHING TRANSISTOR
- SELF REGULATED POSITIVE BASE CURRENT (1 A max)
- NEGATIVE BASE CURRENT ENSURING FAST TURN-OFF (3 A max)
- THE OUTPUT CURRENT CAN BE INCREASED BY MEANS OF ONE (or more) EXTERNAL TRANSISTOR(S)
- MINIMUM CONDUCTING TIME (or no conduction) TO ALLOW THE DISCHARGE OF A RDC NETWORK
- PROTECTION AGAINST SATURATION FAILURE OF THE POWER TRANSISTOR DURING CONDUCTING PERIOD, WITH ADJUSTABLE DETECTION THRESHOLD
- INSTANTANEOUS-COLLECTOR CURRENT LIMITATION
- POSITIVE SUPPLY (V_{CC}) MONITORING
- NEGATIVE SUPPLY MONITORING WITH ADJUSTABLE THRESHOLD
- ON-CHIP THERMAL PROTECTION
- PROGRAMMABLE MAXIMUM ON TIME
- TTL AND CMOS COMPATIBLE INPUT
- CAN BE DRIVEN WITH ALTERNATE PULSES
- ADJUSTABLE DELAY BETWEEN THE RISING EDGE OF THE INPUT SIGNAL AND THE BEGINNING OF THE POSITIVE BASE DRIVE



DIP-16/2

ORDER CODE : UAA4002DP

Figure 1: Block Diagram



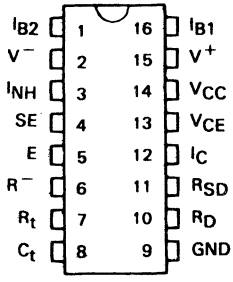
I_{B2}	:	Output sink current
V^-	:	Negative power supply (power stage)
I_{NH}	:	Inhibition input
S_E	:	Input selection
E	:	Input
R^-	:	Negative supply monitoring time resistor
R_t	:	Minimum conducting time resistor
C_t	:	Minimum conducting time capacitor
I_{B1}	:	Output source current
V^+	:	Positive power supply (power stage)
V_{CC}	:	Positive supply voltage
V_{CE}	:	$V_{CE(sat)}$ sensing
I_C	:	Collector current monitoring input
R_{SD}	:	$V_{CE(sat)}$ threshold voltage monitoring
R_d	:	Delay time resistor
G_{ND}	:	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+ 15	V
V^+	Positive Supply Voltage (power stage)	+ 15	V
V^-	Negative Supply Voltage (power stage)	− 10	V
$V^+ - V^-$	Voltage between Pins 15 and 2	+ 18	V
I_{B1}	Positive Output Current	+ 1.5	A
I_{B2}	Negative Output Current	− 3.5	A
I_C	Current into Input I_C (internal protection diodes)	± 5	mA
–	Minimum Value of Resistors R_t and R_D	5	kΩ
–	Voltage between Input and V^-	+ 18	V
T_j	Junction Temperature Range	− 40 to + 150	°C
T_{stg}	Storage Temperature Range	− 40 to + 150	°C

Note : 1. Pin 2 (V-) should not be left open.

PIN CONNECTION (top view)



I_{B2} : Output sink current
V^- : Negative power supply (power stage)
I_{NH} : Inhibition input
S_E : Input selection
E : Input
R^- : Negative supply monitoring time resistor
R_t : Minimum conducting time resistor
C_t : Minimum conducting time capacitor
I_{B1} : Output source current
V^+ : Positive power supply (power stage)
V_{CC} : Positive supply voltage
V_{CE} : $V_{CE(sat)}$ sensing
I_C : Collector current monitoring input
R_{SD} : $V_{CE(sat)}$ threshold voltage monitoring
R_d : Delay time resistor
G_{ND} : Ground

THERMAL DATA

$R_{th(j-a)}$	Maximum Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C, V_{CC} = + 10 V, V^- = – 5 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	7	–	14	V
–	Positive Supply Voltage Monitoring Threshold	–	7	–	V
I_{CC}	Supply Current	–	12	–	mA
V^+	Positive Supply Voltage (power stage)	4	–	14	V
V^-	Negative Supply Voltage (power stage)	– 1	–	– 9	V
V_I	Threshold of Input I_C	0.160	0.2	0.240	V
I_I	Current into Input I_C	–	5	20	µA
R_t	Value of Resistor R_t (R_t between pin 7 and ground)	10	47	200	kΩ
R_D	Value of Resistor R_D (R_D between pin 10 and ground)	20	–	200	kΩ
I_{B1}	Positive Output Current ($V_{(15)} - V_{(16)}$ = + 2 V)	0.5	–	–	A
$I_{B1(peak)}$	Positive Output Current (peak value)	1	–	–	A
I_{B2}	Negative Output Current ($V_{(1)} - V_{(2)}$ = + 4 V)	3	–	–	A
V_{SD}	Comparator V_{CE} Threshold Voltage	1	–	5.6	V
–	High Level on Input E ($V_{(5)} - V^-$ < + 18 V)	2	–	V_{CC}	V
–	Low Level on Input E (input SE not connected)	V^-	–	0.8	V
–	Low Level on Input E ($\|V^-\|$ > 2.5 V, input SE tied to ground)	V^-	–	– 2	V
–	Current into Input E ($V_{(5)}$ = 0 V) Input SE Left Open Input SE Grounded	 – –	 10 0.2	 50 0.3	 µA mA
–	Low Level on Input I_{NH}	0	–	0.8	V
–	High Level on Input I_{NH}	2	–	V_{CC}	V
$t_{on(min)}$	Time Constant t_{on} min (R_t between pin 7 and ground)	0.06 R_t (kΩ)			µs
t_d	Delay between Input Pulse and Rise of Output Current (R_D between pin 10 and ground)	0.05 R_D (kΩ)			µs
–	Propagation between Input Pulse and Rise of Output Current	0.3			µs
V_{SD}	Desaturation Threshold (R_{SD} between pin 11 and ground)	$10 \times \frac{R_{SD}}{R_t}$			V
R^-	V^- min Detection Resistor Value (R^- between pin 6 and V^-)	$\frac{R_t}{2}\left(1 + \frac{V^- min}{5}\right)$			Ω
$t_{on(max)}$	Time Constant t_{on} max (C_t between pin 8 and ground)	$2R_tC_t$			s
–	Thermal Shut Down	150			°C

APPLICATION INFORMATION

The coexistence of a power circuit handling high voltages and currents, and a control circuit carrying low amplitude signals, does not represent any special difficulty provided that a few simple rules are observed.

Positive and negative supply voltages of the integrated circuit must be carefully filtered by means of capacitors located very close to the device.

The device itself must by situated close to the power transistor, using short connections.

The control circuit ground (pin 9) and the power circuit ground (emitter of the power transistor) must be linked by a single connection, as short as possible and of adequate cross-section.

A ground plane on the printed circuit board may be favourable in noisy environments. With regards to upper switches of a bridge configuration, the auxiliary supplies of the integrated circuit must have a low parasitic capacitor with respect to the ground potentiel. In the same way, the isolated components

driving the UAA4002 (optocoupler or pulse transformer) must have also a low parasitic capacitor in order to reduce dv/t phenomenons and to avoid risks of reswitching or conduction cut-off.

If a free-wheel diode is connected in parallel with the power transistor (witch is generally the case in bridge systems), a diode (1N4148) must be connected between pin 13 and ground (cathode on pin 13 and anode on ground) in order to limit the negative voltage applied to this pin during the conduction of the free-wheel diode.

CIRCUIT DESCRIPTION (see block diagram figure 1)

INPUT INTERFACE E AND SE INPUT

It translates the input signal into the logic levels required by the internal processor.

It also includes a RS flip-flop for the pulse mode operation.

FAULT DETECTORS

- Power transistor collector current limiting (I_C input)

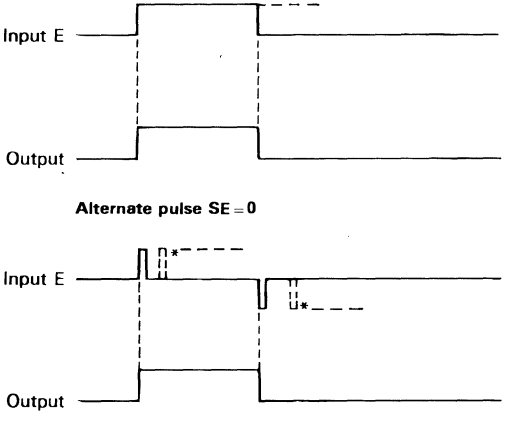
The collector current of the power transistor is measured by means of a shunt connected in the negative return of the power supply. As a result the current rather than the emitter current, since the base current of the switching does not flow through the shunt.

A voltage below - 0.2 V on input I_C causes comparator to change state. This information is transmitted to the logic unit, which blocks the output pulses from the circuit until the next positive transition of the input signal.

If the voltage across the measuring shunt exceeds 0.2 V for the required limiting current value, a voltage divider bridge may be used (see application note NA031A).

If input I_C not used, it must be connected directly to ground.

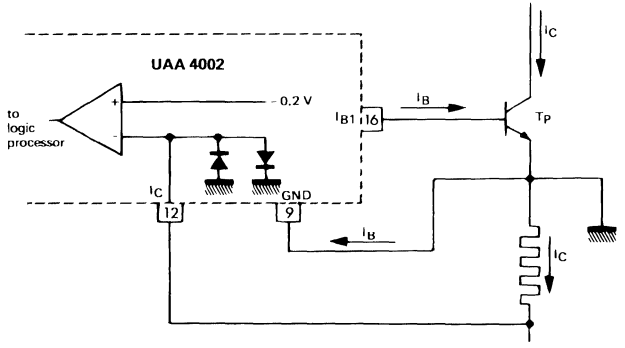
Figure 2 : Level Mode SE = 1.



* These parasitic pulses are not taken into account.

Note : Pulse duration > 100ns.

Figure 3 : Switching Transistor Collector Current Measurement.



- Protection against desaturation of the power transistor.

A comparator monitors continuously during the conduction that the collector voltage on the switching transistor remains lower than the preset value.

The preset value V_{RSD} (see figure 4) is given by :

$$R_{SD} = 5\ V \times 2\frac{R_{SD}}{Rt}$$

Current I set by external resistor R_t is :

$$I\ (mA) = \frac{5\ (V)}{R_t\ (k)}$$

Without resistor R_{SD}, the threshold is set internally at + 5.6 V.

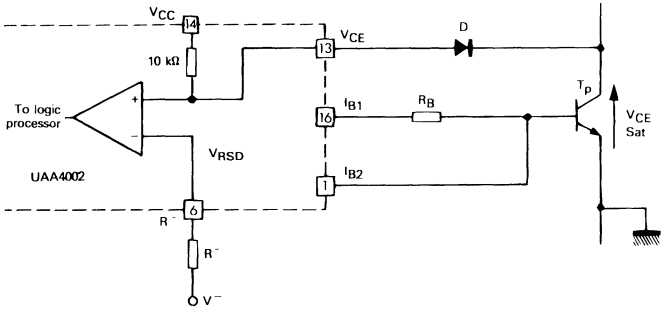
In case of overstep, the information is transmitted to the logic unit, which turns the output off until the next positive edge of the input signal.

To enable the switching transistor collector emitter voltage to fall when conduction begins, the protection function against desaturation is disabled during t_{on} min (see application note NA031A).

This protection is disabled by connecting pin R_{SD} directly to V.

(FOR THRESHOLD EXCEEDING 5.5 V SEE NA031EA).

Figure 4 : V_{CEsat} Voltage Monitoring.



Diode D must be a high-speed diode able to withstand the transistor collector-emitter volatge when the transistor is cut-off.

SUPPLY DEFECT

- Negative supply (R input, see figure 4).

It is possible to disable the output pulses if the negative supply voltage V is insufficient to guarantee the switching of the power transistor (optional).

(FOR USING WITHOUT NEGATIVE POWER SUPPLY SEE NA031A)

For this a resistor R is tied between pin 6 and the negative supply.

A current 2 I flows into it, and the threshold of the detector is + 5 V on pin 6.

Thus giving the relationship :

$$\frac{5 + V_{-\,min}}{R_-} = 2 \times \frac{5}{R_t} \qquad R_- = \frac{R_t}{2}\left(1 + \frac{V_{-\,min}}{5}\right)$$

This function can be disabled ty tying pin 6 to ground.

- Positive supply (V_{CC} input)

An internal comparator ensures that there is no output voltage if positive supply V_{CC} is less than + 7 V. This threshold is not adjustable.

- Inhibition (I_{NH} input)

The action of the inhibition input is shown in the diagram below.

This input is CMOS and TTL compatible. If not used, it must be connected directly to ground.

- Thermal protection

The UAA4002 is protected against excessive overheating by a thermal cut-out which automatically cuts off the output pulses if the chip temperature exceeds + 150 °C. The interruption is stored for a complete conduction period, but the output pulses reappear as soon as the chip temperature falls below the limiting temperature value.

TIME CONSTANTS

- Minimum conducting time (R_t input)

To enable the capacitor of the switching aid network associated with power transistor to discharge completely, the logic processor ensures that the integrated circuit output pulse has a minimum duration t_{on} min. To be effective, this must be at least four times the time constant of the RDC network.

The value of t_{on} min is programmed by a resistor R_t

Typically t_{on} min (s) = 0.06 x R_t (k)

The usable range of values for t_{on} min is between 1 and 12 s.

Resistor R_t has a key role in the operation of the UAA4002 integrated circuit. It sets the value of a bias current internal to the circuit :

$$I\,(mA) = \frac{5}{R_t\,(k)}$$

t_{on} min embodies a priority function : no other security function can stop the conduction during t_{on} min.

The t_{on} min function cannot be disabled.

- Maximum conducting time (R_t and C_t inputs)

At the start of each conduction period the capacitor C_t is loaded by a constant current 1/2, where I is the current through resistor R_t ($I = 5/R_t$). When the voltage across C_t reaches + 5 V the conduction is stopped. The value of t_{on} max is thus given by the equation :

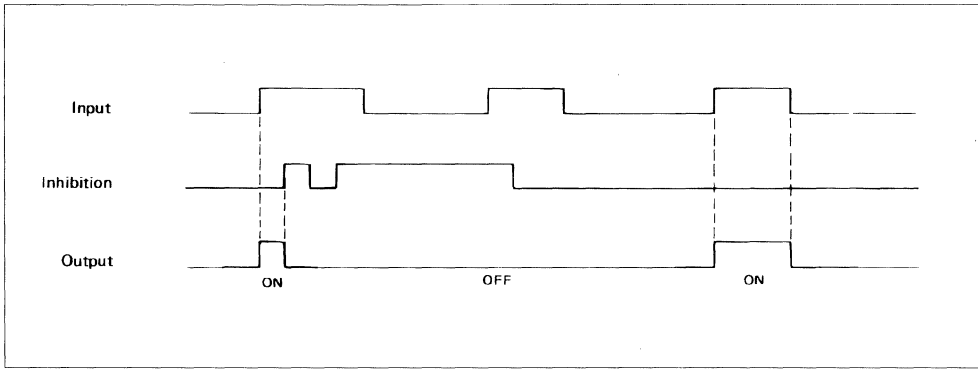
t_{on} max (s) = 2 x R_t (k) x C_t (nF)

If the t_{on} max function is not to be used, it is only necessary to replace capacitor C_t with a short-circuit.

- Time delay function

A constant time delay may be implemented between the rising edge of the control pulse and the begin-

Figure 5.

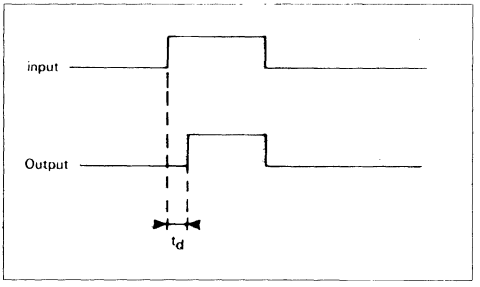


ning of the conduction pulse at the circuit output = (1 to 20 µs by using resistor R_D, t_d (µs) = 0.05 R_D (kΩ).

LOGIC PROCESSOR

A logic unit processes the information coming from the fault detectors, and ensures that the output signal fulfils two conditions :

Figure 6.



- No double pulsing within a period : the occurence of a defect is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum output pulse width is set at a given value t_{on} min.

OUTPUT STAGE : V^+, V–, I_{B1}, I_{B2}, INPUTS

- Introduction

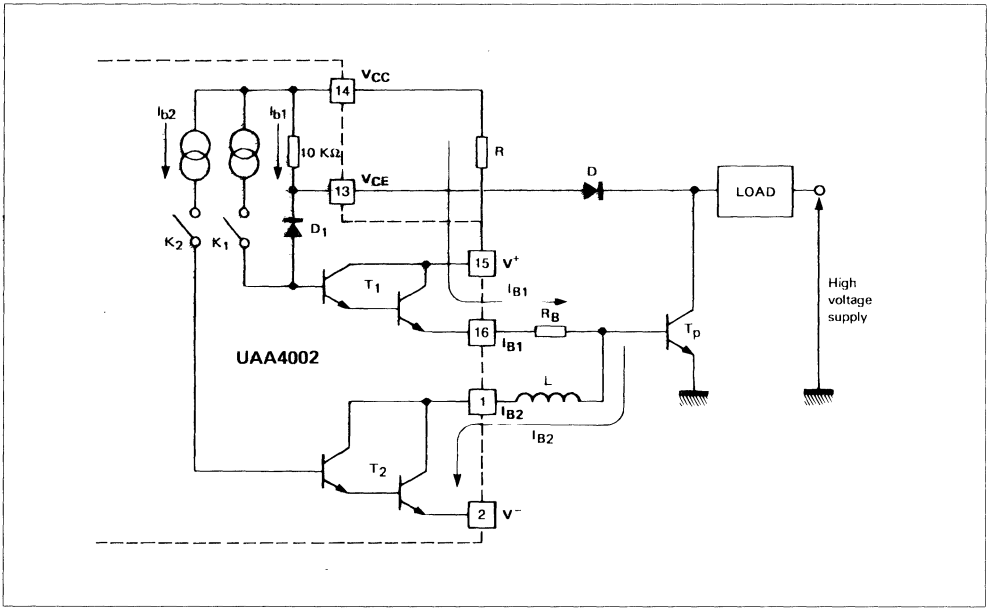
The highly sophisticated output stage of the UAA4002 offers high performance is terms of switching transistor control.

Its principal features are as follows :

- the switching transistor is direct driven
- the transistor remains in a quasi-saturated state, whence reduced storage time
- control power is limited to the strict minimum
- it is easy to use

This stage is in fact in two parts, a positive driver stage which turns on the transistor and a negative driver stage which turns off the transistor.

Figure 7.



■ Power transistor conduction

The maximum value of the positive base current is determined by the limitation resistor R (I_{B1} 1 A). A regulation loop is used to keep T_p in a quasi-saturation mode : the more T_p becomes saturated, the more diode D will shunt an important part of the drive current I_{B1}, through diode D_1. R_B is a low value resistor (about 1) which helps to stabilize the regulation loop.

Voltage V_{CE} across transistor Q is :

V_{CE} (V) = V_{BE} (V) + R_B () I_{B1} (A)

If the required drive current is greater than 0.5 A, one external NPN transistor may be added.

In this case :

V_{CE} (V) = 2 V_{BE} (V) + R_B ().I_B (A)

■ Turn-off switching of power transistors

The closing of contact K_2 (figure 10) causes Darlington T_2 to conduct. The negative supply voltage is applied to the base of transistor T_P and a high negative base current I_{B2} flows, permitting the rapid evacuation of charges stored in the base-emitter junction of transistor T_P.

A low-value inductor L may be required between the base of transistor T_P and the I_{B2} output of the UAA4002, so as to limit the gradient dI_{B2}/dt (see "The Power Transistor in its Environment" published by the Discrete Semiconductors Division of Thomson-CSF). In many cases, this inductor is not required.

The Darlington T_2 can carry a maximum current of 3 A. The corresponding saturation voltage is typically 3 V. Like the positive stage, this stage is designed for easy augmentation of the available output current by the addition of one or more external transistors.

■ Typical inductive load waveforms

When conduction begins, the base current assumes a high value briefly and then reverts to zero. This base current spike permits rapid switching on of the power transistor. The base current value is then that required for quasi-saturation of the transistor. The base current curve is generally curved upwardy, due to the decreased gain of the power transistor with increased collector current.

Figure 8.

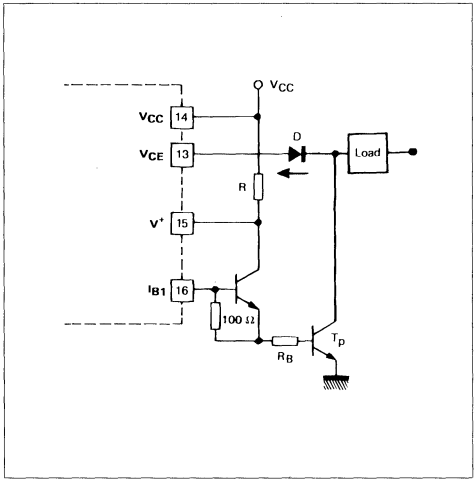
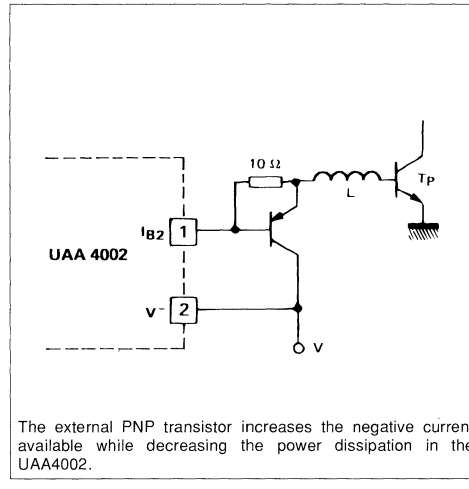
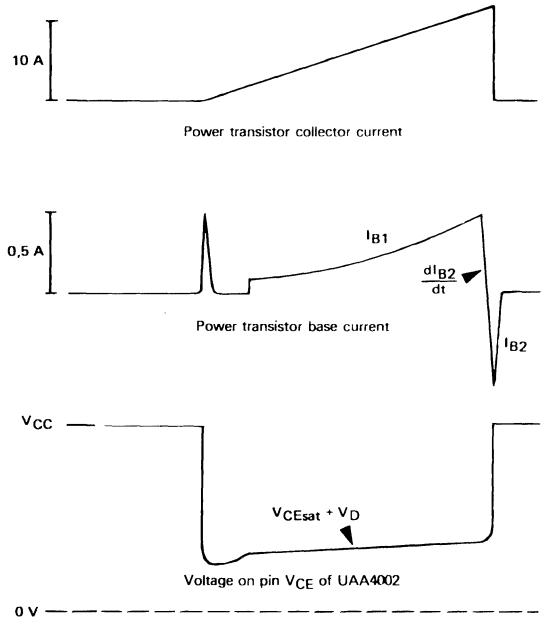


Figure 9.



The external PNP transistor increases the negative current available while decreasing the power dissipation in the UAA4002.

Figure 10.



CONTROL OF MOS POWER TRANSISTORS

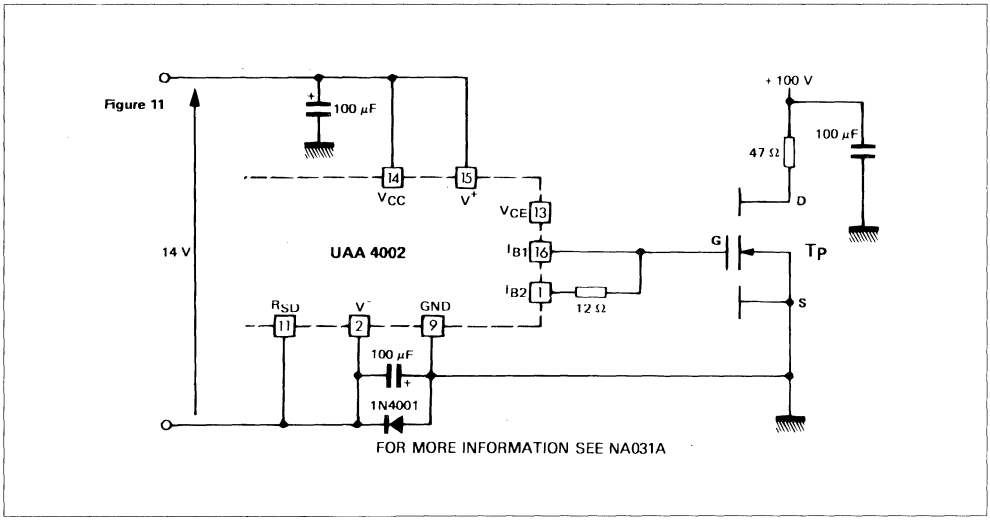
Ideally,MOS power transistors should be voltage-controlled. In practice, in order to benefit from the high speed typical of this type of transistor it is necessary to charge and discharge the spurious input capacitance at high speed, so that high currents flow. By virtue of the high current capability of its output stages, the UAA4002 is particularly suitable for controlling MOS power transistors.

The output of the positive stage is connected directly to the gate of the MOS transistor, to switch it into conduction very fast. The negative stage controls the turning off of the MOS transistor, by discharging the gate capacitance of the transistor. There is no need for a high negative supply voltage, and the arrangement described in the previous section is therefore used.

In this circuit the UAA4002 is used in a completely conventional manner, in "level" control mode.

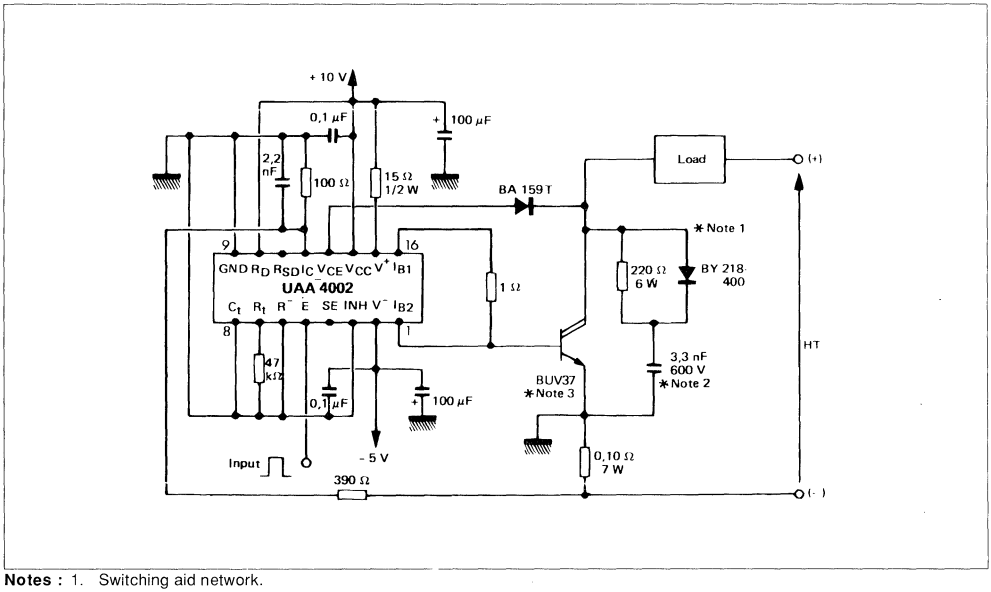
The time constant t_{on} min is set at 2.8 s, which is four times the time constant of the snubber network associated with the BUV37 transistor. The positive output stage of the UAA4002 is connected to the V_{CC} rail through a 15 resistor. The maximum base current is approximately 0.45 A. The collector current is measured using a 0.10 shunt, and is limited to 10 A. The BUV37 Darlington for which the specified value of I_{Csat} is 12 A, is thus operated with a considerable safety margin.

Figure 11.



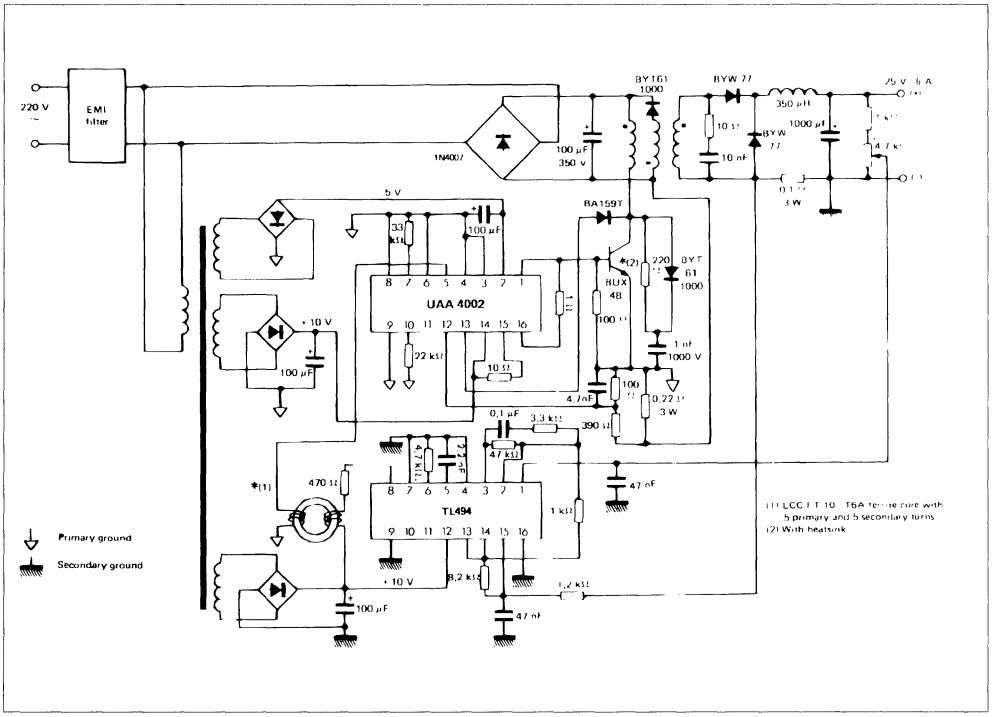
TYPICAL APPLICATIONS

Figure 12 : 8 A, 400 V switch.



Notes : 1. Switching aid network.
2. Polypropylene capacitor.
3. With heatsink, $R_{HT} < 3.5$ °/W.

Figure 13 : 150 W Forward Type Power Supply.



Performance

- Output voltage stability :
  For an input voltage varying from 190 to 245 V, the maximum relative variation in the output voltage is 0.7 % at nominal operating conditions.
  (V_{OUT} = 25 V, I_{OUT} = 6 A).
  For a variation in the load from 0 to 100 % the relative variation in the output voltage is 1.3 %.
  For a variation in the load from 10 to 100 % (I_{OUT} = 0.6 to 6 A), the relative variation in the output voltage is 0.4 %.
- Efficiency 80 % under nominal operating conditions.
- Behaviour on overload :
  The power supply is fully protected against overloads and short-circuits, the output current being limited to 7 A.

Figure 14 : Capacitor Type Half Bridge Symmetrical Converter.

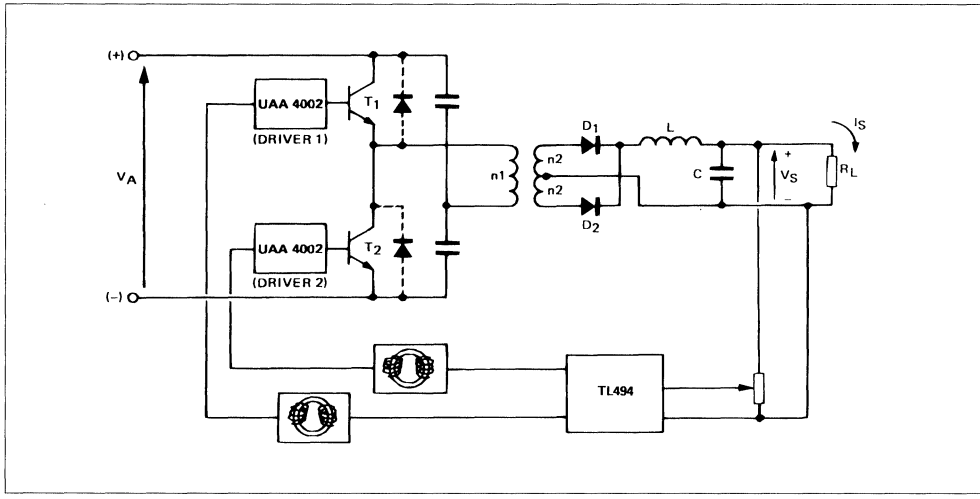
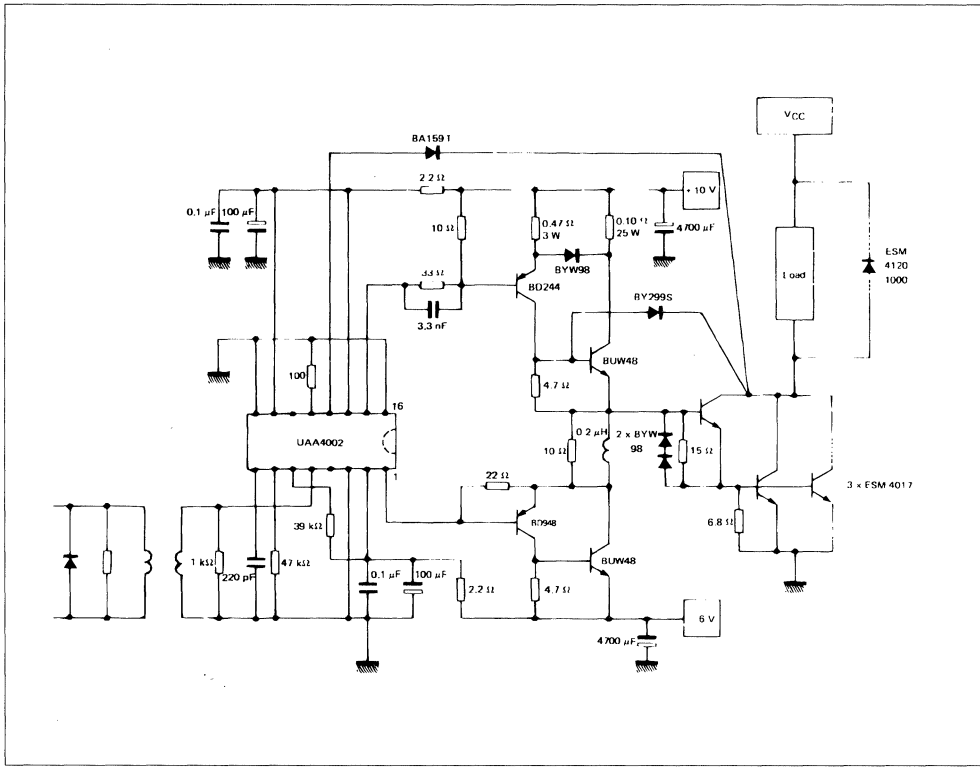


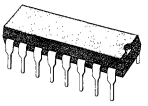
Figure 15 : 200 A, 700 V Switch.



SWITCH MODE REGULATOR FOR DC MOTORS

- SOFT START
- DIRECT DRIVE OF THE SWITCHING TRANSISTOR (or darlington)
- SELF-REGULATED POSITIVE BASE CURRENT (peak 1.5 A)
- NEGATIVE BASE CURRENT PROVIDING FAST TURN-OFF, AND ALLOWING THE BEST USE OF THE SAFE OPERATING AREA (peak 1.5 A)
- SWITCHING TRANSISTOR PROTECTED AGAINST SATURATION FAILURE
- INSTANTANEOUS LIMITATION OF THE COLLECTOR CURRENT
- POWER SUPPLY MONITORING
- ON-CHIP THERMAL PROTECTION
- INCLUDES 2 µs MINIMUM CONDUCTING TIME (or no conduction) FOR USE OF A SNUBBER CIRCUIT

DIP-16/2
(Plastic)

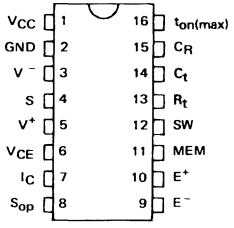


ORDER CODE : UAA4003DP

DESCRIPTION

The UAA4003 is a regulation and control device for the drive of DC motors.
Includes oscillator, PWM and error amplifier.

PIN CONNECTION



1 - Supply voltage
2 - Ground
3 - Negative supply (power stage)
4 - Power stage output
5 - Positive supply (power stage)
6 - $V_{CE(sat)}$ sensing
7 - Collector current monitoring
8 - Op. amp. output
9 - Op. amp. inverting input
10 - Op. amp. non-inverting input
11 - Memory input
12 - SW
13 - R_t resistor (oscillator)
14 - C_t capacitor (oscillator)
15 - Locked rotor
16 - Limit access

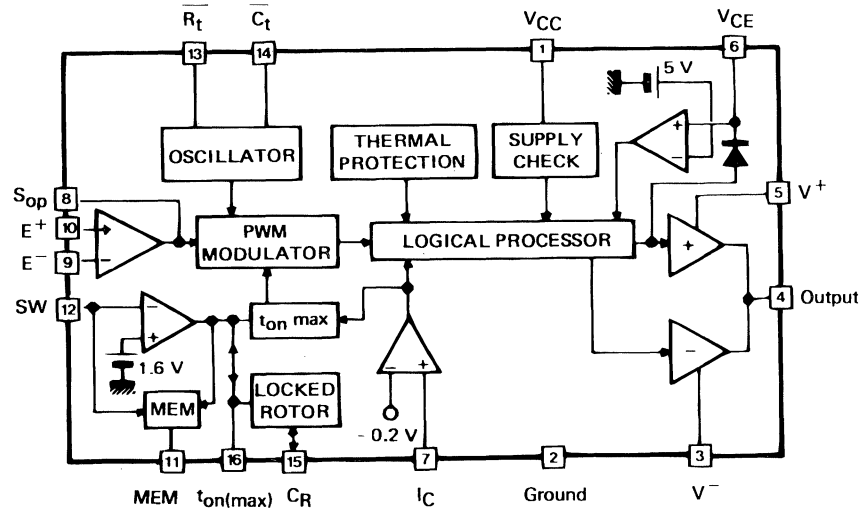
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	+ 15	V
	Supply Voltages (power stage)		V
V^+	Positive	+ 15	
V^-	Negative	− 9	
$V^+ - V^-$	Voltage between Pin 5 and Pin 3	+ 18	V
I_O	Output Current	± 2	A
−	MEM Output Current	10	mA
−	Current into Input I_C (internal protection diodes)	± 5	mA
R_t	Minimum Value of Resistance R_t	10	kΩ
T_j	Junction Temperature Range	− 40 to + 150	°C
T_{stg}	Storage Temperature Range	− 40 to + 150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Maximum Junction–ambient Thermal Resistance	80	°C/W

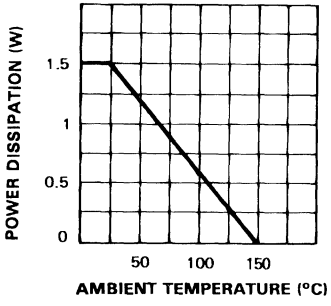
BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, V_{CC} = + 10 V, V^- = – 5 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	6.2	–	14	V
I_{CC}	Supply Current (V_{CC} = + 10 V)	–	10	–	mA
V^+	Positive Supply Voltage (power stage)	4	–	14	V
V^-	Negative Supply Voltage (power stage)	0	–	– 8	V
$V_{I(th)}$	Threshold of Input I_C	– 0.260	– 0.2	– 0.140	V
–	I_C Input Current ($V_{(7)}$ = 0 V)	–	5	20	µA
A_V	Op. Amp. Open Loop Gain	60	–	–	dB
–	Op. Amp. Input Current	–	–	1	µA
–	Op. Amp. Offset Voltage	–	5	–	mV
–	Op. Amp. Common-mode Voltage	0	–	V_{CC} – 3	V
f_{osc}	Oscillator Frequency	–	$\frac{2}{R_t.C_t}$	50	kHz
R_t	Value of Resistance R_t	10	50	500	kΩ
–	Dead Time	–	5	–	µs
I_O	Output Current ($V_{(5)} - V_{(4)}$ = + 3 V)	± 1.5	–	–	A
–	Input Current into Pin 12 (SW) ($V_{(12)}$ = 0 V)	–	25	50	µA
–	MEM Output Current (open collector) ($V_{(11)}$ = + 0.3 V)	1.2	–	–	mA
–	"Locked Rotor" Time Constant (V_{CC} = + 10 V)	–	0.3	–	s/µF
–	V_{CE} Comparator Threshold Voltage	–	5	–	V
$t_{on(min)}$	Time Constant $t_{on(min)}$	–	2	–	µs

MAXIMUM POWER DISSIPATION



CIRCUIT DESCRIPTION

OSCILLATOR

It is a sawtooth generator whose fall time is much inferior to its rise time. The period is $T_{osc} = 0.5\ R_t.C_t$, R_t and C_t being tied between pins 13 and 14 respectively, and ground.

The voltage swing is about $V_{CC}/2$ and the low level is + 1.5 V.

The maximum working frequency is 50 kHz.

PULSE WIDTH MODULATOR (PWM)

A signal with a variable duty cycle is generated by a comparison between pin 14 voltage (oscillator) and pin 8 voltage (output of the error amplifier).

A second comparator limits the maximum conduction ratio by a comparison between the sawtooth and pin 16 voltage ($t_{on\ (max)}$). If $V_{(16)} = 0$, there is an internal fixed dead time (≈5 µs).

CURRENT LIMITATION

A level lower than – 0.2 V on pin 7 (I_C) involves two actions.

- A direct action through a logic processor which stops the drive until the end of the period.
- An indirect action through the $t_{on\ (max)}$ function. The change of state at the output of comparator I_C is applied to pin 16 as long as the current overload persists. By inserting capacitor C_B between pin 16 and V_{CC} (about 0.1 µF), the voltage at this point rises up by a quantity ΔV proportional to the duration and the frequency of the oversteps.

This will consequently lower the maximum conduction ratio, thus decreasing the frequency of the oversteps.

At the end of an overload state, capacitor C_B slowly charges through a 20 kΩ internal impedance, in order to return progressively to normal operation.

This capacitor also achieves a soft-start during power-up.

Note : It is possible to use direct action only provided pin 16 is tied to ground.
In this case, "locked rotor" and "memory" functions cannot be used.

LOCKED ROTOR

A voltage greater than + 1.5 V at pin 16 starts up the linear charge of a capacitor C_R connected between pin 15 and ground (3 µF/ s).

If V_{16} becomes lower than + 1.5 V again before $V_{(15)}$ reaches V_{CC}, capacitor C_R is quickly discharged.

In the fault persists, $V_{(15)}$ reaches V_{CC}, and the output is definitively cut. There are two possible ways to return to normal drive :

- Tie temporarily pin 12 (SW) to ground.
- Tie temporarily pin 15 to ground to discharge C_R.

If this function is not to be used, simply tie pin 15 to ground.

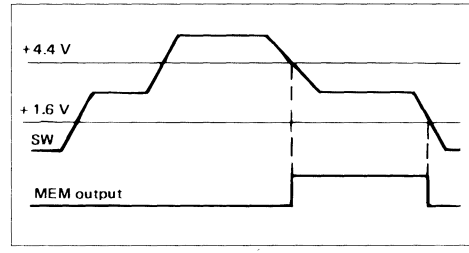
ERROR AMPLIFIER

This is an operational amplifier whose open loop gain is greater than 1000.

The input currents are lower than 1 µA, and the input offset voltage is typically 5 mV. The input common mode voltage can range from 0 V to ($V_{CC} - 3V$).

MEMORY AND INHIBITIION

Input SW (pin 12) senses a three-state logic signal. The response of the output MEM is represented here-under :



When the input signal is lower than + 1.6 V, there is an inhibition of the output drive through the $t_{on(max)}$ function. In this case the voltage on pin 16 remains close to V_{CC}.

If the input SW becomes greater than + 1.6 V, the voltage $V_{(16)}$ (between t_{on} and ground) falls. The restart is accomplished in a soft mode.

PROTECTION AGAINST DESATURATION

If, because of a too low base current or a too heavy load, voltage V_{CE} on the switching transistor rises above 4.5 V approximately, the output of comparator V_{CE} changes state, and the drive is interrupted.

POWER SUPPLY MONITORING

The drive is disabled if V_{CC} is less than + 6.2 V. Pin 3 should be connected to a voltage equal to or less than + 0.5 V.

Note that under no circumstances should this pin be left open.

THERMAL PROTECTION

This protection becomes active when the junction temperature reaches + 150 °C.

LOGIC PROCESSOR

A logic unit processes the information coming from the fault detectors, and ensures that the output signal fulfils two conditions :

- No double pulsing within a period : the occurence of a fault is memorized until the end of the period.
- To allow the discharge of a snubber network, the minimum width of the output pulse is set at 2 µs by an internal monostable. If this monostable is not triggered, there will be no conduction.

OUTPUT STAGE

ON-STATE

The positive drive achieves a very efficient drive of the switching transistor.

Its features are essentially :

- Direct drive (neither inductor nor transformer)
- The transistor stays in a quasi-saturation mode, and thus has a reduced storage time.
- The drive energy is strictly limited to the required amount.
- Easy implementation.

K_1 is closed to turn the positive stage on. The maximum value of the positive base current is set by the limitation resistor R.

Diode D maintains Q in a quasi-saturation mode : the more Q is saturated, the more diode D will shunt an important part of the drive current I_{B1}, through diode D_1.

Resistor R_B has a low value (about 1 Ω), and is used to stabilize the regulation loop.

For a good efficiency of the negative drive, the value of this resistor should be as low as possible (about 1 Ω).

Integrated Darlington T_1 is able to supply a peak current of 1.5 A with a 12 V saturation voltage.

The voltage V_{CE} on transistor Q is :
$V_{CE} = V_D + R_B I_{B1}$

OFF-STATE

The turn off is accomplished in two steps :

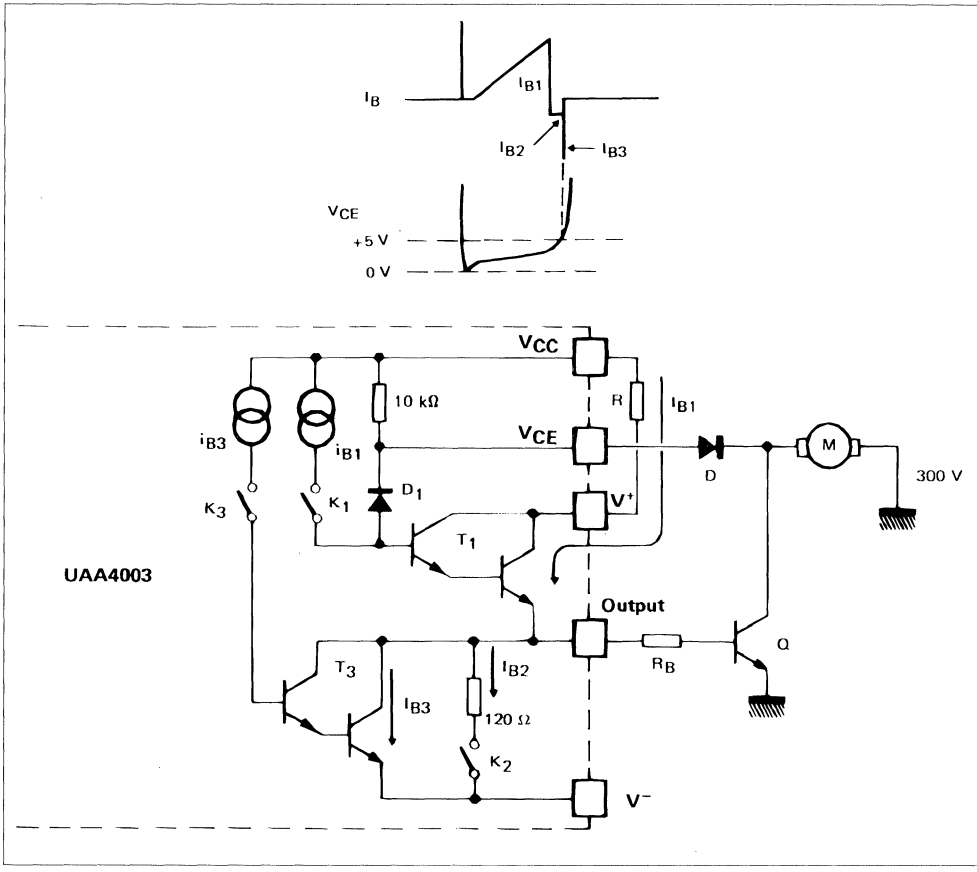
- An immediate action through K_2 which connects the base of the switching transistor to the negative supply through a 120 Ω integrated resistor (current I_{B2}).
- A delayed action through K_3 which is closed only after the desaturation of the external transistor.

This is detected by comparator V_{CE}, when collector to emitter voltage reaches 4.5 V.

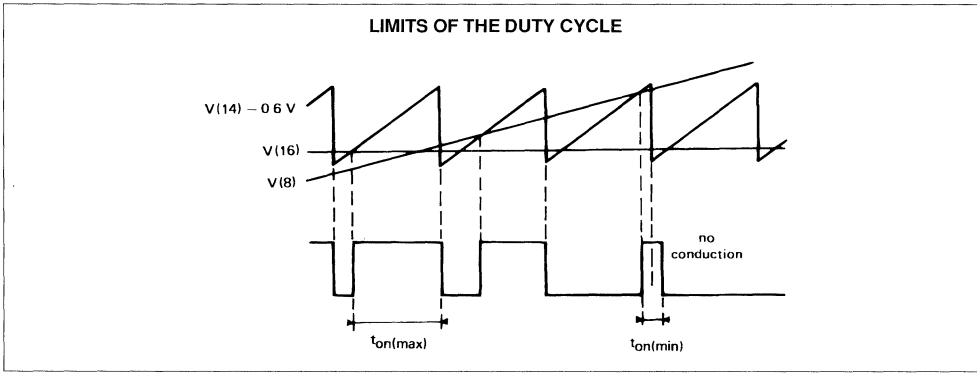
Darlington T_2 can supply 1.5 A with a 2 V saturation voltage (current I_{B3}).

NOTE : The negative drive I_{B3} for the removal of the stored charges is delayed in order to limit the slope dI_B/dt at the on-off transition. A high dI_B/dt might indeed lead to a destructive overheating of the base-collector junction (see "The power transistor in its environment" published by Thomson CSF Division Semiconducteurs Discrets).

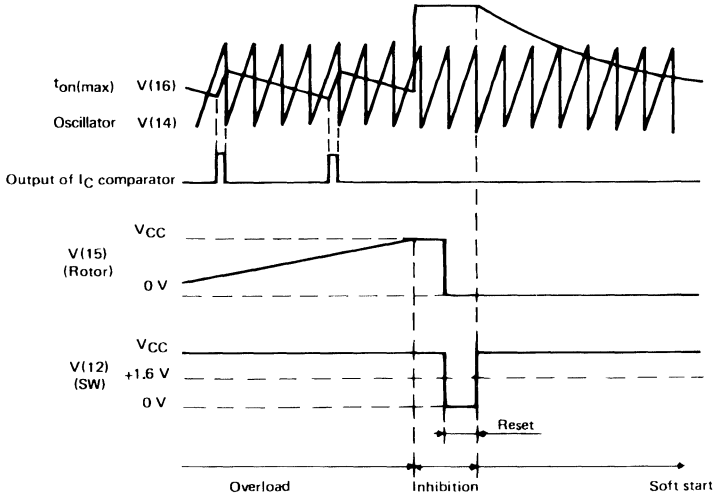
SELF REGULATED BASE CURRENT $I_B = f(V_{CE})$



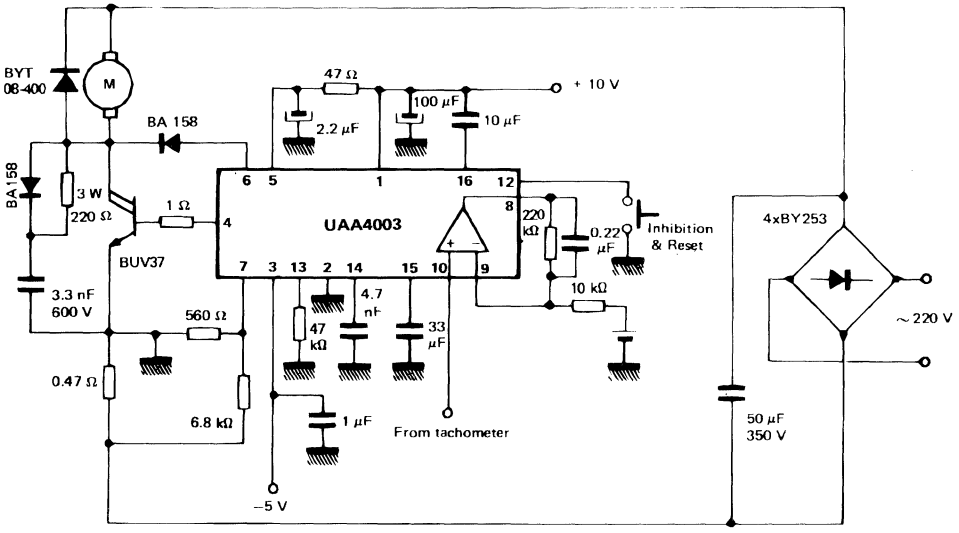
TYPICAL WAVEFORMS



"CURRENT LIMITATION" AND "LOCKED ROTOR" OPERATION



SPEED REGULATOR 1.5 kW



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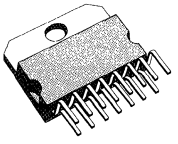
UAB4718
UAF4718

STEPPER MOTOR DRIVE CIRCUIT

- HALF AND FULL STEP MODES
- BIPOLAR DRIVE OF STEPPER MOTOR FOR MAXIMUM MOTOR PERFORMANCE
- BUILT-IN PROTECTION DIODES
- WIDE RANGE OF CURRENT CONTROL : UP TO 1500 mA
- WIDE VOLTAGE RANGE : 10 TO 55 V
- DESIGNED FOR UNSTABILIZED MOTOR SUPPLY VOLTAGE
- CURRENT LEVELS CONTROLLED BY AN EXTERNAL VOLTAGE REFERENCE
- THERMAL OVERLOAD PROTECTION



MULTIWATT 15

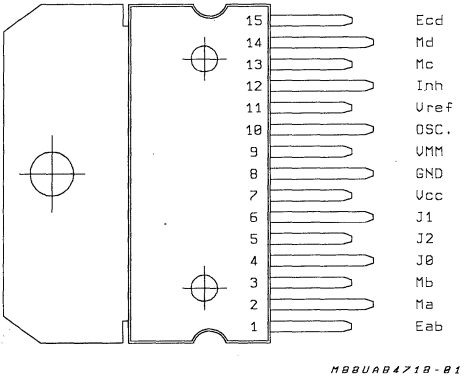
ORDER CODES :
UAB 4718SP (0 to 70 °C)
UAF 4718SP (– 40 to + 85 °C)

DESCRIPTION

The UAB/UAF 4718 provides direct interface between a logical unit and the two windings of a bipolar stepper motor.

It ensures switch-mode current regulation up to 1.5 A with 55 V supply voltage.

PIN CONNECTION



Pin Number	Name	Function	
1 2 3	Eab Ma Mb	Current Sensing Resistor Output Ma Output Mb	H-Bridge a-b
4 5 6	JO J2 J1	Decoder Inputs	Logic Inputs
7 8 9	V_{CC} GND V_{MM}	Logic Supply Voltage Ground Power Supply Voltage	Supply Voltages
10	Osc	Oscillator	
11	V_{ref}	Reference Voltage	
12	I_{nh}	Inhibition	Logic Input
13 14 15	Mc Md Ecd	Output Mc Output Md Current Sensing Resistor	H-Bridge c-d

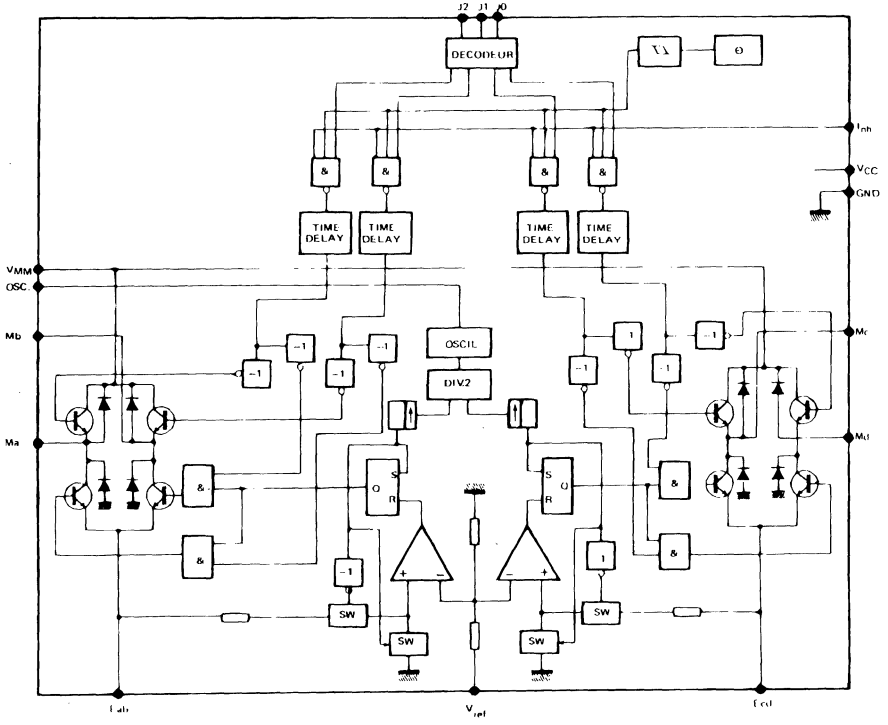
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC} V_{MM}	Supply Voltage		10 60	V
V_{ref}	Reference Voltage		15	V
V_{IN}	Logic Input Voltage		− 0.3 to V_{CC} + 0.3	V
I_O	Output Current		± 1.5	A
T_j	Maximum Juction Temperature		+ 150	°C
T_{amb}	Operating Ambient Temperature Range	UAB4718 UAF4718	0 to + 70 − 40 to + 85	°C
T_{stg}	Storage Temperature Range		− 55 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}c)}$	Maximum Junction-case Thermal Resistance	Max	3	C/W
$R_{th\ (j\text{-}a)}$	Maximum Junction-ambient Thermal Resistance	Max	40	C/W

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS V_{CC} = 5 V ± 10 %, V_{MM} = 10 V to 55 V, T_j = – 40 °C to 125 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current		15		mA
$I_{mm\ off}$	Motor Supply Current (all drivers OFF)			100	µA
I_{off}	Output Leakage Current (V_{MM} = 60 V, I_{nh} = 0)			100	µA
V_{IH}	High Level Input Voltage. Logic Input	$2V_{CC}/3$			µA
V_{IL}	Low Level Input Voltage. Logic Input			$V_{CC}/3$	µA
I_{IH}	High Level Input Current. Logic Input (V_I = 3.5 V)			1	µA
I_{IL}	Low Level Input Current. Logic Input (V_I = 0.8 V)	– 1			µA
V_C^+	Comparator's Threshold Voltage (V_{ref} = 5 V)		500		mV
I_R	Reference Input Current (V_{ref} = 5 V)		0.2		mA
V_{sat}	Source Diode Transistor Pair (T_{amb} = 25 °C) Saturation Voltage I_M = 0.7 A I_M = 1.4 A		 1.1 1.6		 V V
V_F	Diode Forward Voltage I_F = 0.7 A I_F = 1.4 A		1.25 1.65		V V
I_{sub}	Substract Leakage Current I_F =1.4 A				mA
V_{sat}	Sink Diode Transistor Pair (T_{amb} = 25 °C) Saturation Voltage I_M = 0.7 A I_M = 1.4 A		 1.08 1.5		 V V
V_F	Diode Forward Voltage I_F = 0.7 A I_F = 2.4 A		1.55 2.1		V V
P	Total Power Dissipation (T_{amb} = 25 °C) (I_M = 0.7 A ; 2 phases On ; T = 16 µS ; V_{MM} = 34 V)		3.6		W
T	Switching Period (case = 1.8 nF)		39		µs
t_d	Turn-off Delay		0.9		µs
$T_{ON\ (min)}$			25		µs
T_j	Thermal Protection Operation		170		°C
ΔT_j	Hysteresis on Thermal Protection		30		°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC} V_{MM}	Supply Voltage		4.5 10	5 –	5.5 55	V
V_{ref}	Reference Voltage		0	–	10	V
I_O	Output Current					A
	No Heatsink	One Phase On	–	–	0.7	
		Two Phase On	–	–	0.4	
	10 °C/W Heatsink	One Phase On	–	–	1.5	
		Two Phase On	–	–	0.9	

FUNCTIONAL DESCRIPTION

The circuit is organised around two H-bridges. Each one has is switched current regulation, synchronized by a common oscillator.

LOGIC

The logic inputs J2, J1 and J0 define the different sequences of a hald or full step mode excitation of the modor.

Step	J2	J1
0	0	0
1	0	1
2	1	0
3	1	1

JO = 0 : Two phases-on drive

JO = 1 : One phase-on drive

FULL-STEP ROTATION

The reference voltage used for the current regulation varies from 0 to 10 V. Owe to its high impedance input, it can be driven by any DAC. For the simplest applications, it can be connected directly to V_{CC}.

Step	J2	J1	J0
0	0	0	0
5	0	0	1
1	0	1	0
1.5	0	1	1
2	1	0	0
2.5	1	0	1
3	1	1	0
3.5	1	1	1

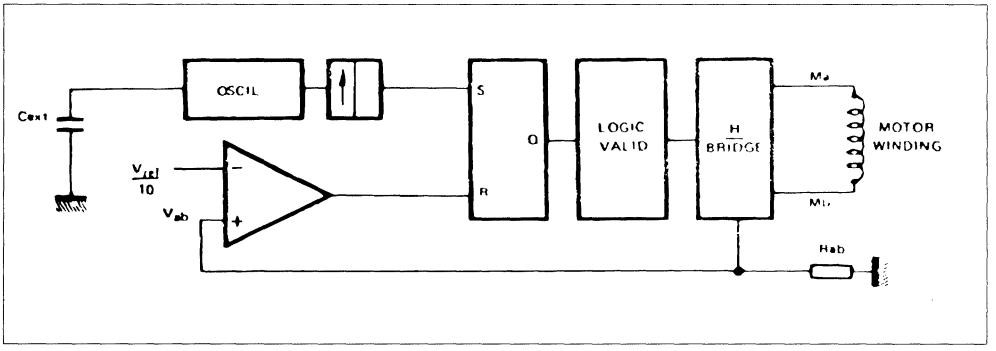
HALF-STEP ROTATION

These 3 Bits are decoded into 4 Bits (one per half H-bridge). An inhibition signal (INH) low activ and an integrated thermal protection can switch off the two output stages simultaneously.

The four logic inputs (INH, J2, J1 and J0) are CMOS compatible.

CURRENT REGULATION

Figure 1.

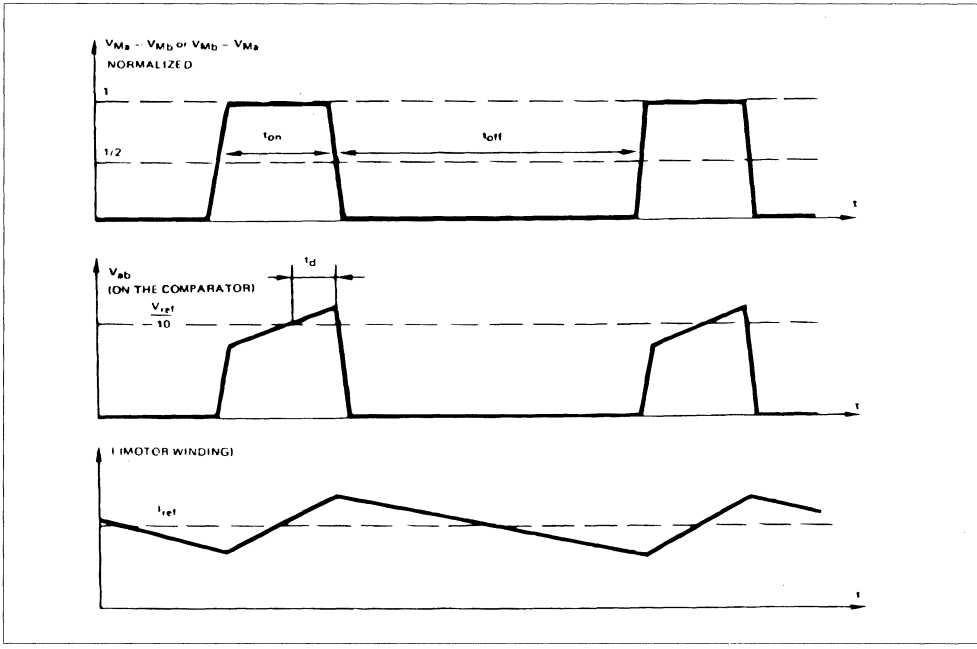


For each H-bridge, a comparator defines the current flowing in the winding by comparison between a reference voltage (defined by the external voltage Vref) and the voltage across the current sensing resistor Rab. The moto current flows through the sensing resistor Rab. When the current has increased so that the voltage across Rab becomes higher than the reference voltage, the comparator output goes high. This output, acting on the Reset input of the RS flip-flop turns of the H-bridge. Then after the next rising edge of the oscillator signal the current flows agains in the sensing resistor Rab.

$$Iout = \frac{V_{ref}}{10\ Rab}$$

WAVEFORMS

Figure 2.



t_d : delay time of comparator + logic + H-bridge,

t_{off} : delay time between ($V_{ab} < \frac{ref}{10}$) and the next rising edge of the oscillator.

$t_{on} + t_{off} = T$, T = oscillator period, $V'ref = \frac{Vref}{10}$

TIMING DIAGRAM

The oscillator frequency applied on S input is typically 60 KHz (with an external capacitor equal to 1 nF). This frequency can be adapted to the characteristics of the motor by a different value of Cext.

This switching frequency is $f\ (KHz) \# \frac{70}{C\ (nF)}$

THE COMPARATORS

The two comparators ar of PMOS type. The high input impedance of such a comparator allows the integration of an RC-filter which avoids errors on parasitic voltages.

To prevent current spikes from friggering the comparator when the sink stage is switched on, a MOS switch short-circuits the comparator input to ground during these current spikes.

OUTPUT STAGES

The two H-bridges are identical. Each output stage contains four Darlington transistor and four diodes, connected in an H-bridge. The two sinking transistors are used to switch the power supplied to the motor winding, thus driving a constant current through the winding.

It should be noted, however, that it is not permitted to short-circuit the outputs.

OPERATION OF ONE H-BRIDGE

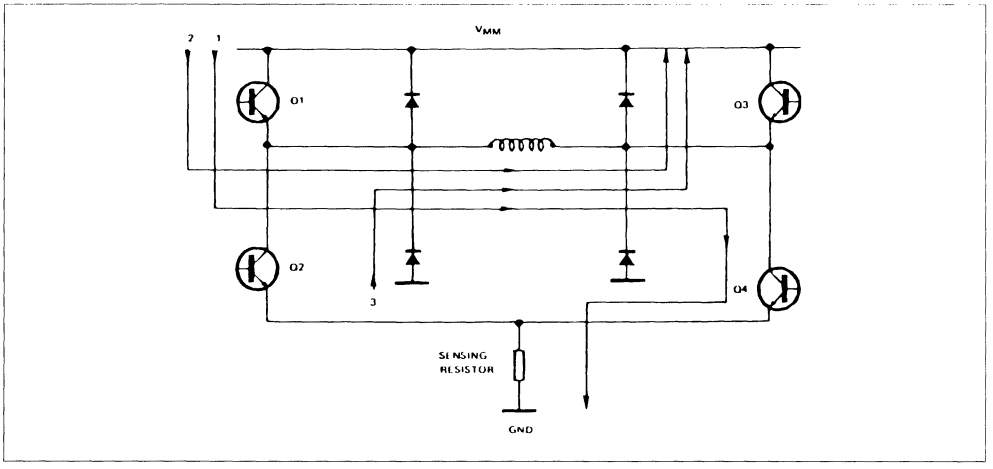
To energize the motor winding, the current flows from the power supply Vmm to the ground through the source transistor, the motor winding and the sink transistor (arrow n. 1) until the voltage drop in the current sensing resistor exceeds the reference voltage of the comparator. Then the RS flip-flop is reset and its output turns off the sink transistor. The current flows through the source transistor, the motor winding and the free wheeling diode (arrow n. 2).

Then, the rising edge of the oscillator signal sets the RS flip-flop and turns on the sink transistor.

To reverse the current in the winding, a fast current decay solution is used (arrow n. 3).

When the output stage is switched off by the inhinition input or by the thermal protection, the fast current decay solution is used too.

Figure 3



LOGIC INPUTS

There are four logic inputs

. J_2, J_1, J_0 select the current direction in the bridges

. Inh disables both bridges.

Table 1: Logic Inputs Operation.

Inh	J2	J1	J0	Bridge ab	Bridge cd
0	X	X	X	0	0
1	0	0	0	I	–I
1	0	0	1	I	0
1	0	1	0	I	I
1	0	1	1	0	I
1	1	0	0	–I	I
1	1	0	0	–I	0
1	1	1	1	–I	–I
1	1	1	0	0	–I

X : Irrelevant
I : Current from Ma to Mb
or from Mc to Md
I : Current from Mb to Ma
or from Md to Mc.

THERMAL OVERLOAD PROTECTION

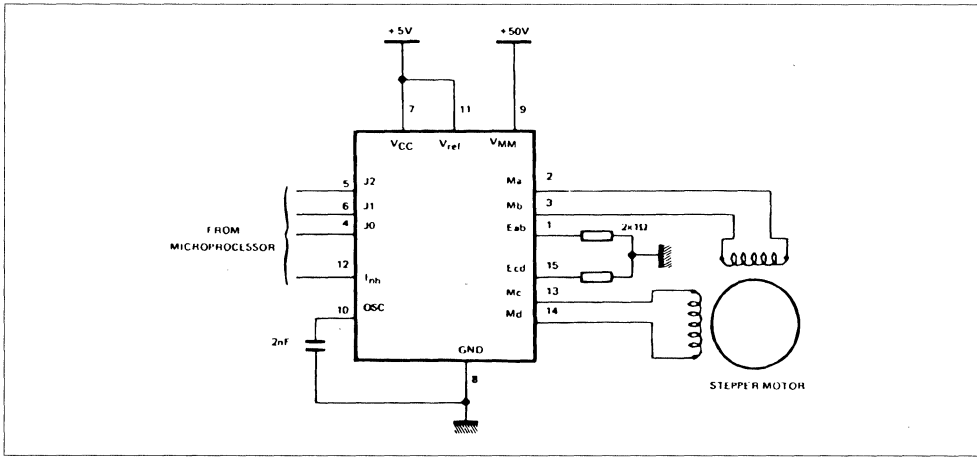
If internal dissipation becomes too high (typically Tj > 170 °C), the two output stages are disabled. After a decrease of the junction temperature (typically 30 °C), the outputs are again enabled.

TYPICAL APPLICATION

EXAMPLE OF APPLICATION

A complete application can be built with only one UA.4718 and three external components (2 resistors and 1 capacitor). On the figure below, I_O A per output, the switching frequency is 35 KHz.

Figure 4.



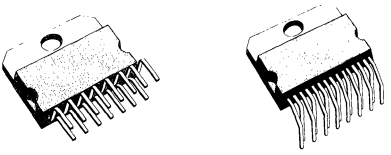
UAF1780-1781-1782

DUAL 2 A LOW DROP OUT INTELLIGENT POWER SWITCH

ADVANCE DATA

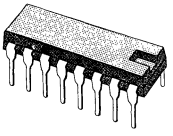
- LOW POWER DISSIPATION (LOW V_{SAT} : 0.6 V @ 2 A)
- ALL INPUTS ARE OPERATIONAL WITH CONTROL SIGNALS HIGHER THAN V_{CC}
- ALL INPUTS WITHSTAND VOLTAGES LOWER THAN GROUND
- HIGH OUTPUT CURRENTS
- PROTECTION OF OUTPUT TRANSISTORS (UP TO + 32 V)
- THE OUTPUTS CAN WITHSTAND VOLTAGES LOWER THAN GROUND
- WITHSTAND ON V_{CC} SPIKES UP TO (60 V, 10 ms)
- DIFFERENTIAL INPUTS

MULTIWATT-15



ORDER CODES :
UAF1780SP
UAF1782SP
UAF1780HSP
UAF1782HSP

DIP-16/2



ORDER CODE :
UAF1780DP-1781DP

DESCRIPTION

The UAF1780-1781-1782 are dual interface circuits delivering high output currents and capable of driving any type of load.

An on-chip dc/dc conversion unit in conjuction with a few low-cost external components (a low value inductor and a low voltage capacitor) are implemented to limit the saturation voltage thereby optimizing the efficiency.

The devices are particularly well protected against destructive overloads. Each output implements a current limit circuitry, a desaturation monitoring unit for the detection of overloads and short-circuits, and a thermal protection feature.

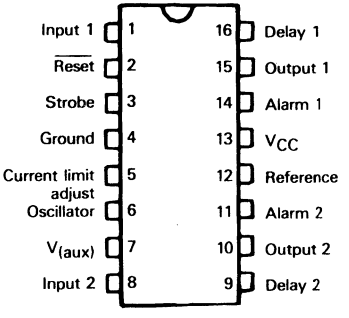
Corresponding output is turned off in case of prolonged desaturation or excessive internal dissipation. This condition is reflected by a low level on ALARM output terminal. This protection unit can be reactivated by applying a logic low signal to RESET input.

However, for inductive loads, a delay is imposed on signal applied to this RESET input so as to prevent a rapid and premature conduction of output transistors.

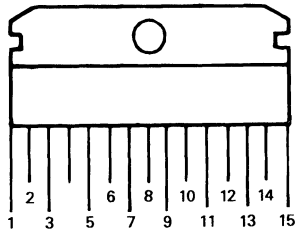
A logic high signal applied to STROBE input will disable both power outputs.

The devices operates within a supply voltage range of + 8 V to + 32 V.

PIN CONNECTIONS



PIN CONNECTIONS



1 - Oscillator
2 - $V_{(aux)}$
3 - Input 2
4 - Delay 2
5 - Alarm 2
6 - Reference
7 - Output 2
8 - Ground
9 - V_{CC}
10 - Output 1
11 - Alarm 1
12 - Delay 1
13 - Input 1
14 - Reset
15 - Strobe

ABSOLUTE MAXIMUM RATINGS

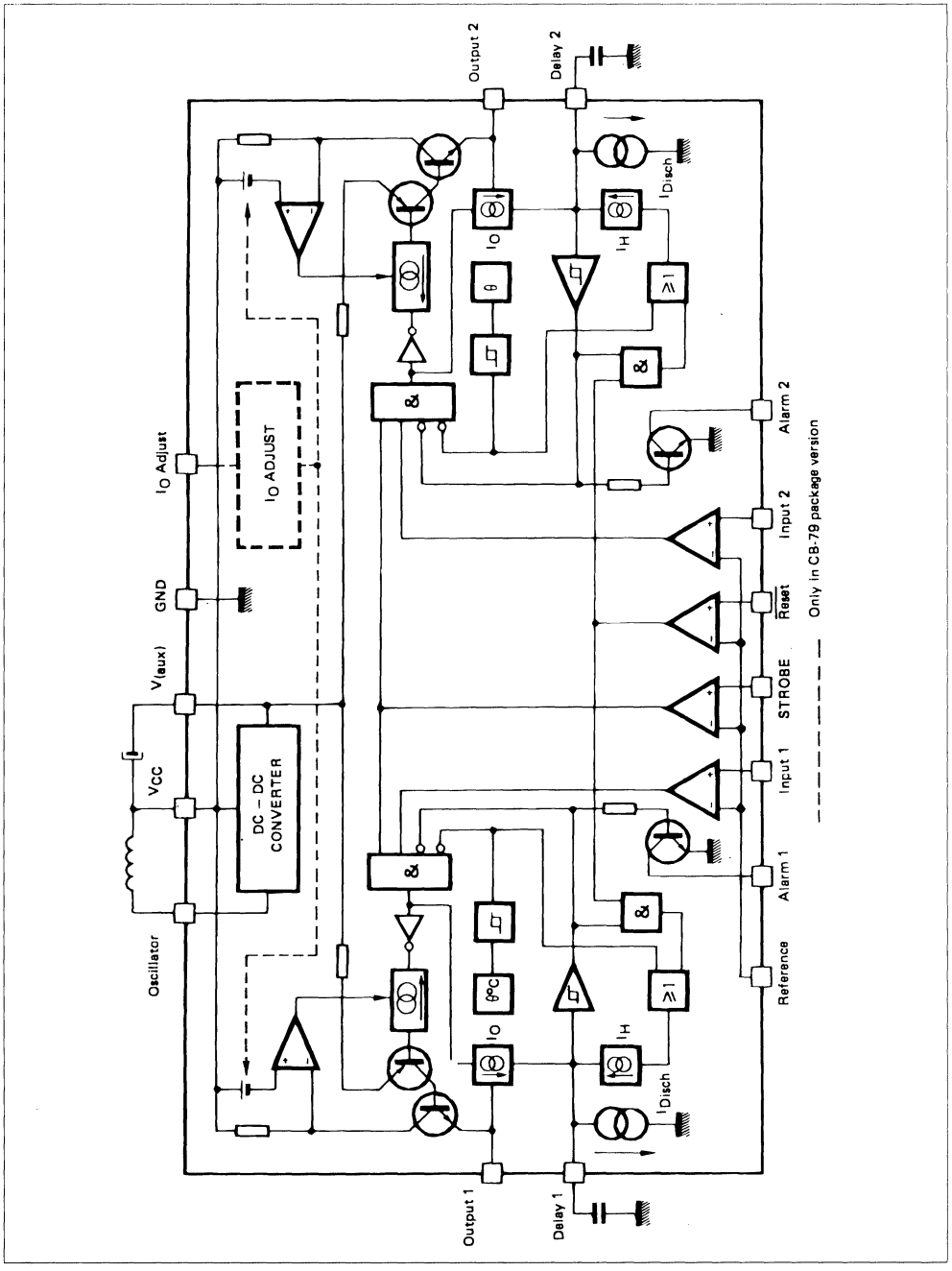
Symbol	Parameter	Value	Unit
V_{CC} (*)	Supply Voltage	+ 35	V
V_{I1} V_{I2} V_{reset} V_{strobe}	Input Voltages	30 to + 55	V
I_O	Output Current	Internally Limited	A
I_L	Current In DC/DC Converter Inductance	0.4	A
P_{tot}	Total Power Dissipation	Internally Limited	W
T_{oper}	Operating Free-air Temperature Range	− 40 to + 85	°C
T_j	Junction Temperature	+ 150	°C

* + 60 V (10 mS)

THERMAL DATA

$R_{th(j-c)}$	Maximum Junction–case Thermal Resistance	DIP.16 Multiwatt	25 2.5	°C/W
$R_{th(j-a)}$	Maximum Junction–ambient Thermal Resistance	DIP.16 Multiwatt	70 40	°C/W

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{CC} = + 24 V, − 40 °C, ≤ T_{amb} ≤ + 85 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	8		32	V
I_{CC}	Supply Current				mA
	Input 1 = Input 2 : Low	–	7		
	Input 1 = Input 1 : High, I_O = 2 x 2 A		25	32	
I_1	Input Current (all inputs)				
	$V_I > V_{ref}$		15	50	
	$V_I < V_{ref}$		0		
I_{OHA}	High Level Alarm Output Leakage Current (V_A = + 10 V)		0	10	µA
V_{OLA}	Low Level Alarm Output Voltage (I_A = + 10 mA)		1.1	1.3	V
$V_{CC} - V_O$	Power Outputs Dropout Voltage				V
	I_O = 0.5 A		0.15	0.25	
	I_O = 1 A		0.3	0.4	
	I_O = 2 A		0.6	0.7	
I_{OL}	Power Outputs Leakage Current			100	µA
t_{reset}	Reset Pulse Duration (C1 = C2 = 1 µF)		400		mS
t_d	Delay Time before Desaturation Monitoring Unit Becomes Active (C1 = C2 = 1µF)				mS
	$V_{CC} - V_O$ = + 12 V		20		
	$V_{CC} - V_O$ = + 24 V		10		
	$V_{CC} - V_O$ = + 32 V		5		
V_{ref}	Reference Input Voltage	1.4		55	V
I_{ref}	Reference Input Current (V_{ref} = 1.4 V)				µA
	All Inputs < V_{ref}		80	150	
	All Inputs > V_{ref}	− 1	0	+ 1	
I_O	Available Output Current				
	UAF1780DP $R_O = \infty$	2.5			A
	UAF1780DP R_O = 2 KΩ	1			
	UAF1780SP	2.5			
	UAF1781DP $R_O = \infty$	2			
	UAF1781DP R_O = 2 KΩ	1			
	UAF1782SP	2			
$V_{CC} - V_O$	Maximum Output Voltage Swing		–	50	V
$V_{aux} - V_{CC}$	DC/DC Output Voltage				
	0.5 A < I_O < 2 A (each output) CO = 47 µF, L = 100 µH	–	1.25	–	V

Fig. 1 – DIP. 16 PACKAGE.

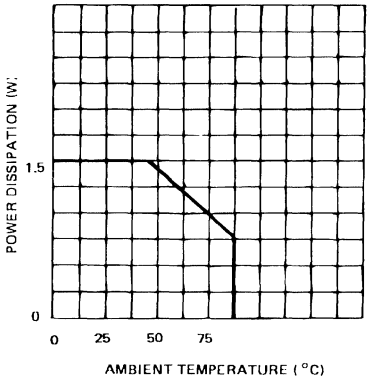


Fig. 2 – MULTIWATT PACKAGE.

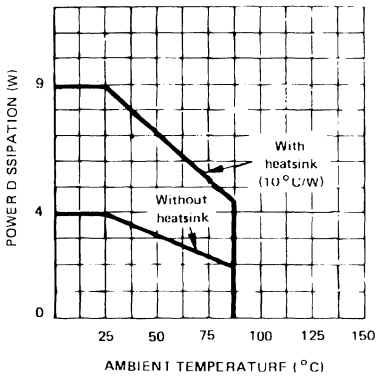


Fig. 3 – AVAILABLE OUTPUT CURRENT VS EXTERNAL RESISTANCE VALUE DIP. 16 PACKAGE.

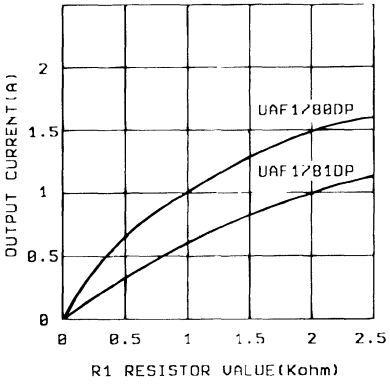


Fig. 4 – SATURATION VOLTAGE VS OUTPUT CURRENT.

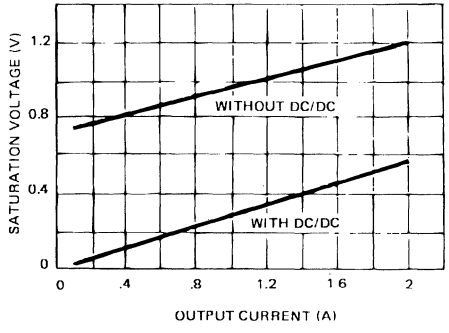


Fig. 5 – RESPONSE TIME.

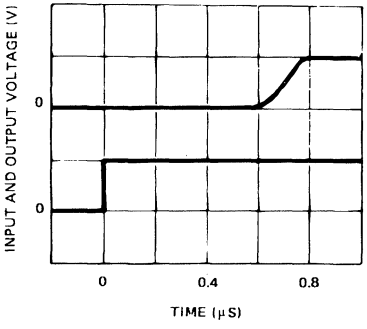


Fig. 6 RESPONSE TIME.

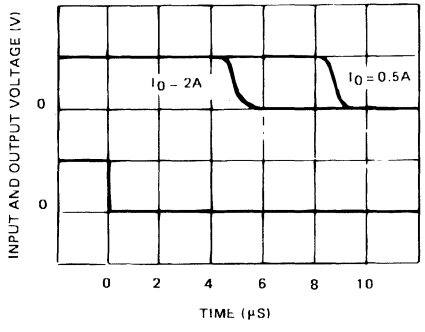
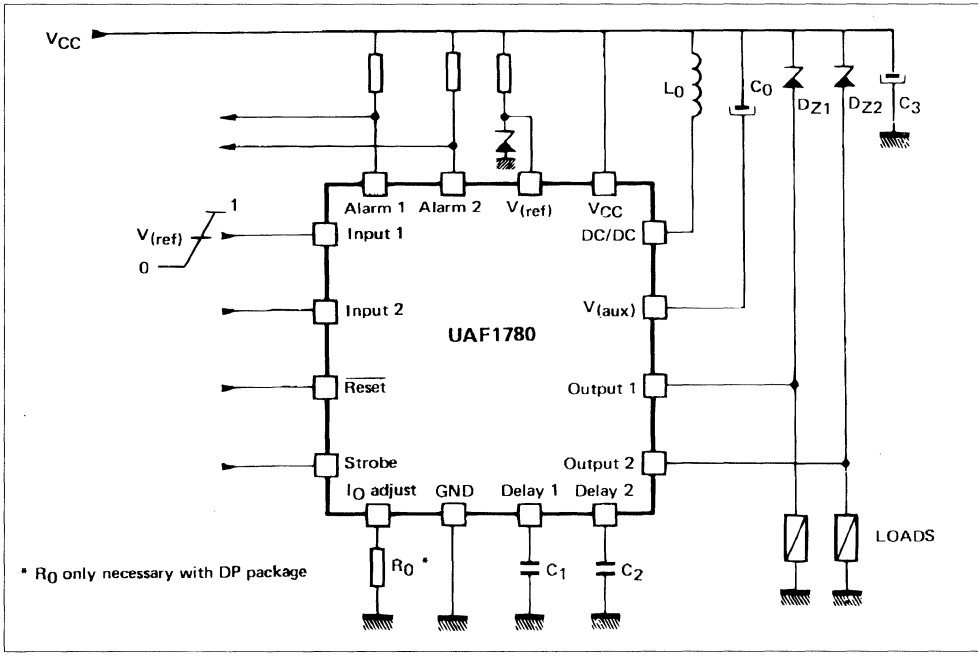
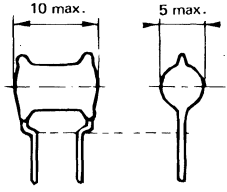


Figure 7 : Typical Application.



- L_O and C_O are the external elements of the dc/dc converter. Typical values and characteristics of these components are as follows :
  For L_O : - inductance = 100 µH (tolerance ± 10%)
  - maximal current ≥ 400 mA

Size Evaluation For dc/dc Inductance



For C_O : The value of this capacitor is not critical, a capacitor of C1 ≥ 47 F, Vn ≥ 6.3 V will be suitable for the majority of the applications.

- The on-chip dc/dc converter can be disabled by connecting $V_{(aux)}$ terminal to V_{CC} and leaving "Oscillator" pin floating.

- C_1 and C_2 implement two distinct functions :
  - response time required by the desaturation monitoring unit to become active.
  - time delay imposed on each power output prior to conduction.

$$t_d = \frac{C \cdot 3.5\ V}{7\ \mu A}$$

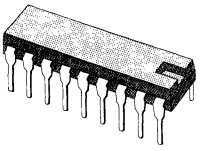
With $C_2 = C_3 = 1$ µF, the outputs are protected against voltage transients of as high as + 32 V and the response time of the desaturation monitoring unit is 400 ms.

- D_{Z1} and D_{Z2} Zener Diodes are required in the case of inductive loads. V_Z of these diodes should be < 60 V.

- R_O determines the value of maximum output current (DIP package). Its value is given in curve 3, where output current values are plotted against the corresponding values of this resistor.

PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

- ALL CONTROL, DRIVING, MONITORING, AND PROTECTION FUNCTIONS INCLUDED
- LOW-CURRENT, OFF-LINE START CIRCUIT
- FEED-FORWARD LINE REGULATION OVER 4 TO 1 INPUT RANGE
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- PULSE-BY-PULSE CURRENT LIMITING PLUS SHUTDOWN FOR OVER-CURRENT FAULT
- NO START-UP OR SHUTDOWN TRANSIENTS
- SLOW TURN-ON AND MAXIMUM DUTY-CYCLE CLAMP
- SHUTDOWN UPON OVER-OR UNDERVOLTAGE SENSING
- LATCH OFF OR CONTINUOUS RETRY AFTER FAULT
- REMOTE, PULSE-COMMANDABLE START/STOP
- PWM OUTPUT SWITCH USABLE TO 1A PEAK CURRENT
- 1% REFERENCE ACCURACY
- 500 kHz OPERATION



DIP-18
(Plastic and Ceramic)

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primaryside operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

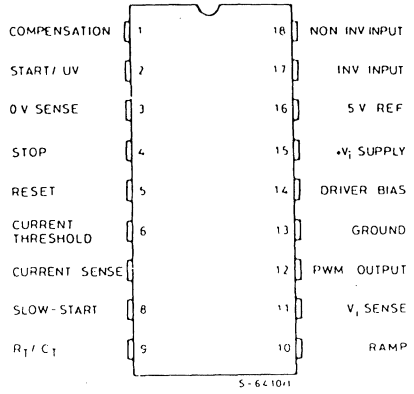
In addition to startup and normal regulating PWM functions, these devices ofter built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and highspeed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The UC1840 is characterized for operation over the full military temperature range of –55°C to +125°C. The UC2840 and UC3840 are designed for operation from –25°C to +85°C and 0°C to +70°C, respectively.

PIN CONNECTION AND ORDER CODES



Type	Plastic	Ceramic
UC1840	–	UC1840J
UC2840	UC2840N	UC2840J
UC3840	UC3840N	UC3840J

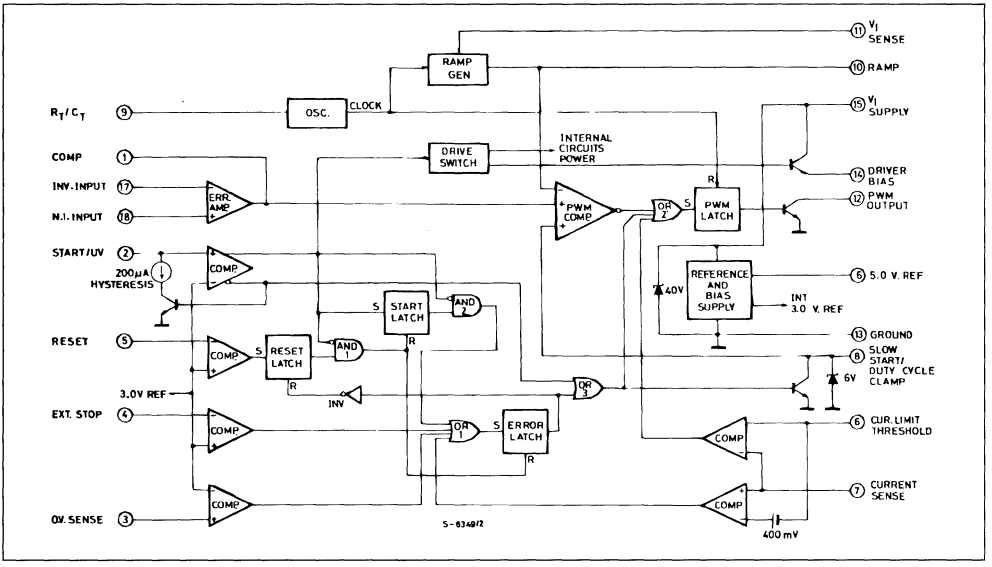
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_i	Supply Voltage + V_i (pin 15) Voltage Driven Current Driven 100 mA Maximum	 32 Self Limiting	 V
V_o	PWM Output Volage (pin 12)	40	V
I_o	PWM Output Current, Steady-state (pin 12)	400	mA
E_{op}	PWM Output Peak Energy Discharge Driver Bias Current (pin 14)	20 –200	µJ mA
$I_{o(REF)}$	Reference Output Current (pin 16) Slow Start Sink Current (pin 8) V_i Sense Current (pin 11) Current Limit Inputs (pin 6, 7) Comparator Inputs (pins 2, 3, 4, 5, 17, 18)	– 50 20 10 – 0.5 to + 55 – 0.3 to + 32	mA mA mA V V
P_{tot}	Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to + 150	°C
T_{op}	Operating Ambient Temperature Range : UC1840 UC2840 UC3840	– 55 to + 125 – 25 to + 85 0 to + 70	°C °C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Name	Function

PWM CONTROL

OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first-order correction factor ≈ 0.3 log (C_T x 10^{12}).
RAMP GENERATOR	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected ≤ C_T and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance : unity-gain stable.
REFERENCE GENERATOR	Precision 5.0 V for internal and external usage to 50 mA. Tracking 3.0 V reference for internal usage only with nominal accuracy of ± 2 %. 40 V clamp zener for chip 0. V. protection, 100 mA maximum current.
PWM COMPARATOR	Generates output pulse wich starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
PWM LATCH	Terminates the PWM output pulse when set by inputs for either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets wich each internal clock pulse.
PWM OUTPUT SWITCH	Transistor capable of sinking current to ground wich is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400 mA saturated with peak capacitance discharge in excess of one amp.

FUNCTIONAL DESCRIPTION (continued)

Name	Function
SEQUENCING FUNCTIONS	
START/U. V. SENSE	This comparator performs three functions. With an increasing voltage, it generates a turn-on signal at a start threshold With a decreasing voltage, it generates a U. V. fault signal at a lower level separated by a 200 µA hysteresis current. At the U. V. threshold, it also resets the Error Latch if the Reset Latch has been set.
DRIVE SWITCH	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
DRIVE BIAS	Supplies drive current to external power switch to provide turn-on bias.
SLOW START	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by R_SC_S for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider R_S R_{DC}.
START LATCH	Keeps low input voltage at initial turn-on from being defined as a U. V. fault. Sets at start level to monitor for U. V. fault.
RESET LATCH	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set, this latch resets the Start and Error latches at the U. V. low threshold, allowing a restart.
PROTECTION FUNCTIONS	
ERROR LATCH	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are : a. U. V. low (after turn-on) b. O. V. high c. Step low d. Current Sense 400 mV over threshold Error Latch resets at U. V. threshold if Reset Latch is set.
CURRENT LIMITING	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400 mV above threshold, a shutdown signal it sent to Error Latch.

ELECTRICAL CHARACTERISTICS (refer to the test circuit. Unless otherwise stated, these specifications apply for T_i = – 55 to + 125 °C for the UC1840, – 25 °C to + 85 °C for the UC2840 and 0 to + 70 °C for the UC3840; V_i = 20 V, R_T = 20 KΩ, C_T = 0.001μF, C_R = 0.001 μF, current limit threshold = 200 mV)

Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
POWER INPUTS									
I_{ST}	Start-up Current	V_i = 30 V, Pin 2 = 2.5 V, T_j = 25 °C		4	5.5		4	5.5	mA
	*Start-up Current T.C.	V_i = 30 V, Pin 2 = 2.5 V		– 0.1	– 0.2		– 0.1	– 0.2	%/°C
I_i	Operating Current	V_i = 30 V, Pin 2 = 3.5 V	5	10	15	5	10	15	mA
V_{SOV}	Supply O.V. Clamp	I_i = 20 m A	33	40	45	33	40	48	V
REFERENCE SECTION									
V_{REF}	Reference Voltage	T_j = 25 °C	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line Regulation	V_i = 8 to 30 V		10	15		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20mA		10	20		10	30	mV
$\Delta V_{REF}/\Delta T$*	Temperature Coeff.	Over Op. Temp. Range			± 0.4			± 0.4	mV/°C
I_{SC}	Short Circuit Curr.	V_{REF} = 0, T_j = 25 °C		– 80	– 100		– 80	– 100	mA
OSCILLATOR									
f_s	Nominal Frequency	T_j = 25 °C	47	50	53	45	50	55	KHz
	Voltage Stability	V_i = 8 to 30 V		0.5	1		0.5	1	%
	*Temperature Coeff.	Over Op. Temp. Range			± 0.8			± 0.8	%/°C
$f_{s(max)}$	Maxim. Frequency	R_T = 2 KΩ, C_T = 330 pF	500			500			KHz
RAMP GENERATOR									
	Ramp Current Min.	I_{SENSE} = – 10 μA		– 11	– 14		– 11	–14	μA
	Ramp Current Max.	I_{SENSE} = 1 mA	– 0.9	– 0.95		–0.9	–0.95		mA
	Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V
	Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

ELECTRICAL CHARACTERISTICS (continued)

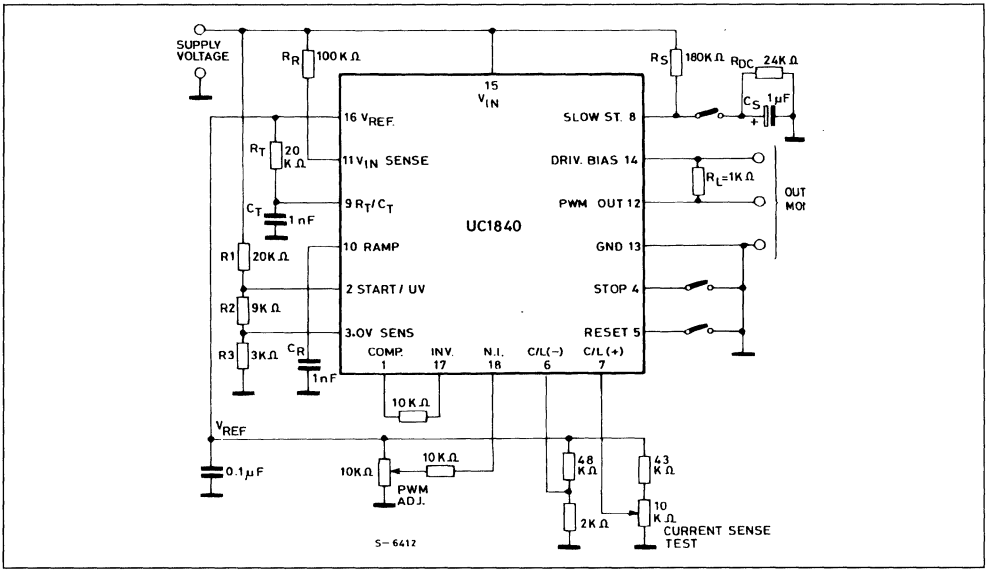
Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
ERROR AMPLIFIER									
V_{os}	Input Offset Voltage	V_{CM} = 5 V		0.5	5		2	10	mV
I_b	Input Bias Current			0.5	2		1	5	µA
I_{os}	Input Offset Current				0.5			0.5	µA
G_v	Open Loop Gain	ΔV_o = 1 to 3 V	60	66		60	66		dB
	Output Swing (max Out ≤ Ramp Peak – 100 mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMR	Common Mode Rejection	V_{CM} = 1.5 to 5.5 V	70	80		70	80		dB
SVR	Supply Voltage Rejection	V_i = 8 to 30 V	40	50		40	50		dB
I_{SC}	Short Circuit Current	V_{comp} = 0V		– 4	– 10		– 4	– 10	mA
B*	Gain Bandwidth	T_j = 25 °C, G_V = 0 dB	1	2		1	2		MHz
SR*	Slew Rate	T_j = 25 °C, G_V = 0 dB		0.8			0.8		V/µs
PWM SECTION									
	*Continuous Duty Cycle Range (other than zero)	Min. Total Cont. Range Ramp Peak < 4.2 V	5		95	5		95	%
$V_{o(sat)}$	Output Saturation	I_o = 20 mA		0.2	0.4		0.2	0.4	V
$V_{o(sat)}$	Output Saturation	I_o = 200 mA		1.7	2.2		1.7	2.2	V
I_{OL}	Output Leakage	V_o = 40 V		0.1	10		0.1	10	µA
τ_d	*Comparator Delay	Pin 8 to pin 12 T_j = 25 °C, R_L = 1 KΩ		300	500		300	500	ns
SEQUENCING FUNCTIONS									
V_T	Comparator Threshold	Pins 2, 3, 4, 5	2.8	3	3.2	2.8	3	3.2	V
I_b	Input Bias Current	Pins 3, 4, 5 = 0V		– 1	– 3		–1	–3	µA
	Start/UV Hysteresis Current	Pin 2 = 2.5 V, T_j = 25 °C	120	180	240	120	180	240	µA
	Input Leakage	V_i = 20 V		0.1	10		0.1	10	µA
	Driver Bias Saturation Voltage V_{IN}–V_{OH}	I_B = – 50 mA		2	3		2	3	V
	Driver Bias Leakage	V_B = 0V		– 0.1	– 10		– 0.1	– 10	µA
	Slow-start Saturation	I_s = 2 mA		0.2	0.5		0.2	0.5	V
	Slow-start Leakage	V_s = 4.5 V		0.1	2		0.1	2	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT CONTROL									
	Current Limit Offset			0	5		0	10	mV
	Current Shutdown Offset		340	400	440	340	400	440	mV
I_b	Input Bias Current	Pin 7 = 0V		– 2	– 5		– 2	– 5	µA
	*Common mode Range		– 0.3		3	– 0.3		3	V
τ_d*	Current Limit Delay	T_j = 25 °C, Pin 7 to 12 R_L = 1 KΩ		200	400		200	400	ns

* Guaranteed by design. Not 100 % tested in production.

Figure 1 : Open Loop Test Circuit.



Nominal frequency = $\frac{1}{R_T C_T}$ = 50 kHz

Start voltage = $3 \frac{(R1 + R2 + R3)}{R2 + R3} + 0.2$ R1 = 12 V

U.V. fault voltage = $3 \frac{(R1 + R2 + R3)}{R2 + R3}$ = 8 V

O.V. fault voltage = $3 \frac{(R1 + R2 + R3)}{R3}$ = 32 V

Current limit = 200mV

Current fault voltage = 600mV

Duty cycle clamp = 50%

Figure 2 : Start U.V. Hysteresis Current.

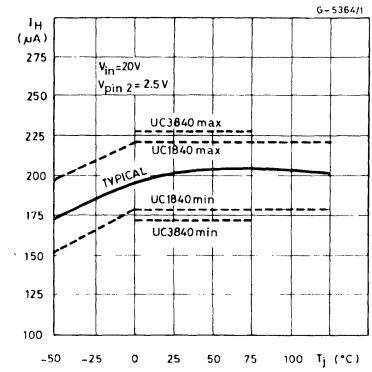


Figure 3 : PWM Output Saturation Voltage.

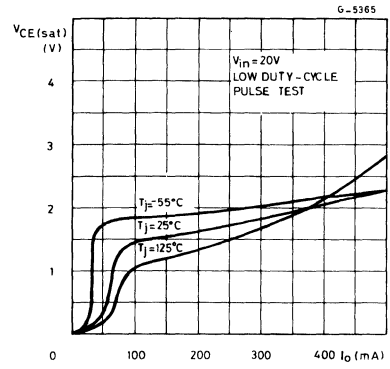


Figure 4 : Oscillator Frequency.

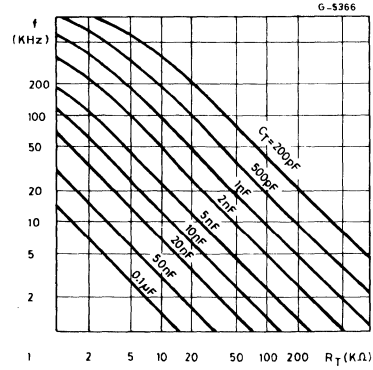


Figure 5 : PWM Output Minimum Pulse Width.

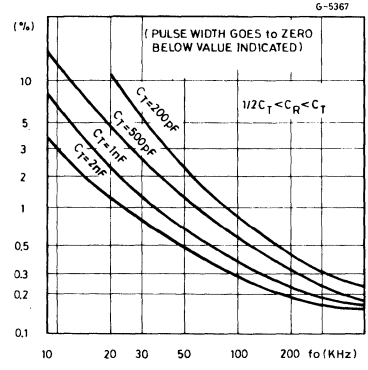


Figure 6 : Error Amplifier Open-loop Gain and Phase.

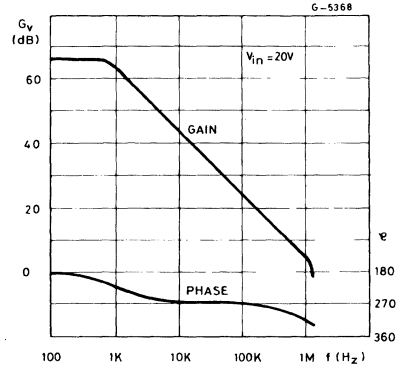
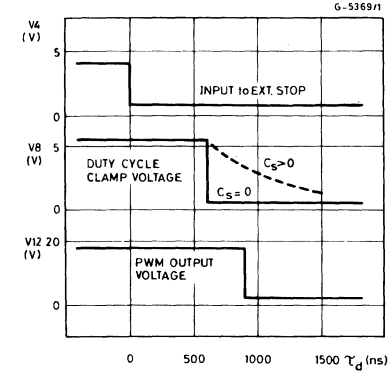
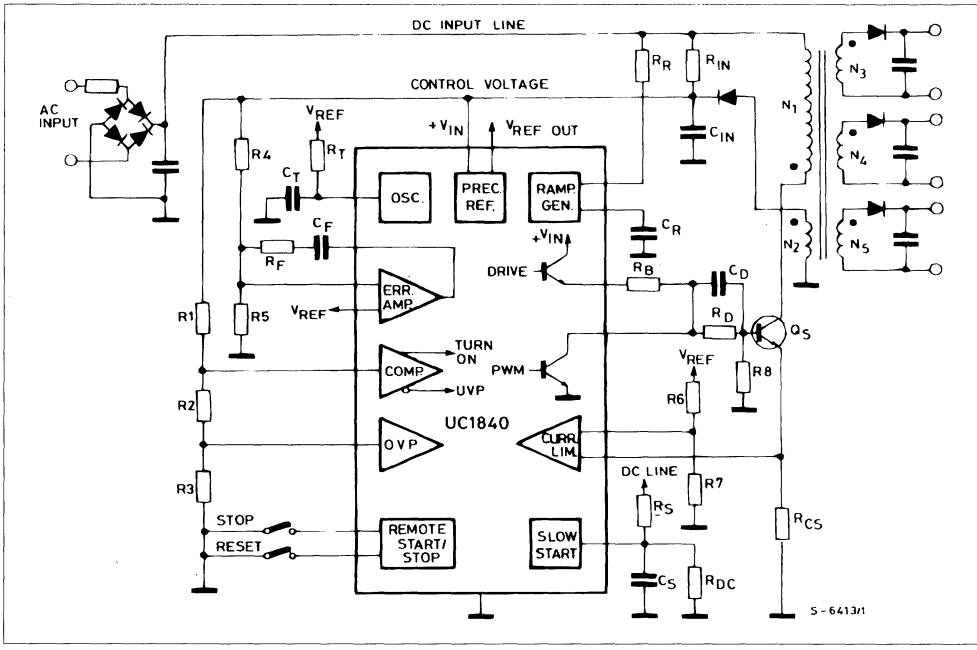


Figure 7 : Shutdown Timing.



APPLICATION INFORMATION

Figure 8 : Programmable PWM Controller in a Simplified Flyback Regulator.

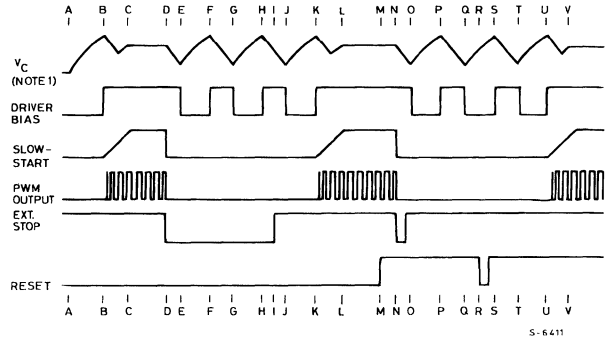


In this application [see Fig.8] complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding. N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling - a task made even easier with the UC1840's feed-forward line regulation.

The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application

Figure 9 : Power Sequencing Functions.



Notes : 1. VC represents an analog of the output voltage generated by a primary-referenced secondary winding of the power transformer. It is the voltage monitored by the start/U.V. comparator and, in most cases, is the supply voltage, Vi, for the UC1840.
2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

POWER FREQUENCY FUNCTIONS

Time	Event
A	Initial Turn-on, V_c Rises with Light Load
B	Start Threshold. Driver Bias Loads V_c
C	Operating PWM Regulates V_c
D	Stop Input Sets Error Latch Turning off PWM
E	U. V. Low Threshold. Error Latch Remain Set
F	Start Turns on Driver Bias Bus Error Latch Still Set
G H	V_c and Driver Bias Continue to Cycle
I	Stop Command Removed
J	Error Latch Reset at U. V. Low Threshold
K	Start Threshold Now Removes Slow-start Clam

Time	Event
L	Return to Normal Run State
M	Reset Latch Set Signal Removed
N	Error Latch Set with Momentary Fault
O	Error Latch does not reset as Reset Latch is reset
P Q	V_c and Driver Bias Recycle with no Turn-on
R	Reset Latch Set is Set with Momentary Reset Signal
S	V_c must Complete Cycle to Turn-on
T	Start and Error Latches Reset
U	Normal Start Initiated
V	Return to Normal Run State

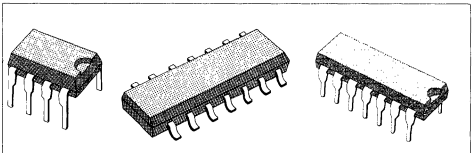
CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1 mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500 KHz OPERATION
- LOW R_O ERROR AMP

DESCRIPTION

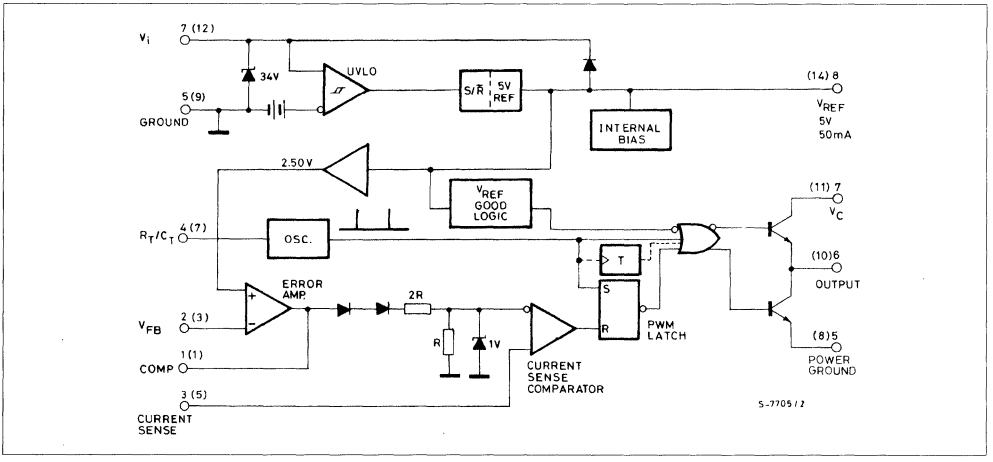
The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under voltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16 V (on) and 10 V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5 V and 7.9 V. The UC1842 and UC1843 can operate to duty cycles approaching 100 %. A range of the zero to < 50 % is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.



Minidip Plastic and Ceramic **SO-14 J** **DIP-14 Plastic**

BLOCK DIAGRAM (toggle flip flop used only in UC1844 and UC1845)



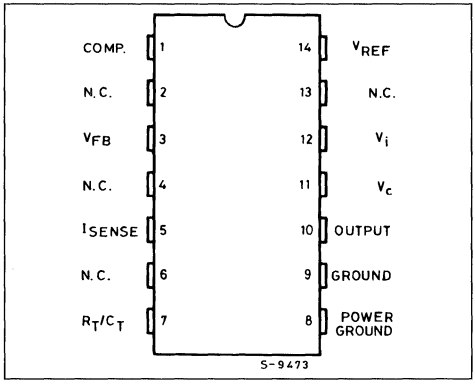
ABSOLUTE MAXIMUM RATINGS *

Symbol	Parameter	Value	Unit
V_i	Supply Voltage (low impedance source)	30	V
V_i	Supply Voltage (I_i < 30 mA)	Self Limiting	
I_O	Output Current	± 1	A
E_O	Output Energy (capacitive load)	5	μJ
	Analog Inputs (pins 2, 3)	– 0.3 to 6.3	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 50$ ° C (minidip, DIP-14)	1	W
P_{tot}	Power Dissipation at $T_{amb} \leq 25$ ° C (SO-14)	725	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_L	Lead Temperature (soldering 10 s)	300	°C

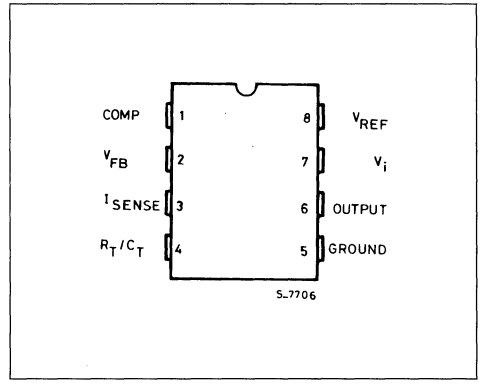
* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

BLOCK DIAGRAM (top view)

DIP-14 / SO-14.



Minidip Plastic and Ceramic.



ORDERING NUMBERS

TYPE	PLASTIC MINIDIP	CERAMIC MINIDIP	DIP-14	SO-14
UC1842		UC1842J		
UC1843		UC1843J		
UC1844		UC1844J		
UC1845		UC1845J		
UC2842	UC2842N	UC2842J	UC2842B	UC2842D
UC2843	UC2843N	UC2843J	UC2843B	UC2843D
UC2844	UC2844N	UC2844J	UC2844B	UC2844D
UC2845	UC2845N	UC2845J	UC2845B	UC2845D
UC3842	UC3842N	UC3842J	UC3842B	UC3842D
UC3843	UC3843N	UC3843J	UC3843B	UC3843D
UC3844	UC3844N	UC3844J	UC3844B	UC3844D
UC3845	UC3845N	UC3845J	UC3845B	UC3845D

THERMAL DATA

		Ceramic Minidip	Plastic Minidip	DIP-14 Plastic	SO-14
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	200 °C/W	100 °C/W	100 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (unless otherwise stated, these specifications apply for $-55 \le T_{amb} \le 125$ °C for UC184X ; $-25 \le T_{amb} \le 85$ °C for UC284X ; $0 \le T_{amb} \le 70$ °C for UC384X ; V_i = 15 V (Note 5) ; R_T = 10 K ; C_T = 3.3 nF)

Symbol	Parameter	Test Conditions	UC184X 284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION									
V_{REF}	Output Voltage	T_j = 25 °C I_o = 1 mA	4.95	5.00	5.05	4.90	5.00	5.10	V
ΔV_{REF}	Line Regulation	12 V ≤ V_i ≤ 25 V		6	20		6	20	mV
ΔV_{REF}	Load Regulation	1 ≤ I_o ≤ 20 mA		6	25		6	25	mV
$\Delta V_{REF}/\Delta T$	Temperature Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/°C
	Total Output Variation	Line, Load, Temperature (Note 2)	4.9		5.1	4.82		5.18	V
e_N	Output Noise Voltage	10 Hz ≤ f ≤ 10 KHz T_j = 25 °C (Note 2)		50			50		µV
	Long Term Stability	T_{amb} = 125 °C, 1000 Hrs (Note 2)		5	25		5	25	mV
I_{sc}	Output Short Circuit		−30	−100	−180	− 30	−100	−180	mA
OSCILLATOR SECTION									
f_s	Initial Accuracy	T_j = 25 °C (Note 6)	47	52	57	47	52	57	KHz
	Voltage Stability	12 ≤ V_i ≤ 25 V		0.2	1		0.2	1	%
	Temperature Stability	$T_{MIN} \le T_{amb} \le T_{MAX}$ (Note 2)		5			5		%
V_4	Amplitude	V_{PIN4} Peak to Peak		1.7			1.7		V
ERROR AMP SECTION									
V_2	Input Voltage	V_{PIN1} = 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
I_b	Input Bias Current			− 0.3	− 1		− 0.3	− 2	µA
	A_{VOL}	2 ≤ V_o ≤ 4 V	65	90		65	90		dB
B	Unity Gain Bandwidth	(Note 2)	0.7	1		0.7	1		MHz
SVR	Supply Voltage Rejection	12 ≤ V_i ≤ 25 V	60	70		60	70		dB
I_o	Output Sink Current	V_{PIN2} = 2.7 V V_{PIN1} = 1.1 V	2	6		2	6		mA
I_o	Output Source Current	V_{PIN2} = 2.3 V V_{PIN1} = 5 V	− 0.5	− 0.8		− 0.5	− 0.8		mA
	V_{OUT} High	V_{PIN2} = 2.3 V ; R_L = 15 KΩ to Ground	5	6		5	6		V
	V_{OUT} Low	V_{PIN2} = 2.7 V ; R_L=15 KΩ to Pin 8		0.7	1.1		0.7	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC184X UC284X			UC384X			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT SENSE SECTION									
G_v	Gain	(Notes 3 & 4)	2.85	3	3.15	2.8	3	3.2	V/V
V_3	Maximum Input Signal	V_{PIN1} = 5 V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
SVR	Supply Voltage Rejection	12 ≤ V_i ≤ 25 V (Note 3)		70			70		dB
I_b	Input Bias Current			– 2	– 10		– 2	– 10	µA
	Delay to Output			150	300		150	300	ns
OUTPUT SECTION									
I_{OL}	Output Low Level	I_{SINK} = 20 mA		0.1	0.4		0.1	0.4	V
		I_{SINK} = 200 mA		1.5	2.2		1.5	2.2	
I_{OH}	Output High Level	I_{SOURCE} = 20 mA	13	13.5		13	13.5		V
		I_{SOURCE} = 200 mA	12	13.5		12	13.5		
t_r	Rise Time	T_j = 25 °C C_L = 1 nF (Note 2)		50	150		50	150	ns
t_f	Fall Time	T_j = 25 °C C_L = 1 nF (Note 2)		50	150		50	150	ns
UNDER-VOLTAGE LOCKOUT SECTION									
	Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
		X843/5	7.8	8.4	9.0	7.8	8.4	9.0	
	Min. Operating Voltage After Turn-on	X842/4	9	10	11	8.5	10	11.5	V
		X843/5	7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION									
	Maximum Duty Cycle	X842/3	93	97	100	93	97	100	%
		X844/5	44	48	50	45	48	50	
	Minimum Duty Cycle				0			0	%
TOTAL STANDBY CURRENT									
I_{st}	Start-up Current			0.5	1		0.5	1	mA
I_i	Operating Supply Current	V_{PIN2} = V_{PIN3} = 0 V		11	20		11	20	mA
V_{iz}	Zener Voltage	I_i = 25 mA		34			34		V

Notes : 2. These parameters, although guaranteed, are not 100% tested in production.
3. Parameter measured at trip point of latch with V_{PIN2} = 0.
4. Gain defined as :

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8 \text{ V}$$

5. Adjust V_i above the start threshold before setting at 15 V.
6. Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.

Figure 1 : Error Amp Configuration.

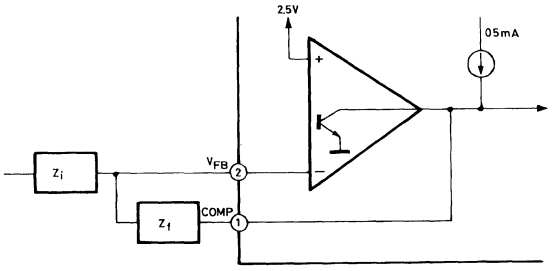
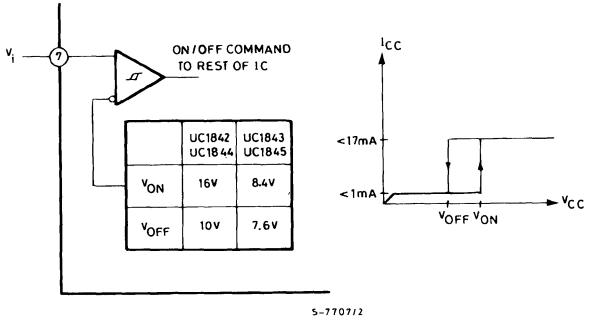
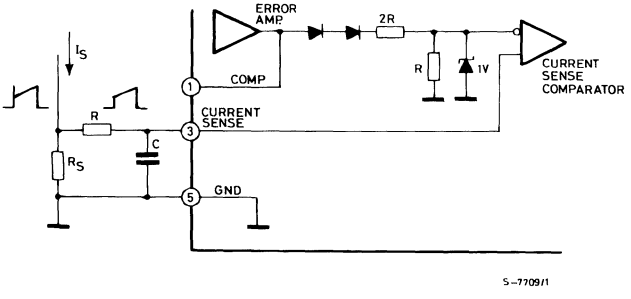


Figure 2 : Under Voltage Lockout.



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

Figure 3 : Current Sense Circuit .



PEAK CURRENT (I_S) IS DETERMINED BY THE FORMULA

$$I_{S\,max} \approx \frac{1.0\ V}{R_S}$$

A SMALL RC FILTER MAY BE REQUIRED TO SUPPRESS SWITCH TRANSIENTS.

Figure 4.

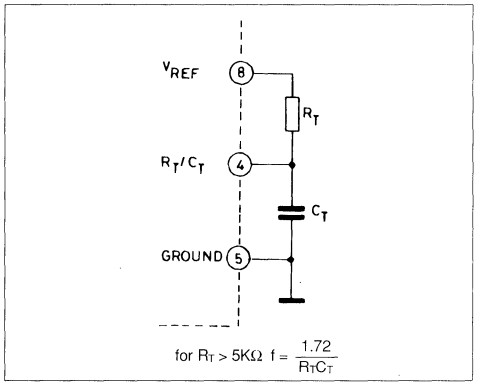


Figure 5 : Deadtime vs. C_T (R_T > 5KΩ).

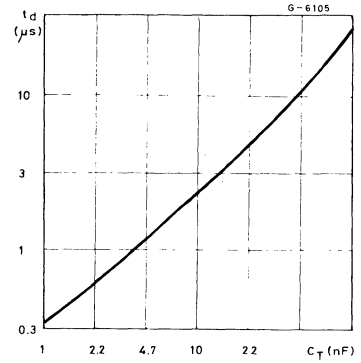


Figure 6 : Timing Resistance vs. Frequency.

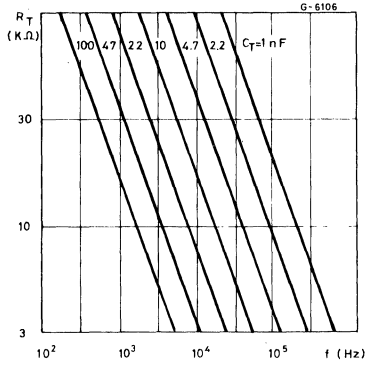


Figure 7 : Output Saturation Characteristics.

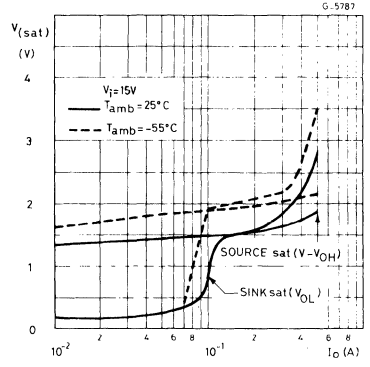


Figure 8 : Error Amplifier Open-loop Frequency Response.

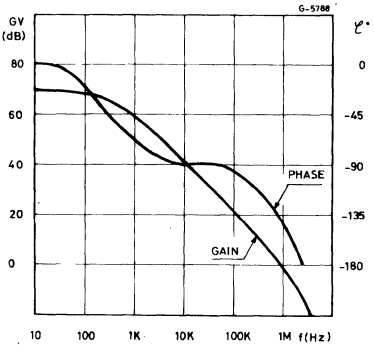
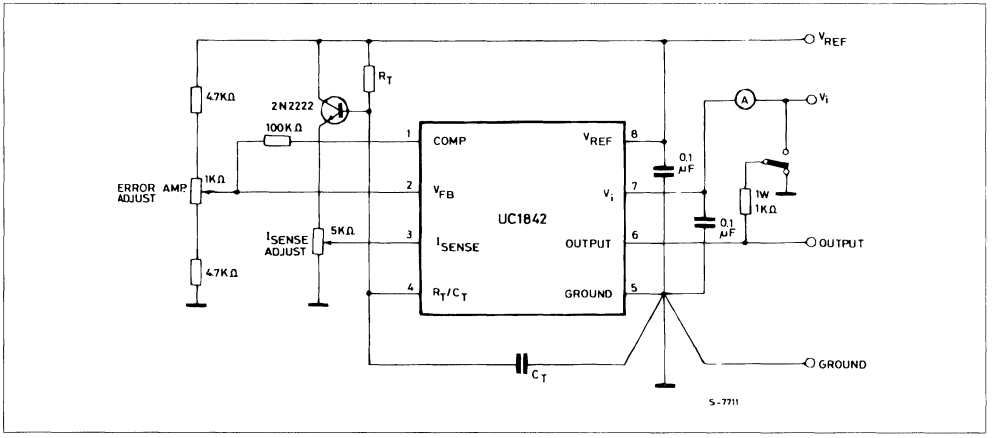
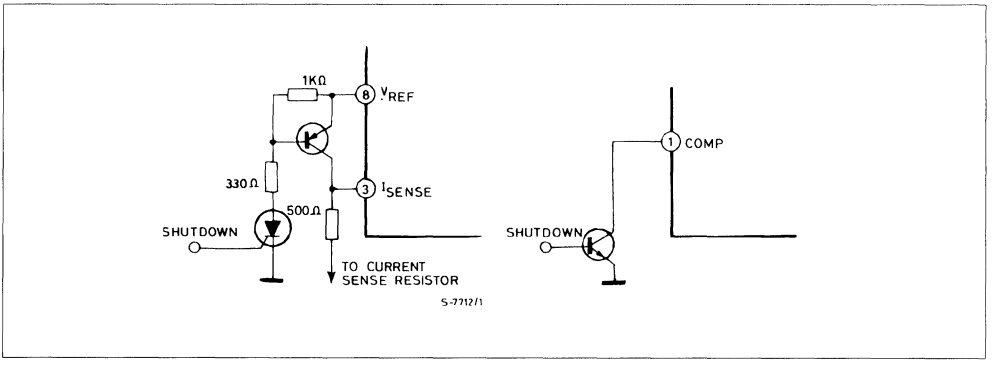


Figure 9 : Open Loop Test Circuit.



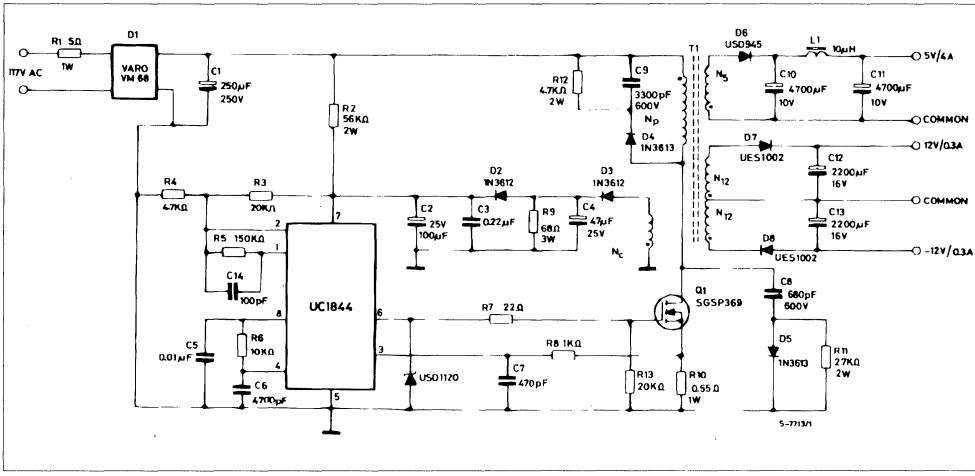
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 10 : Shutdown Techniques.



Shutdown of the UC1842 can be accomplished by two methods ; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

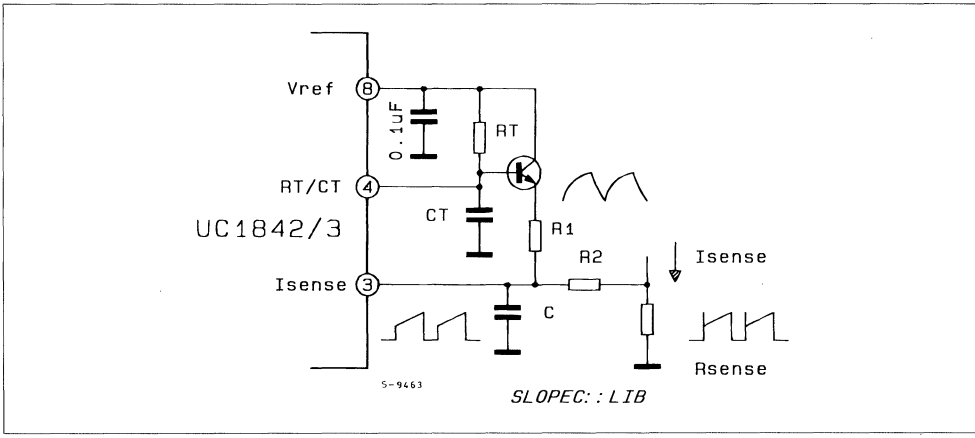
Figure 11 : Off-line Flyback Regulator.



Power Supply Specifications

1. Input Voltage : 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation : 3750 V
3. Switching Frequency : 40 KHz
4. Efficiency @ Full Load : 70 %
5. Output Voltage :
   A. + 5 V, ± 5 % : 1 A to 4 A load
   Ripple voltage : 50 mV P-P Max.
   B. + 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.
   C. – 12 V, ± 3 % : 0.1 A to 0.3 A load
   Ripple voltage : 100 mV P-P Max.

Figure 12 : Slope Compensation.



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50 %.

Note that capacitor, C, forms a filter with R_2 to suppress the leading edge switch spikes.

SGS-THOMSON MICROELECTRONICS

UCN4801A

BIMOS LATCH/DRIVERS

ADVANCE DATA

- HIGH-VOLTAGE, HIGH-CURRENT OUTPUTS
- OUTPUT TRANSIENT PROTECTION
- CMOS, PMOS, NMOS, TTL COMPATIBLE INPUTS
- INTERNAL PULL-DOWN RESISTORS
- LOW-POWER CMOS LATCHES

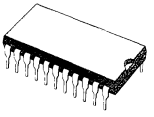
DESCRIPTION

The UCN4801A is a high-voltage, high-current latch/driver comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility.

The CMOS inputs are compatible with standard CMOS, PMOS and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power load.

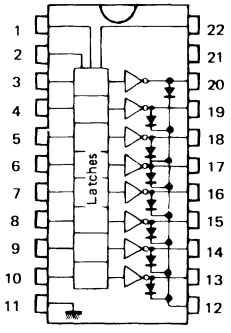
The unit feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

DIP-22
(Plastic)



ORDER CODE : UCN4801ADP

PIN CONNECTIONS (Top view)



1 - Clear
2 - Strobe
3 - Input 1
4 - Input 2
5 - Input 3
6 - Input 4
7 - Input 5
8 - Input 6
9 - Input 7
10 - Input 8
11 - GND

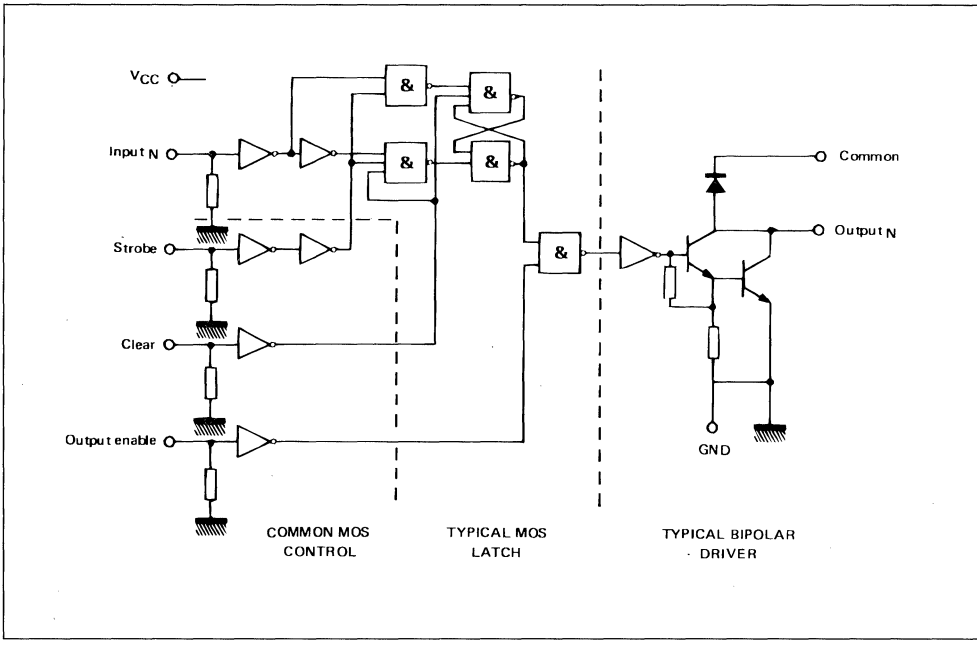
22 - Output enable
21 - V_{CC}
20 - Output 1
19 - Output 2
18 - Output 3
17 - Output 4
16 - Output 5
15 - Output 6
14 - Output 7
13 - Output 8
12 - Common

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_O	Output Voltage	50	V
V_{CC}	Supply Voltage	18	V
V_I	Input Voltage Range	− 0.3 to V_{CC} + 0.3	V
I_C	Continuous Collector Current	500	mA
P_{tot}	Power Dissipation*	2.0	W
T_{op}	Operating Ambient Temperature Range	− 20 to + 85	°C
T_{stg}	Storage Temperature	− 55 to + 125	°C

* Derate at the rate of 20 m/°C above T_{amb} = + 25 °C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, V_{CC} = 5 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_O	Output Leakage Current (V_O = 50 V)				µA
	T_{amb} = + 25 °C	–	–	50	
	T_{amb} = + 70 °C	–	–	100	
$V_{O(Sat)}$	Collector-emitter Saturation Voltage				V
	I_O = 100 mA	–	0.9	1.1	
	I_O = 200 mA	–	1.1	1.3	
	I_O = 350 mA, V_{CC} = 7 V	–	1.3	1.6	
$V_{I(O)}$	Input Voltage	–	–	1	V
$V_{I(1)}$	V_{CC} = 15 V	13.5	–	–	
	V_{CC} = 10 V	8.5	–	–	
	V_{CC} = 5 V - (note 1)	3.5	–	–	
R_{IN}	Input Resistance				KΩ
	V_{CC} = 15 V	50	200	–	
	V_{CC} = 10 V	50	300	–	
	V_{CC} = 5 V	50	600	–	
$I_{CC(on)}$	Supply Current - Outputs Open				mA
(each stage)	V_{CC} = 15 V	–	1	2	
	V_{CC} = 10 V	–	0.9	1.7	
	V_{CC} = 5 V	–	0.7	1	
$I_{CC(off)}$	All Drivers off, All Inputs = 0 V	–	50	100	µA
I_R	Clamp Diode Leakage Current (V_R = 50 V)				µA
	T_{amb} = + 25 °C	–	–	50	
	T_{amb} = + 70 °C	–	–	100	
V_F	Clamp Diode Forward Voltage I_F = 350 mA	–	1.7	2	V

Note : 1. Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "I".

TRUTH TABLE

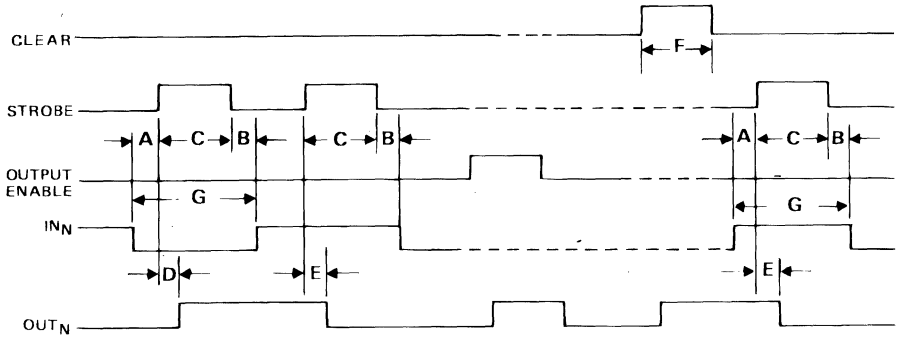
			Output	OUT_N	
IN_N	Strobe	Clear	Enable	t–1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON

X = irrelevant
t-1 = previous output state
t = present output state

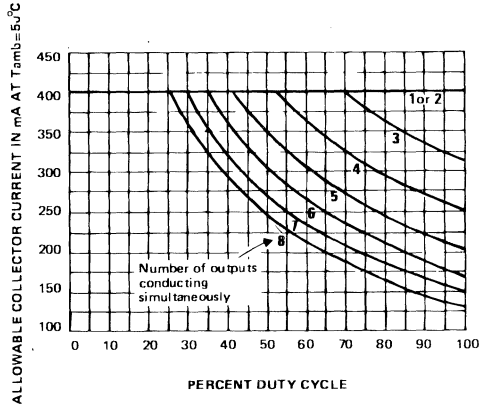
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TIMING CONDITIONS

(Logic levels are V_{CC} and GND) V_{CC} = 5 V, Tamb + 25°C



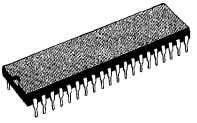
A. Minimum data active time before strobe enabled (data set-up time)	100 ns
B. Minimum data active time after strobe disabled (data hold time)	100 ns
C. Minimum strobe pulse width	300 ns
D. Typical time between strobe activation and output on to off transition	500 ns
E. Typical time between strobe activation and output off to on transition	500 ns
F. Minimum clear pulse width	300 ns
G. Minimum data pulse width	500 ns



A.C. PLASMA PANEL DRIVER

- 32-BIT SHIFT REGISTER WITH LATCHES
- DECODING LOGIC CIRCUIT
- LOW TO HIGH VOLTAGE INTERFACE FOR DIRECT CONNECTION TO 32 ELECTRODES

DIP-40
(Plastic)



ORDER CODE : UEB4732DP

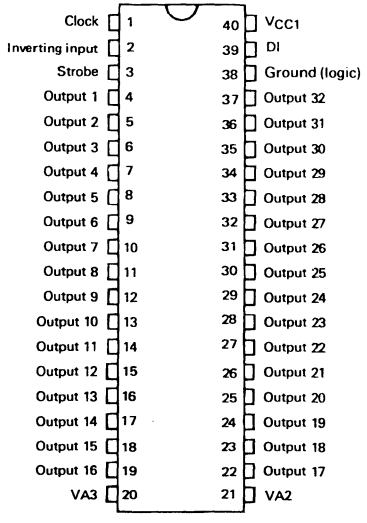
DESCRIPTION

UEB4732 is a BIMOS* IC's especially designed to provide selective and sustain signals needed by the X and Y electrodes of an A.C. plasma panel.

Realizing a complete A.C. plasma panel control system requires only UEB4732 and two high voltage common amplifiers for rows and columns of the panel. The whole network is driven by a few CMOS logical signals.

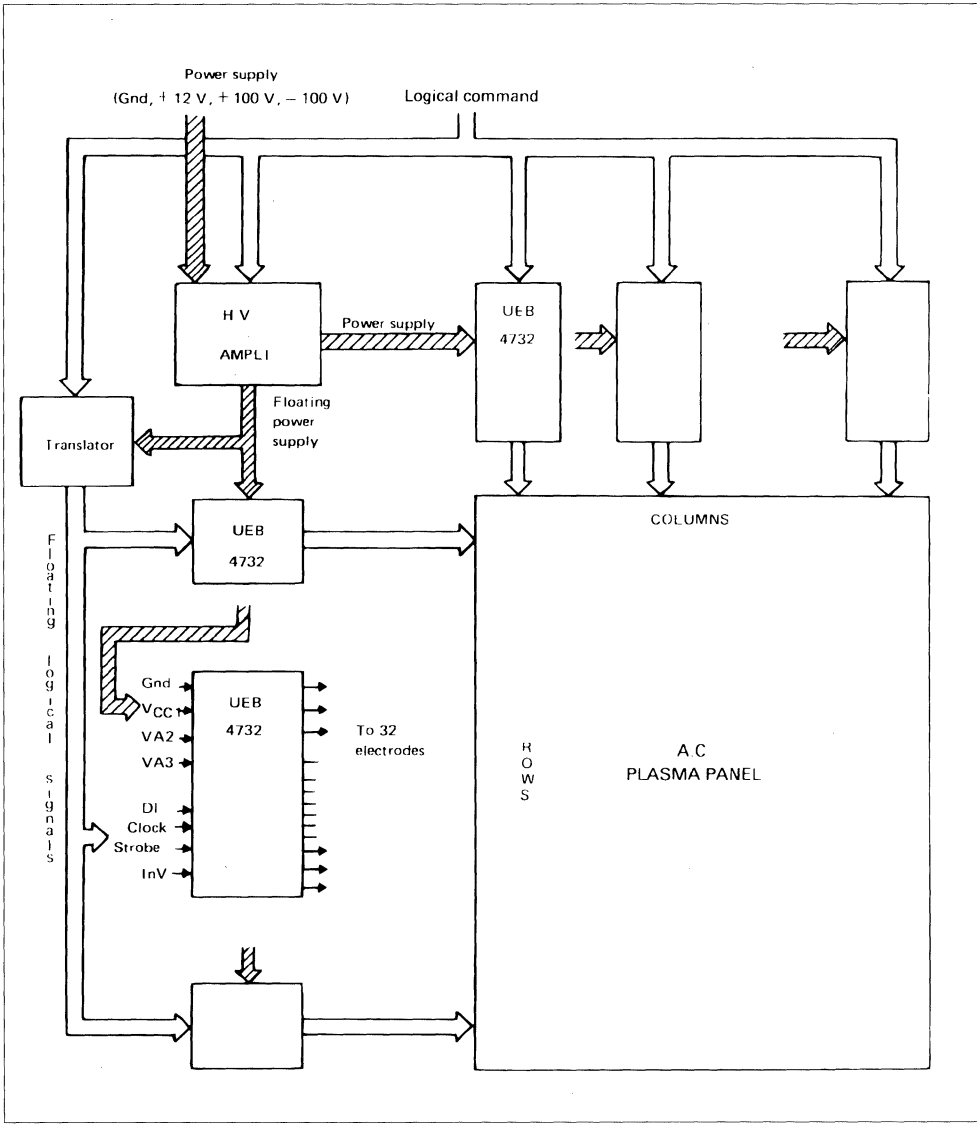
* Bipolar CMOS and complementary DMOS on same chip.

PIN CONNECTION



- 4 CMOS compatible logic inputs : DI, Clock, Strobe, Inv.
- 32 totem pole 100 V outputs, with clamping diodes to the VA2 and VA3 inputs.
- Logic supplies (Ground and V_{CC1}) separated from hight voltage (VA2, VA3) to avoid disturbances.

TYPICAL APPLICATION

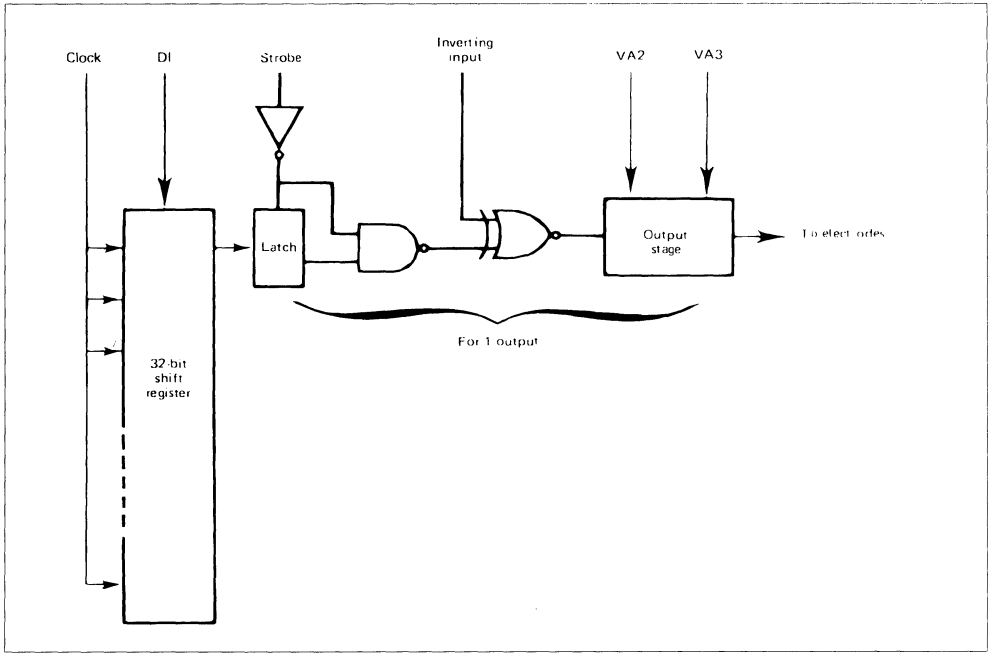


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC1}	Logic Supply Voltage	18	V
V_{A2}	V_{A2} Voltage ($V_{A2} \geq V_{A3}$)	120	V
V_{A3}	V_{A3} Voltage	10	V
V_i	Input Voltage Range	− 0.3 to V_{CC1} + 0.3	V

NOTE: Voltage values are with respect to network ground terminal (ground logic).

SCHEMATIC DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS (over recommended operating range)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	High Level Dropout Voltage (for one output) V_{A2} > 20 V				V
	− I_{OH} = − 10 mA		5	10	
	− I_{OH} = − 20 mA		10	20	
V_{OL}	Low Level Dropout Voltage (for one output) V_{A3} = Ground				V
	− I_{OL} = 10 mA		5	10	
	− I_{OL} = 20 mA		10	20	
V_{OK}	Dropout Clamp Voltage				V
	− I_O = ± 100 mA in One Output			2	
	− I_O = ± 100 mA Simultaneously in the 32 Outputs			3	
f_{clock}	Maximum Clock Pulse Frequency	4	8		MHz

* All typical values are at V_{CC1} = 12 V, T_{amb} = 25 °C.

RECOMMANDED OPERATING CONDITIONS (voltage values are referred to logic ground of the IC)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Logic Supply Voltage	10		15	V
V_{A2}	V_{A2} Voltage ($V_{A2} \geq V_{A3}$)	– 0.6		120	V
V_{A3}	V_{A3} Voltage	– 0.6		10	V
I_O	Peak Current (for one output) – High Level V_{A2} > 20 V – Low Level V_{A3} = Ground		– 20 20		mA
I_O	Peak Clamp Current (for one output)		± 100		mA
T_{amb}	Operating Free Air Temperature UEB4732	0		+ 70	°C

FUNCTION TABLE

Functions	Data	Inputs		Strobe	Shift Register			Latchs			Outputs		
		Clock	Inv.		R1	R2	R32	L1	L2	L32	01	02	032
LOAD	H	↑	X	X	H	R1n	R31n	R1s	R2s	R32s	Levels at 01 through 032 depend on Inv. and strobe (see "strobe").		
	L	↑	X	X	L	R1n	R31n	R1s	R2s	R32s			
LATCH	X	H	L	↓	R1n	R2n	R32n	R1n	R2n	R32n	R1n	$\overline{R2n}$	$\overline{R32n}$
	X	H	H	↓	R1n	R2n	R32n	R1n	R2n	R32n	$\overline{R1n}$	R2n	$\overline{R32n}$
STROBE	X	X	L	L	Levels at R1 through R32 depend only on data and clock (see "load").			R1s	R2s	R32s	$\overline{R1s}$	$\overline{R2s}$	$\overline{R32s}$
	X	X	H	L				R1s	R2s	R32s	$\overline{R1s}$	$\overline{R2s}$	$\overline{R32s}$
	X	X	L	H				R1	R2	R32	L	L	L
	X	X	H	H				R1	R2	R32	H	H	H

H = High level L = Low level X = Irrelevant

↑ = Low to high transition ↓ = High to low transition

For the outputs, the high level (H) is V_{A2}, the low level (L) is V_{A3}.

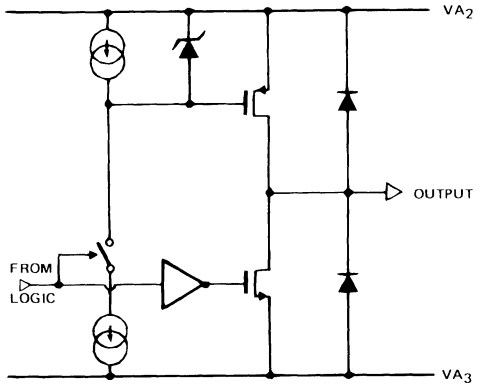
R1.....R32 = Levels currently at internal outputs of shift register.

R1n....R32n = Levels at shift register outputs R1 through R32, respectively, before the most recent ↑ transition of clock.

R1s....R32s = Levels at shift register outputs R1 through R32, respectively, before the most recent ↓ transition of strobe (levels currently stored by the 32 latchs L1 through L32).

$\overline{R1s}$.....$\overline{R32s}$ = Logical inversion of R1s.....R32s.

SCHEMATIC OF ONE OUTPUT STAGE



During the sustaining signal, $V_{A2} = V_{A3}$ and the current flows through the two clamp diodes.

During the selective signals (write and erase on the plasma panel), V_{A2} is at high voltage (typ.100 V, referred to logic ground) V_{A3} is equal to logic ground, and the output is selectively adressed by complementary by DMOS stage.

DESCRIPTION

The UEB4732 is designed to provide easily the line and the column select operation of a plasma display panel. For an use on the X axis of the panel, the Inv. input is set at a steady low level, the outputs are normally low and are selectively switched high when the strobe input is low. For an use on the Y axis of the panel, the Inv. input is set at a steady high level, the outputs are normally high and are selectively switched low when the strobe input is low (the 32 bit data is inverted).

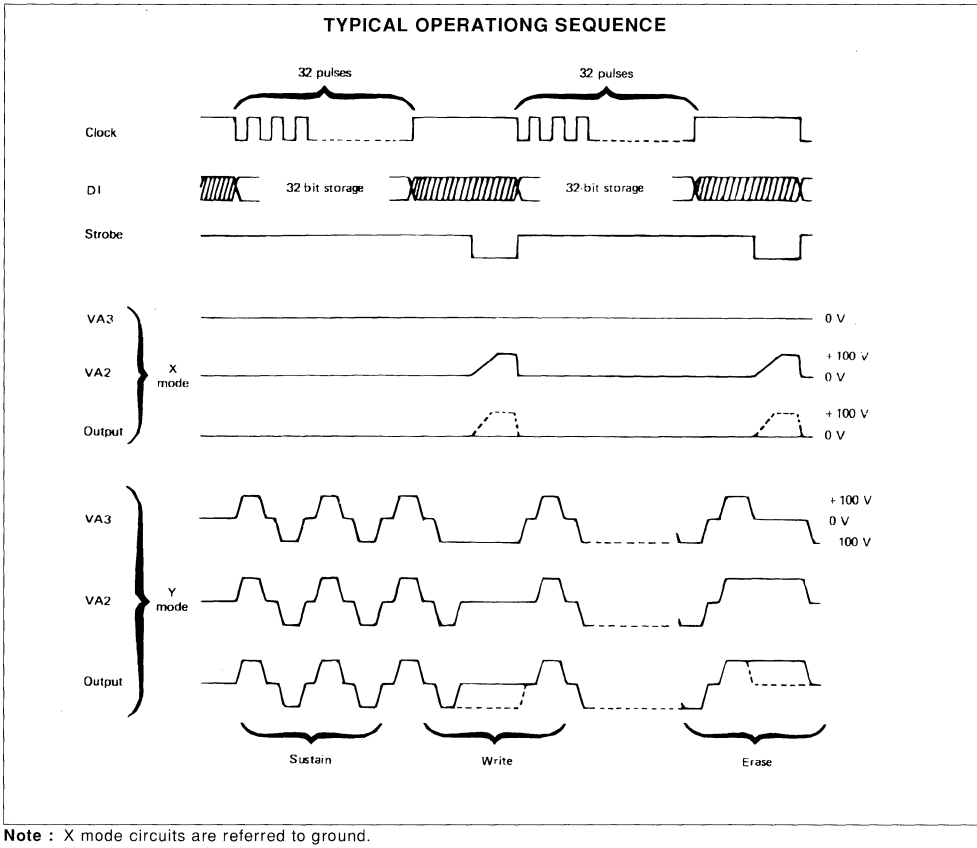
The Inv. input may also be used as a sustain input : when strobe is high, if the Inv. input is switched low, all outputs switch low, if the Inv. input is switched high, all outputs switch high.

Data is enterred serially in the shift register, on the low to high level transition of clock. It is stored in the 32 latchs on the high to low level transition of strobe, so the outputs are stable during the low level of strobe, regradless of the state of clock and data, and a new data can be enterred immediately.

The logical voltage reference (ground logic) and the high voltage reference (V_{A3}) are separated to avoid disturbances.

All output stages are complementary DMOS and contain clamp diodes to the V_{A2} and V_{A3} supply inputs. These diodes are designed to provide the peak current of the sustaining signal (typ. 100 mA/output) without distorsion of the signal.

TIMING DIAGRAM



Note : X mode circuits are referred to ground.
Y mode ones are floating on sustaining voltage.
In X mode, Inv. input is low.
In Y mode, Inv. input is high.

SGS-THOMSON MICROELECTRONICS

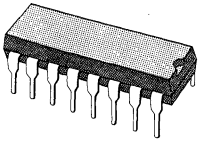
ULN2001A-ULN2003A
ULN2002A-ULN2004A

SEVEN DARLINGTON ARRAYS

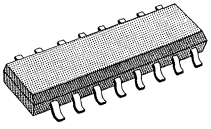
- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUTS CAN BE PARALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays filament lamps, thermal printheads and high power buffers.

The ULN2001A/2002A/2003A and 2004A are supplied in 16 pin plastic DIP packages with a copper leadframe to reduce thermal resistance. They are available also in small outline package (SO-16) as ULN2001D/2002D/2003D/2004D.



DIP-16 Plastic
(0.25)



SO-16J

ORDER CODES :
ULN2001A/2A/3A/4A (DIP-16)
ULN2001D/2D/3D/4D (SO-16)

DESCRIPTION

The ULN2001A, ULN2002A, ULN2003 and ULN2004A are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

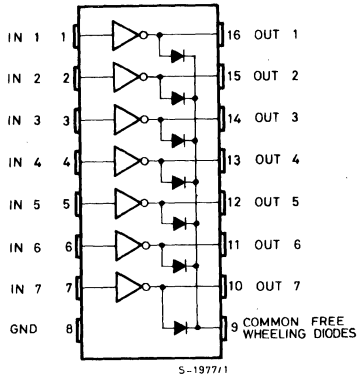
The four versions interface to all common logic families :

ULN2001A	General Purpose, DTL, TTL, PMOS, CMOS
ULN2002A	14-25 V PMOS
ULN2003A	5 V TTL, CMOS
ULN2004A	6–15 V CMOS, PMOS

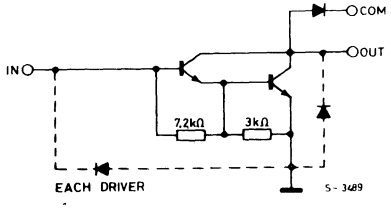
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULN2002A/D - 2003A/D - 2004A/D)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
T_j	Junction Temperature	150	°C

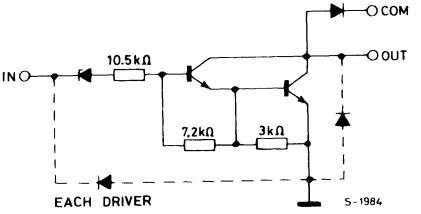
PIN CONNECTION



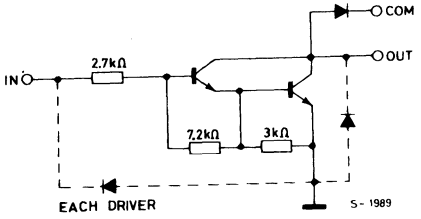
SCHEMATIC DIAGRAM



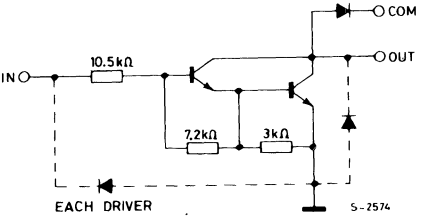
Series ULN-2001A
(each driver)



Series ULN-2002A
(each driver)



Series ULN-2003A
(each driver)



Series ULN-2004A
(each driver)

THERMAL DATA

			DIP–16	SO–16
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70 °C/W	165 °C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2002A** V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULN2004A** V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULN2002A** V_i = 17 V		0.82	1.25	mA	3
		for **ULN2003A** V_i = 3.85 V		0.93	1.35	mA	3
		for **ULN2004A** V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V		1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2002A**					
		V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULN2003A**					
		V_{CE} = 2 V I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V I_C = 300 mA			3	V	5
		for **ULN2004A**					
		V_{CE} = 2 V I_C = 125 mA			5	V	5
		V_{CE} = 2 V I_C = 200 mA			6	V	5
		V_{CE} = 2 V I_C = 275 mA			7	V	5
		V_{CE} = 2 V I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULN2001A** V_{CE} = 2 V I_C = 350 mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

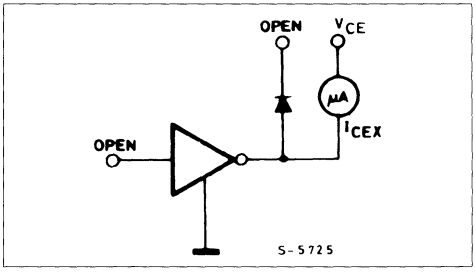


Figure 1b.

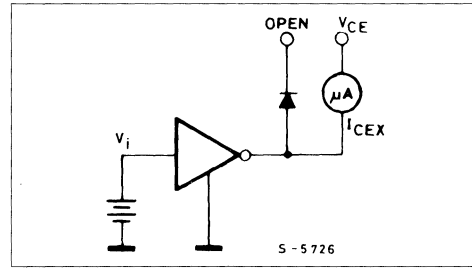


Figure 2.

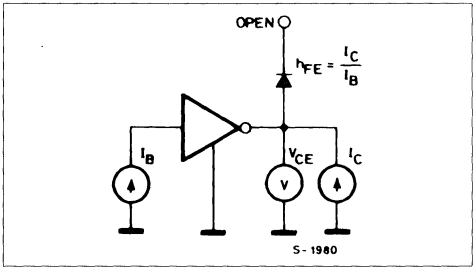


Figure 3.

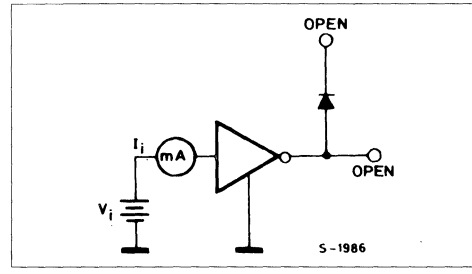


Figure 4.

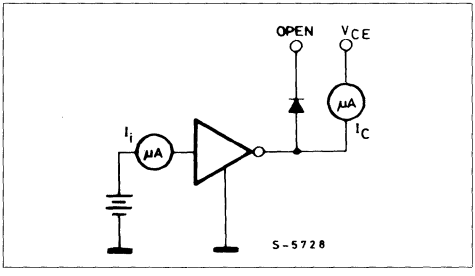


Figure 5.

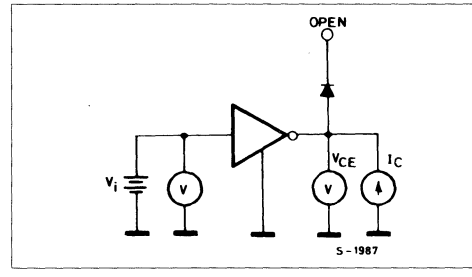


Figure 6.

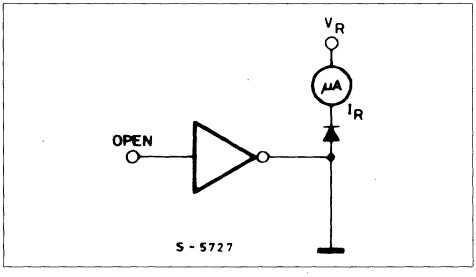
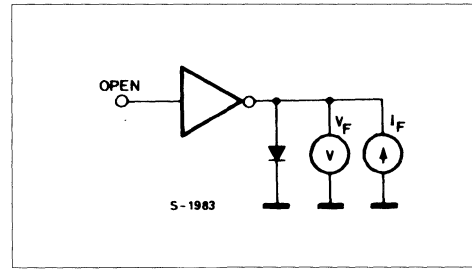


Figure 7.

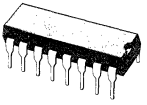


50 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 50 V
- SUSTAINING VOLTAGE AT LEAST 35 V
- INTEGRAL SUPPRESSION DIODES (ULN2064B, ULN2066B, ULN2068B and ULN2070B)
- ISOLATED DARLINGTON PINOUT (ULN2074B, ULN2076B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

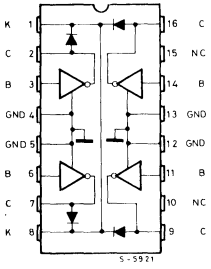
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 50 V and a sustaining voltage of 35 V measured at 100 mA. The ULN2064B, ULN2066B, ULN2068B and ULN2070B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B and ULN2076B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5 V logic families and the ULN2066B and ULN2076B are compatible with 6-15 V CMOS and PMOS. Types ULN2068B and ULN2070B include a predriver stage to reduce loading on the control logic.

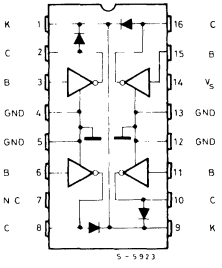


POWERDIP
12 + 2 + 2

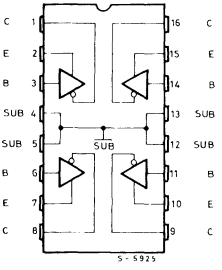
PIN CONNECTIONS (top view) and ORDER CODES



ULN2064B
ULN2068B



ULN2068B
ULN2070B

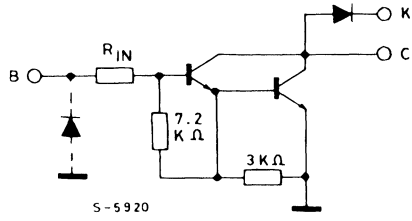


ULN2074B
ULN2076B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	50	V
$V_{CE(sus)}$	Output Sustaining Voltage	35	V
I_o	Output Current	1.75	A
V_i	Input Voltage for **ULN2066B/70B/74B/76B** for **ULN2064B/68B**	30 15	V V
I_i	Input Current	25	mA
V_s	Supply Voltage for **ULN2068B** for **ULN2070B**	10 20	V V
P_{tot}	Power Dissipation : at T_{amb} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



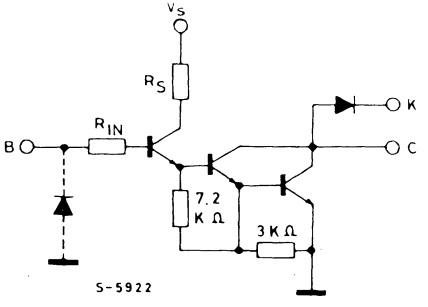
ULN2064B : R_{IN} = 35 Ω
ULN2066B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2064B – ULN2066B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2064B – ULN2066B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2064B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2064B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2066B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2066B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2064B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2066B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn – on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn – off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2064B – ULN2066B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B and ULN2076B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

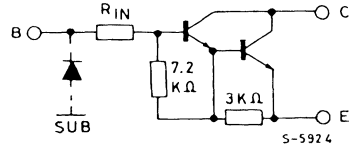


ULN2068B : R_{IN} = 2.5 kΩ R_s = 900 Ω
ULN2070B : R_{IN} = 11.6 kΩ R_s = 3.4 KHΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2068B, V_s = 12 V for ULN2070B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2068B – ULN2070B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2068B – ULN2070B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2068B**					
		I_C = 500 mA V_i = 2.75 V			1.1	V	
		I_C = 750 mA V_i = 2.75 V			1.2	V	
		I_C = 1 A V_i = 2.75 V			1.3	V	
		I_C = 1.25 A V_i = 2.75 V			1.4	V	
		for **ULN2070B**					2
		I_B = 500 mA V_i = 5 V			1.1	V	
		I_B = 750 mA V_i = 5 V			1.2	V	
		I_B = 1 A V_i = 5 V			1.3	V	
		I_B = 1.25 A V_i = 5 V			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2068B** V_i = 2.75 V			550	µA	
		for **ULN2068B** V_i = 3.75 V			1000	µA	
		for **ULN2070B** V_i = 5 V			400	µA	4
		for **ULN2070B** V_i = 12 V			1250	µA	
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					
		for **ULN2068B**			2.75	V	5
		for **ULN2070B**			5	V	
I_s	Supply Current	for **ULN2068B**					
		I_C = 500 mA V_i = 2.75 V			6	mA	
		for **ULN2070B**					8
		I_C = 500 mA V_i = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2068B – ULN2070B**					
		V_R = 50 V			50	µA	6
		V_R = 50 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2074B : R_{IN} = 350 Ω
ULN2076B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig
I_{CEX}	Output Leakage Current	for **ULN2074B – ULN2076B**					
		V_{CE} = 50 V			100	µA	1
		V_{CE} = 50 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2074B – ULN2076B** I_C = 100 mA V_i = 0.4 V	35			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
$I_{i(on)}$	Input Current	for **ULN2074B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2074B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2076B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2076B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2074B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2076B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

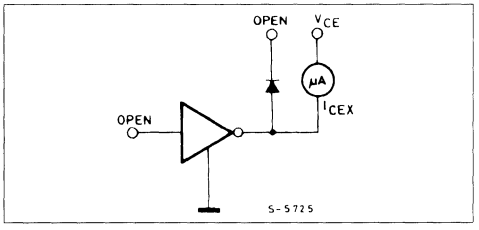


Figure 2.

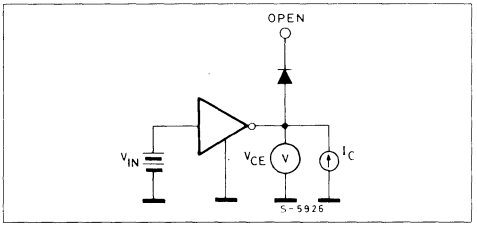


Figure 3.

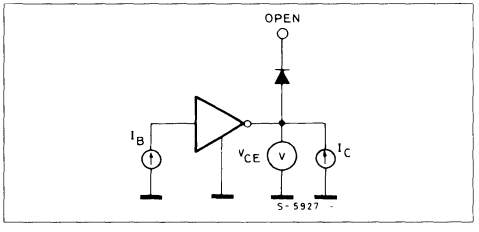


Figure 4.

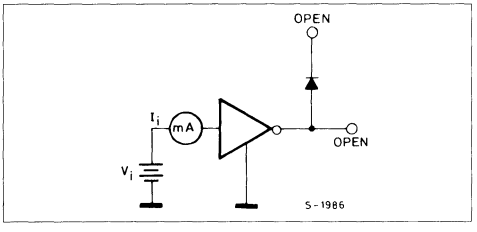


Figure 5.

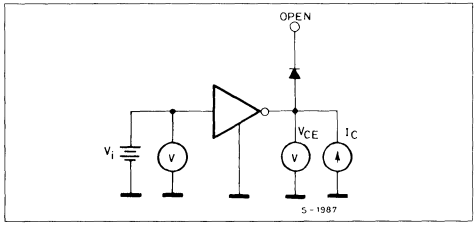


Figure 6.

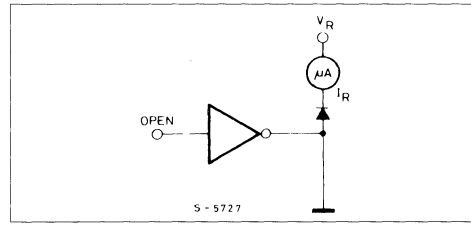


Figure 7.

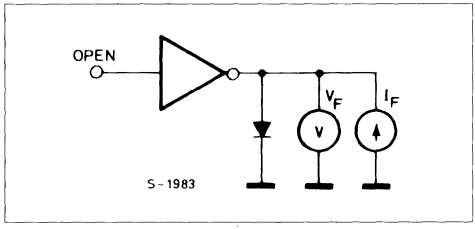


Figure 8.

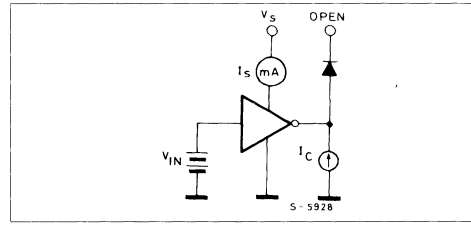


Figure 9 : Input Current as a Function of Input Voltage.

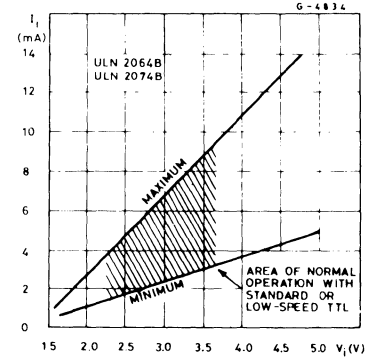


Figure 10 : Input Current as a Function of Input Voltage.

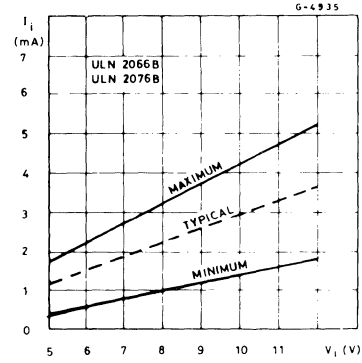
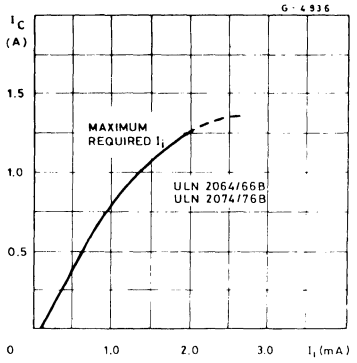


Figure 11 : Collector Current as a Function of Input Current.



TYPICAL APPLICATIONS

Figure 12 : Common-anode LED Drivers.

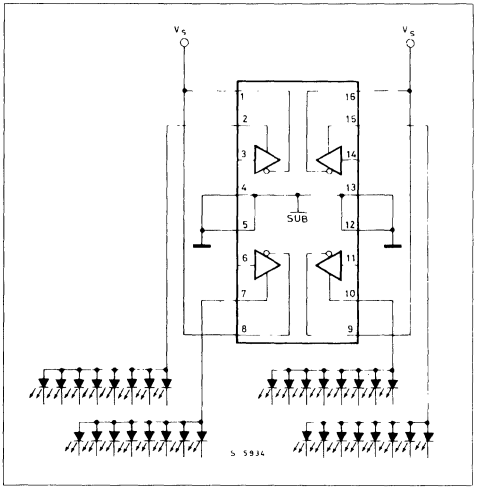
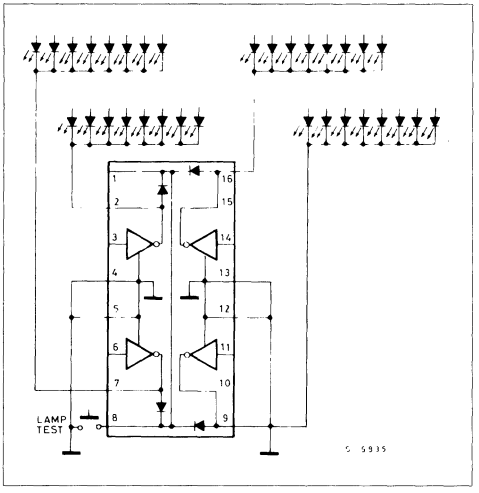


Figure 13 : Common-cathode LED Drivers.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 14) or to an external heatsink (Fig. 15).

The diagram of figure 16 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "α" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 14 : Example of P.C. Board Copper Area which is Used as Heatsink.

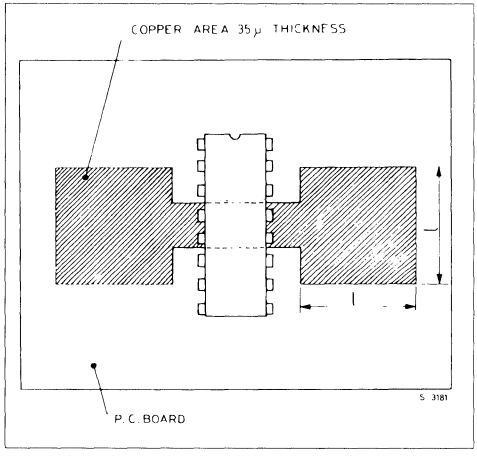


Figure 15 : External Heatsink Mounting Example.

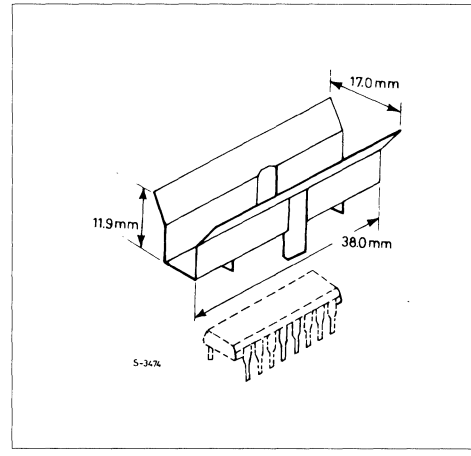


Figure 16 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "α".

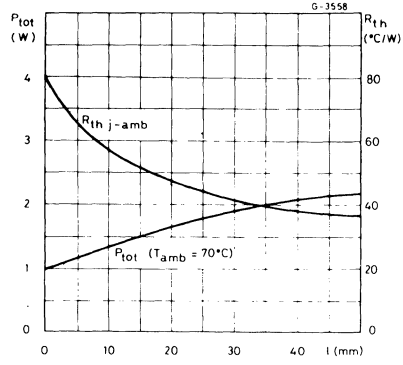
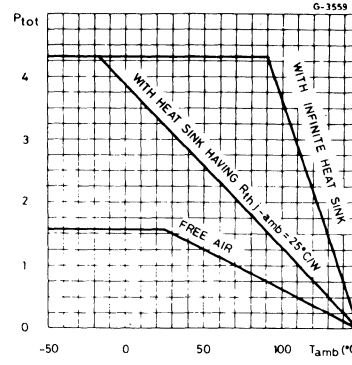


Figure 17 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

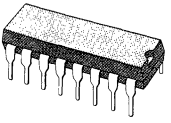


80 V - 1.5 A QUAD DARLINGTON SWITCHES

- OUTPUT CURRENT TO 1.5 A EACH DARLINGTON
- MINIMUM BREAKDOWN 80 V
- SUSTAINING VOLTAGE AT LEAST 50 V
- INTEGRAL SUPPRESSION DIODES (ULN2065B, ULN2067B, ULN2069B and ULN2071B)
- ISOLATED DARLINGTON PINOUT (ULN2075B and ULN2077B)
- VERSIONS COMPATIBLE WITH ALL POPULAR LOGIC FAMILIES

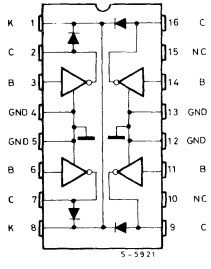
DESCRIPTION

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN darlington switches delivering up to 1.5 A with a specified minimum breakdown of 80 V and a sustaining voltage of 50 V. The ULN2065B, ULN2067B, ULN2069B and ULN2071B contain integral suppression diodes for inductive loads and have common emitters ; the ULN2075B and ULN2077B feature isolated darlington pinouts and are intended for applications such as emitter follower configurations. Inputs of the ULN2065B, ULN2069B and ULN2075B are compatible with popular 5 V logic families and the ULN2067B, ULN2071B and ULN2077B are compatible with 6-15 VCMOS and PMOS. The ULN2069B and ULN2071B include a predriver stage to provide extragain, reducing the load on control logic.

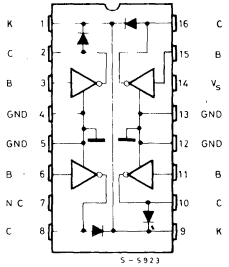


POWERDIP
12 + 2 + 2

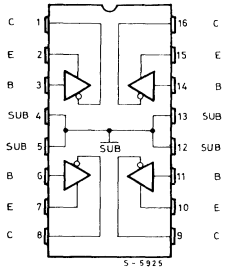
PIN CONNECTIONS AND ORDER CODES



ULN2065B
ULN2067B



ULN2069B
ULN2071B

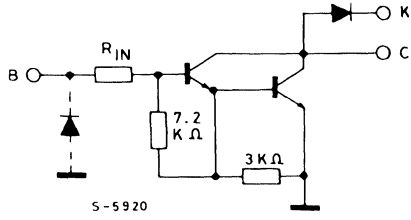


ULN2075B
ULN2077B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CEX}	Output Voltage	80	V
$V_{CE(sus)}$	Output Sustaining Voltage	50	V
I_O	Output Current	1.75	A
V_i	Input Voltage for **ULN2075B – 2077B**	60	V
	for **ULN2067B – 2071B**	30	V
	for **ULN2065B – 2069B**	15	V
I_I	Input Current	25	mA
V_S	Supply Voltage for **ULN2069B**	10	V
	for **ULN2071B**	20	V
P_{tot}	Power Dissipation : at T_{pins} = 90 °C	4.3	W
	at T_{amb} = 70 °C	1	W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

SCHEMATIC DIAGRAM



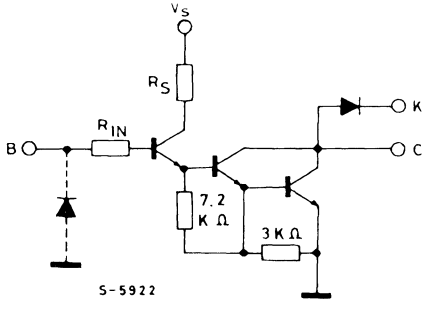
ULN2065B : R_{IN} = 350 Ω
ULN2067B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2065B – ULN2067B**						
		V_{CE} = 80 V				100	µA	1
		V_{CE} = 80 V	T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2065B – ULN2067B**						
		I_C = 100 mA	V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA	I_B = 625 µA			1.1	V	3
		I_C = 750 mA	I_B = 935 µA			1.2	V	
		I_C = 1 A	I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A	I_B = 2 mA			1.4	V	
		for **ULN2065B – ULN2067B**						
		I_C = 1.5 A	I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2065B**	V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2065B**	V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2067B**	V_i = 5 V	0.6		1.8	mA	
		for **ULN2067B**	V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2065B**						5
		V_{CE} = 2 V	I_C = 1 A			2	V	
		V_{CE} = 2 V	I_C = 1.5 A			2.5	V	
		for **ULN2067B**						
		V_{CE} = 2 V	I_C = 1 A			6.5	V	
		V_{CE} = 2 V	I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o				1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o				1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2065B – ULN2067B**						6
		V_R = 80 V				50	µA	
		V_R = 80 V	T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A				1.75	V	7
		I_F = 1.5 A				2	V	

Notes : 1. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2075B and ULN2077B reference is ground for all other types.
2. Input current may be limited by maximum allowable input voltage.

SCHEMATIC DIAGRAM

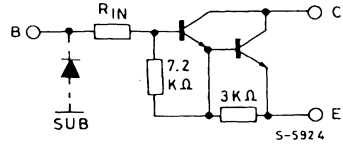


ULN2069B : R_{IN} = 2.5 KΩ, R_s = 900 Ω
ULN2071B : R_{IN} = 11.6 KΩ, R_s = 3.4 KΩ

ELECTRICAL CHARACTERISTICS (V_s = 5 V for ULN2069B, V_s = 12 V for ULN2071B, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2069B – ULN2071B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2069B – ULN2071B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	for **ULN2069B**					2
		I_C = 500 mA V_i = 2.75 V			1.1	V	
		I_C = 750 mA V_i = 2.75 V			1.2	V	
		I_C = 1 A V_i = 2.75 V			1.3	V	
		I_C = 1.25 A V_i = 2.75 V			1.4	V	
		I_C = 1.5 A V_i = 2.75 V			1.5	V	
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			1.1	V	
		I_C = 750 mA V_i = 5 V			1.2	V	
		I_C = 1 A V_i = 5 V			1.3	V	
		I_C = 1.25 A V_i = 5 V			1.4	V	
		I_C = 1.5 A V_i = 5 V			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2069B** V_i = 2.75 V			550	µA	4
		for **ULN2069B** V_i = 3.75 V			1000	µA	
		for **ULN2071B** V_i = 5 V			400	µA	
		for **ULN2071B** V_i = 12 V			1250	µA	
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V I_C = 1.5 A					5
		for **ULN2069B**			2.75	V	
		for **ULN2071B**			5		
I_s	Supply Current	for **ULN2069B**					8
		I_C = 500 mA V_i = 2.75 V			6	mA	
		for **ULN2071B**					
		I_C = 500 mA V_i = 5 V			4.5	mA	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o I_C = 1.25 A			1.5	µs	
I_R	Clamp Diode Leakage Current	for **ULN2069B – ULN2071B**					6
		V_R = 80 V			50	µA	
		V_R = 80 V T_{amb} = 70 °C			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 1 A			1.75	V	7
		I_F = 1.5 A			2	V	

SCHEMATIC DIAGRAM



ULN2075B : R_{IN} = 350 Ω
ULN2077B : R_{IN} = 3 kΩ

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	for **ULN2075B – ULN2077B**					
		V_{CE} = 80 V			100	µA	1
		V_{CE} = 80 V T_{amb} = 70 °C			500	µA	
$V_{CE(sus)}$	Collector-emitter Sustaining Voltage	for **ULN2075B – ULN2077B** I_C = 100 mA V_i = 0.4 V	50			V	2
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 500 mA I_B = 625 µA			1.1	V	3
		I_C = 750 mA I_B = 935 µA			1.2	V	
		I_C = 1 A I_B = 1.25 mA			1.3	V	
		I_C = 1.25 A I_B = 2 mA			1.4	V	
		for **ULN2075B – ULN2077B**					
		I_C = 1.5 A I_B = 2.25 mA			1.5	V	
$I_{i(on)}$	Input Current	for **ULN2075B** V_i = 2.4 V	1.4		4.3	mA	4
		for **ULN2075B** V_i = 3.75 V	3.3		9.6	mA	
		for **ULN2077B** V_i = 5 V	0.6		1.8	mA	
		for **ULN2077B** V_i = 12 V	1.7		5.2	mA	
$V_{i(on)}$	Input Voltage	for **ULN2075B**					5
		V_{CE} = 2 V I_C = 1 A			2	V	
		V_{CE} = 2 V I_C = 1.5 A			2.5	V	
		for **ULN2077B**					
		V_{CE} = 2 V I_C = 1 A			6.5	V	
		V_{CE} = 2 V I_C = 1.5 A			10	V	
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o			1	µs	
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o			1.5	µs	

TEST CIRCUITS

Figure 1.

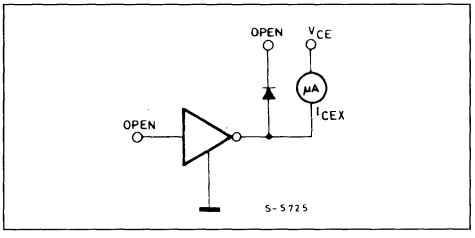


Figure 2.

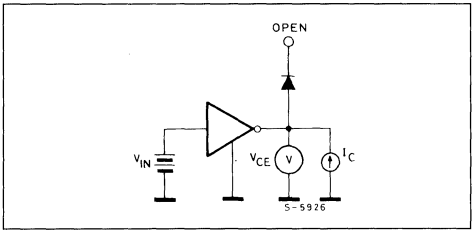


Figure 3.

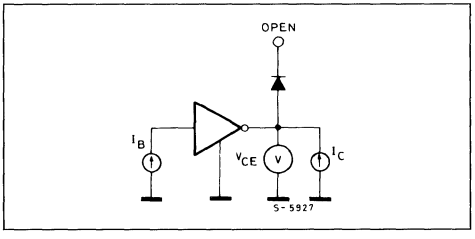


Figure 4.

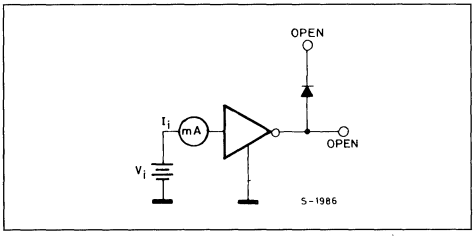


Figure 5.

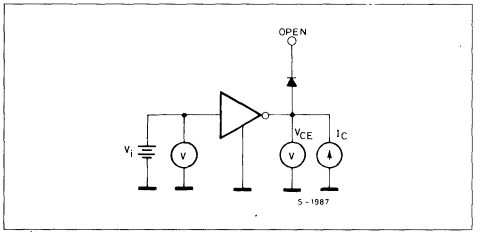


Figure 6.

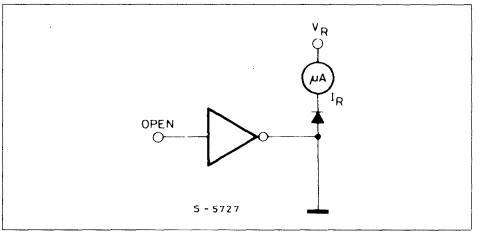


Figure 7.

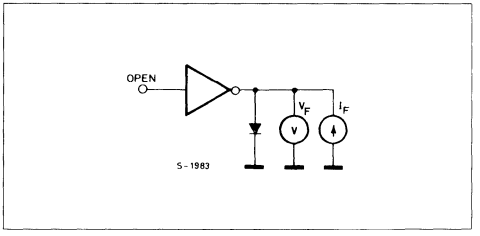


Figure 8.

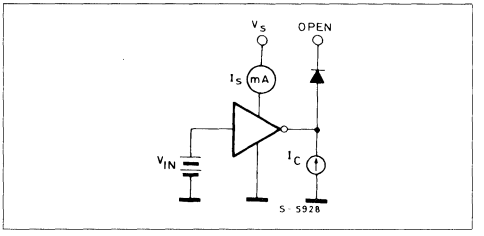


Figure 9 : Input Current as a Function of Input Voltage.

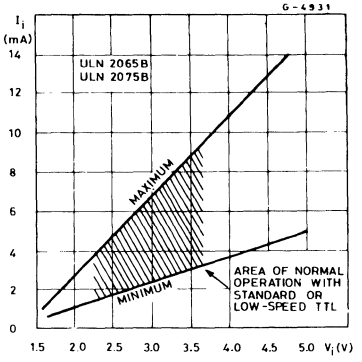


Figure 10 : Input Current as a Function of Input Voltage.

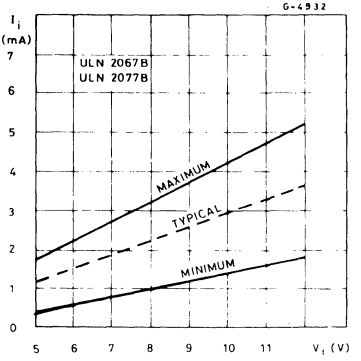
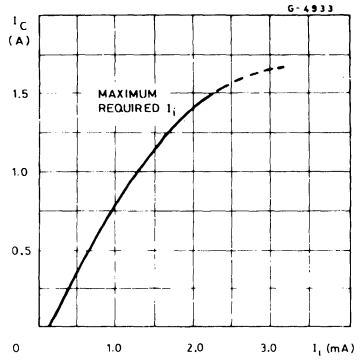


Figure 11 : Collector Current as a Function of Input Current.



MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 12) or to an external heatsink (Fig. 13).

The diagram of figure 14 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35 µ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 12 : Example of P.C. Board Area which is Used as Heatsink.

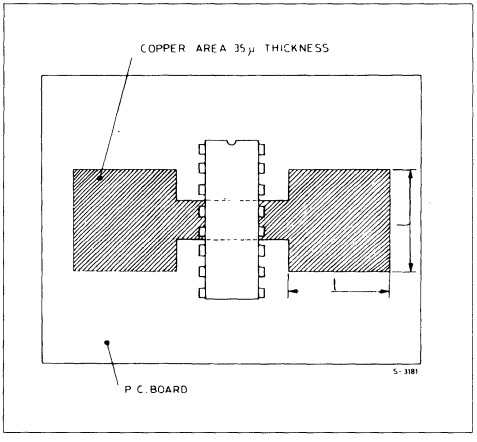


Figure 13 : External Heatsink Mounting Example.

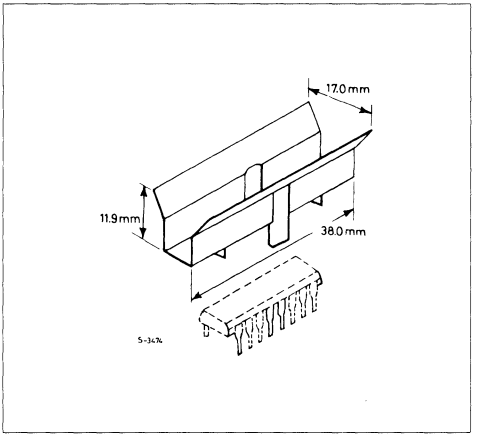


Figure 14 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

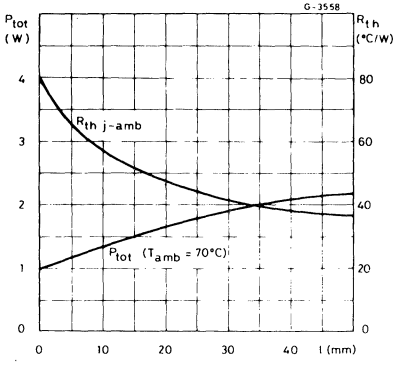
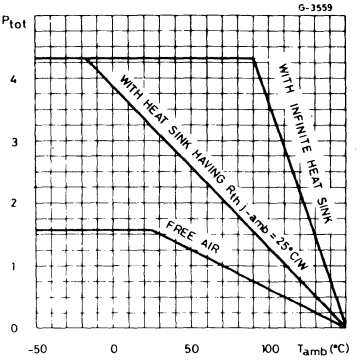


Figure 15 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



EIGHT DARLINGTON ARRAYS

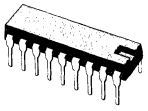
- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT

DESCRIPTION

The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

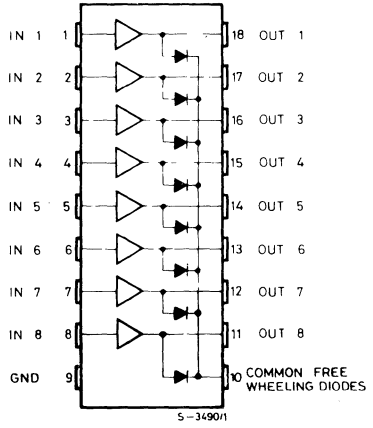
Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor ; the ULN2802A has a 10.5 KΩ input resistor and zener for 14-25 V PMOS ; the ULN2803A has a 2.7 KΩ input resistor for 5 V TTL and CMOS ; the ULN2804A has a 10.5 KΩ input resistor for 6-15 V CMOS and the ULN2805A is designed to sink a minimum of 350 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout.



DIP-18
(Plastic)

CONNECTION DIAGRAM (top view)

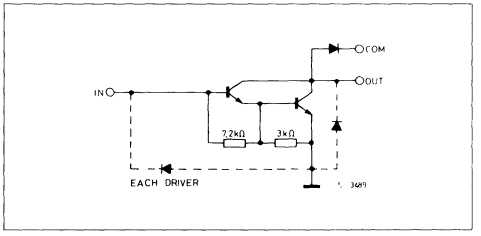


ABSOLUTE MAXIMUM RATINGS

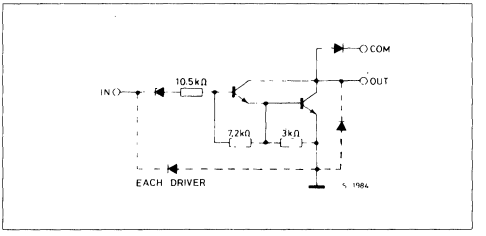
Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULN2802A, 2803A, 2804A for ULN2805A	30 15	V V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

SCHEMATIC DIAGRAM AND ORDER CODES

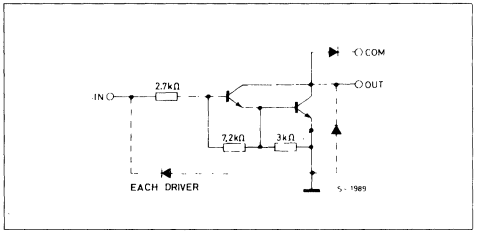
For ULN2801A (each driver for PMOS-CMOS)



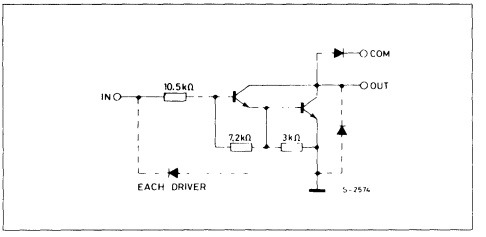
For ULN2802A (each driver for 14-15 V PMOS)



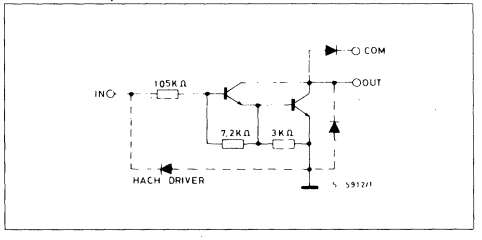
For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS



For ULN2805A (each driver for high out TTL)



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULN2802A** V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULN2804A** V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	
$I_{i(on)}$	Input Current	for **ULN2802A** V_i = 17 V		0.82	1.25	mA	3
		for **ULN2803A** V_i = 3.85 V		0.93	1.35	mA	
		for **ULN2804A** V_i = 5 V		0.35	0.5	mA	
		V_i = 12 V		1	1.45	mA	
		for **ULN2805A** V_i = 3 V		1.5	2.4	mA	
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	for **ULN2802A** V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULN2803A** V_{CE} = 2 V I_C = 200 mA			2.4	V	
		V_{CE} = 2 V I_C = 250 mA			2.7	V	
		V_{CE} = 2 V I_C = 300 mA			3	V	
		for **ULN2804A** V_{CE} = 2 V I_C = 125 mA			5	V	
		V_{CE} = 2 V I_C = 200 mA			6	V	
		V_{CE} = 2 V I_C = 275 mA			7	V	
		V_{CE} = 2 V I_C = 350 mA			8	V	
		for **ULN2805A** V_{CE} = 2 V I_C = 350 mA			2.4	V	
h_{FE}	DC Forward Current Gain	for **ULN2801A** V_{CE} = 2 V I_C = 350 mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

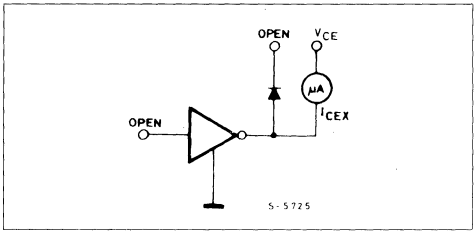


Figure 1b.

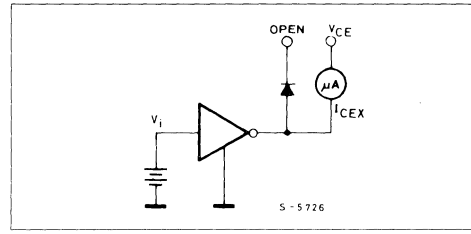


Figure 2.

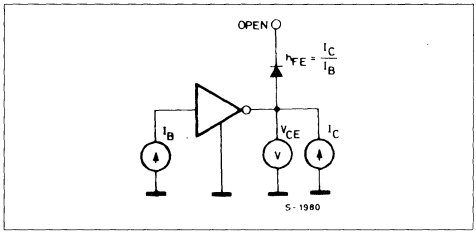


Figure 3.

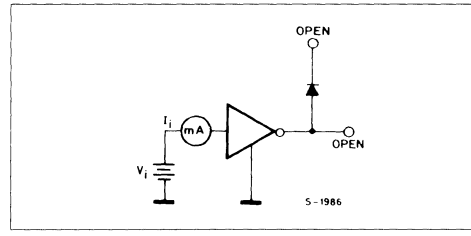


Figure 4.

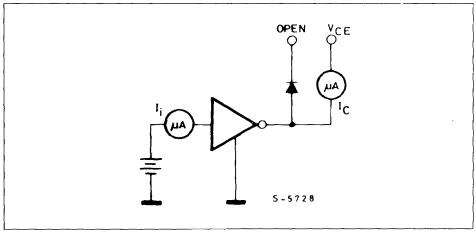


Figure 5.

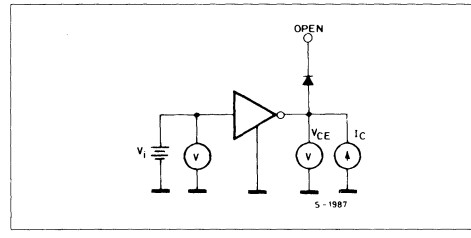


Figure 6.

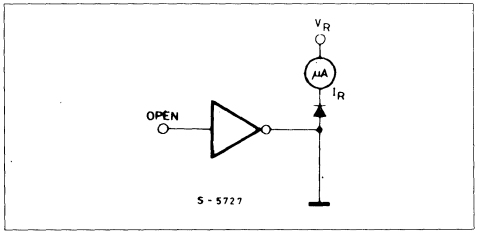


Figure 7.

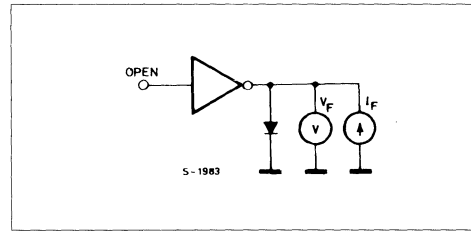


Figure 8 : Collector Current as a Function of Saturation Voltage.

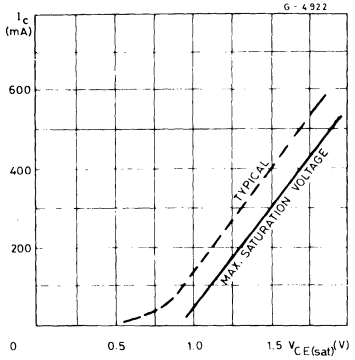


Figure 9 : Collector Current as a Function of Input Current.

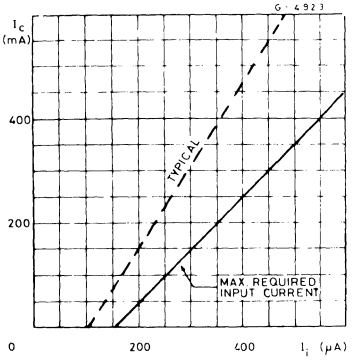


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

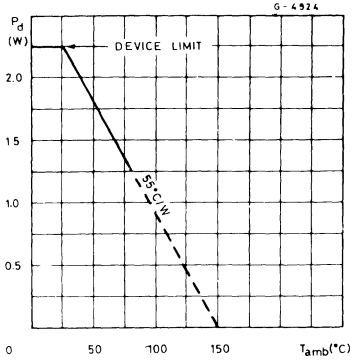


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

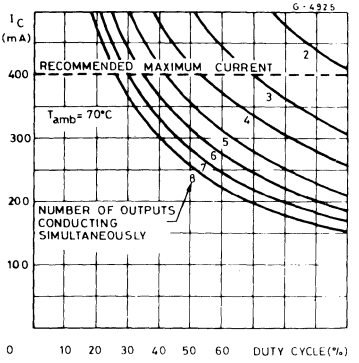


Figure 12 : Peak Collector Current as a Function of Duty.

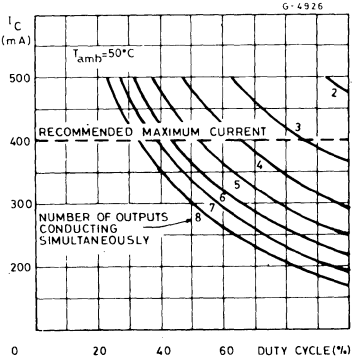


Figure 13 : Input Current as a Function of Input Voltage (for ULN2802A).

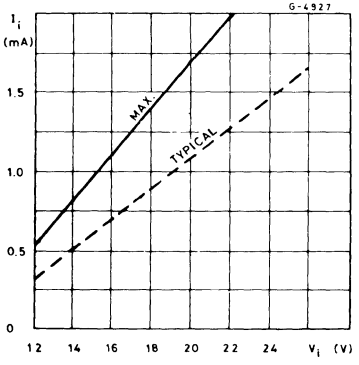


Figure 14 : Input Current as a Function of Input Voltage (for ULN2804A)

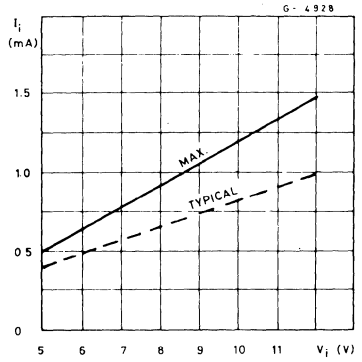


Figure 15 : Input Current as a Function of Input Voltage (for ULN2803A)

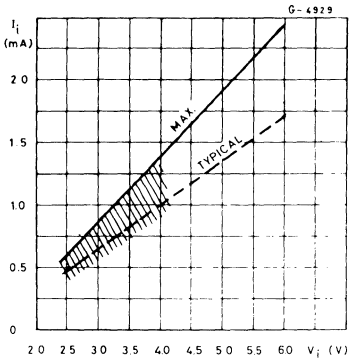
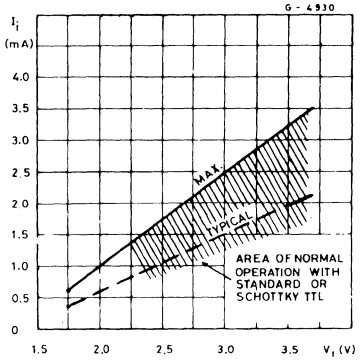


Figure 16 : Input Current as a Function of Input Voltage (for ULN2805A)

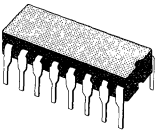


SGS-THOMSON MICROELECTRONICS

ULQ2001R/2R ULQ2003R/4R

SEVEN DARLINGTON ARRAYS

- SEVEN DARLINGTONS PER PACKAGE
- OUTPUT CURRENT 500 mA PER DRIVER (600 mA PEAK)
- OUTPUT VOLTAGE 50 V
- INTEGRAL SUPPRESSION DIODES FOR INDUCTIVE LOADS
- OUTPUT CAN BE PARRALLELED FOR HIGHER CURRENT
- TTL/CMOS/PMOS/DTL COMPATIBLE INPUTS
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY LAYOUT



DIP-16 Ceramic

DESCRIPTION

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ2004R are high voltage, high current darlington arrays each containing seven open collector darlington pairs with common emitters. Each channel is rated at 500 mA and can withstand peak currents of 600 mA. Suppression diodes are included for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

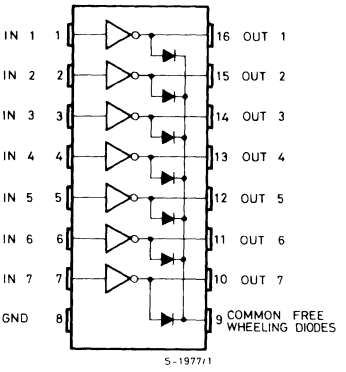
The four versions interface to all common families.

ULQ2001R	General Purpose, DTL, TTL, CMOS
ULQ2002R	15-25 V PMOS
ULQ2003R	5 V TTL, CMOS
ULQ2004R	6-15 V CMOS, PMOS

These versatile devices are useful for driving a wide range of loads including solenoids, relays DC motors, LED displays, filament lamps, thermal printheads and high power buffers.

The ULQ2001R, ULQ2002R, ULQ2003R and ULQ 2004R are supplied in 16 pin ceramic DIP packages.

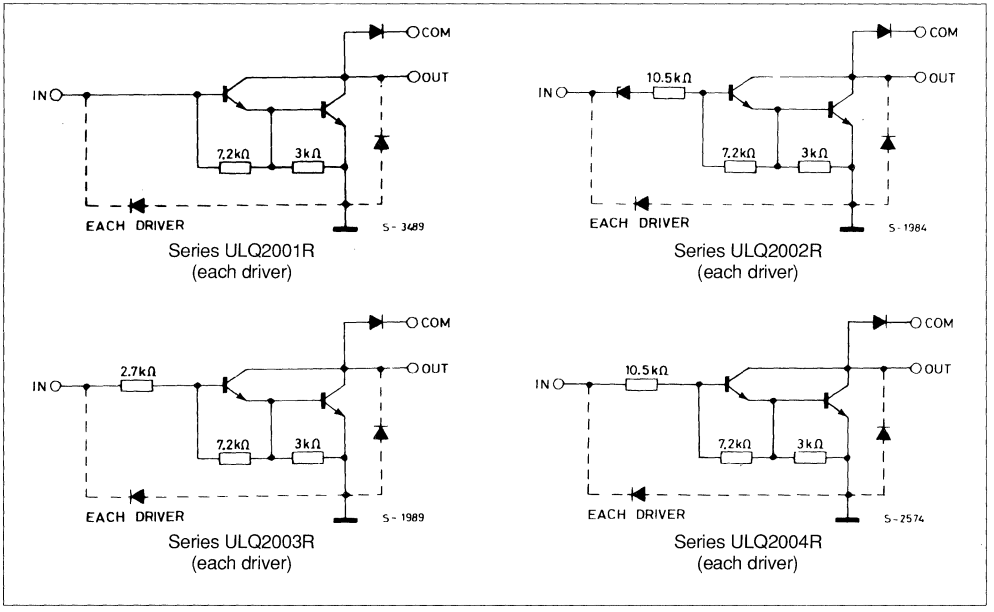
PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_{in}	Input Voltage (for ULQ2002R/2003R/2004R)	30	V
I_c	Continuous Collector Current	500	mA
I_b	Continuous Base Current	25	mA
T_{amb}	Operating Ambient Temperature Range	− 20 to + 85	°C
T_{stg}	Storage Temperature Range	− 55 to 150	°C

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25° C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50 V			50	µA	1a
		T_{amb} = 70 °C V_{CE} = 50 V			100	µA	1a
		T_{amb} = 70 °C for **ULQ2002R** V_{CE} = 50 V V_i = 6 V			500	µA	1b
		for **ULQ2004R** V_{CE} = 50 V V_i = 1 V			500	µA	1b
$V_{CE\ (sat)}$	Collector-emitter Saturation Voltage	I_C = 100 mA I_B = 250 µA		0.9	1.1	V	2
		I_C = 200 mA I_B = 350 µA		1.1	1.3	V	2
		I_C = 350 mA I_B = 500 µA		1.3	1.6	V	2
$I_{i(on)}$	Input Current	for **ULQ2002R** V_i = 17 V		0.82	1.25	mA	3
		for **ULQ2003R** V_i = 3.85 V		0.93	1.35	mA	3
		for **ULQ2004R** V_i = 5 V		0.35	0.5	mA	3
		V_i = 12 V		1	1.45	mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70 °C I_C = 500 µA	50	65		µA	4
$Vi_{(on)}$	Input Voltage	for **ULQ2002R** V_{CE} = 2 V I_C = 300 mA			13	V	5
		for **ULQ2003R** V_{CE} = 2 V I_C = 200 mA			2.4	V	5
		V_{CE} = 2 V I_C = 250 mA			2.7	V	5
		V_{CE} = 2 V I_C = 300 mA			3	V	5
		for **ULQ2004R** V_{CE} = 2 V I_C = 125 mA			5	V	
		V_{CE} = 2 V I_C = 200 mA			6	V	5
		V_{CE} = 2 V I_C = 275 mA			7	V	5
		V_{CE} = 2 V I_C = 350 mA			8	V	5
h_{FE}	DC Forward Current Gain	for **ULQ2001R** V_{CE} = 2 V I_C = 350 mA	1000			-	2
C_i	Input Capacitance			15	25	pF	-
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	-
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	-
I_R	Clamp Diode Leakage Current	V_R = 50 V			50	µA	6
		T_{amb} = 70 °C V_R = 50 V			100	µA	6
V_F	Clamp Diode Forward Voltage	I_F = 350 mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

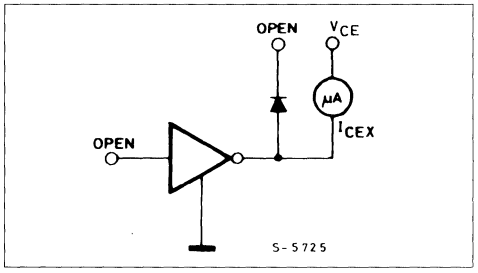


Figure 1b.

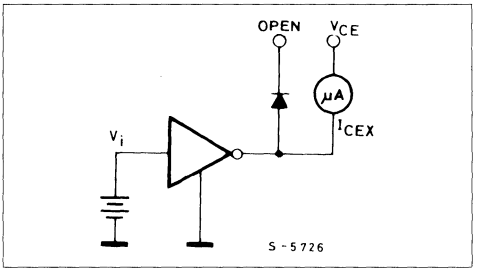


Figure 2.

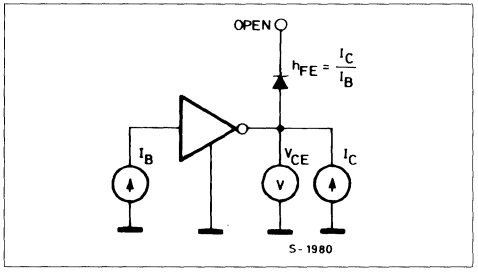


Figure 3.

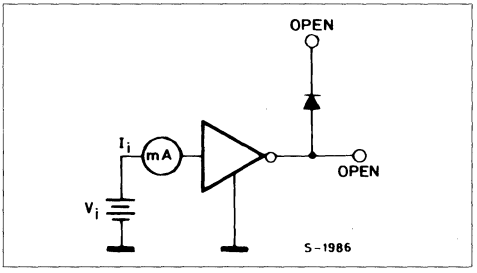


Figure 4.

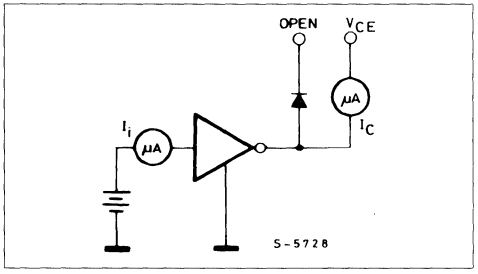


Figure 5.

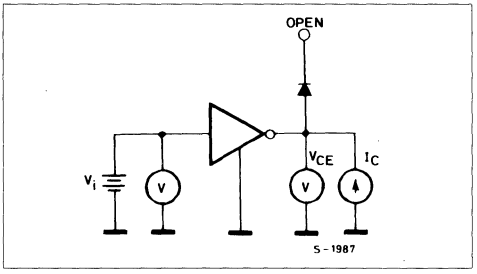


Figure 6.

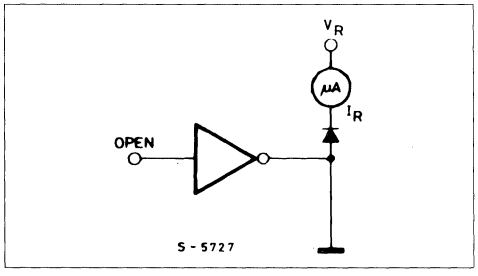
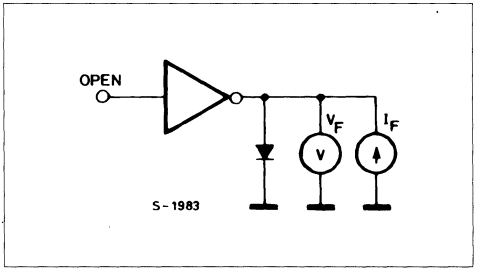


Figure 7.



SGS-THOMSON MICROELECTRONICS

VB100

HIGH VOLTAGE DUTY CYCLE CONTROLLER

ADVANCE DATA

- INTEGRATED 450V POWER DARLINGTON
- OUTPUT CURRENT UP TO 5A
- HIGH IMPEDANCE DIFFERENTIAL INPUTS
- PROGRAMMABLE DRIVER CURRENT
- DUTY CYCLE CONTROL LINEARITY WITHIN 1.5%
- SWITCHING FREQUENCY UP TO 100 kHz
- THERMAL PROTECTION
- INTEGRATED PROTECTION AT COMPARATOR INPUTS
- MINIMUM EXTERNAL COMPONENT COUNT

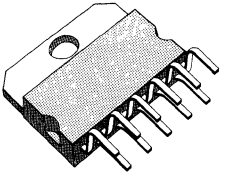
The VB100 is a monolithic integrated circuit which acts as a fully independent duty cycle controller with high voltage, high current open collector darlington output.

It is made using the innovative VI Power M1 technology merging a high voltage vertical discrete Darlington transistor together with bipolar control circuitry.

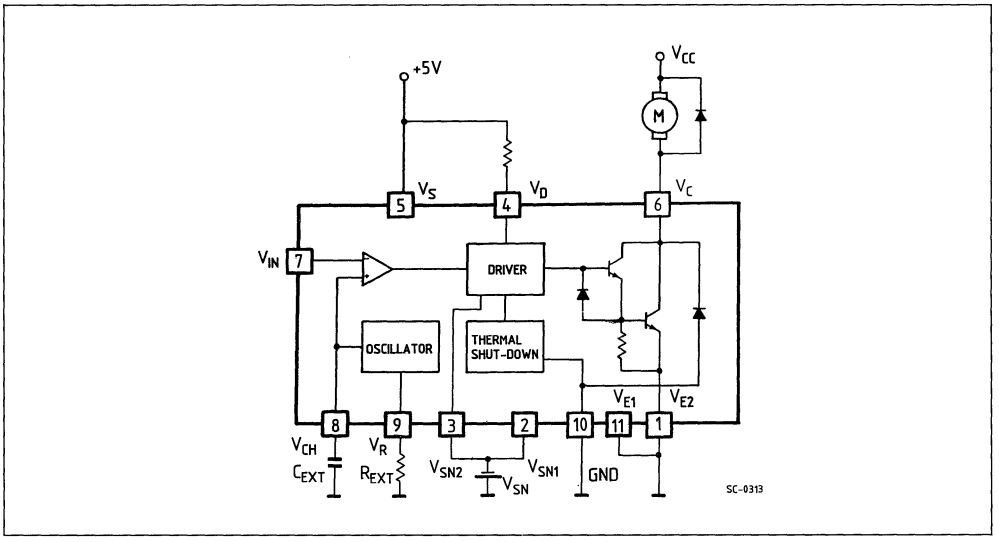
The VB100 is mainly intended as a D.C. motor and high voltage inductive load driver. It is able to adjust the output voltage duty cycle as a function of the input control voltage, at a switching frequency set by an internal stable sawtooh generator.

Built in thermal shut down switches off the power Darlington whenever the junction temperature exceeds an internally set value, typically 150°C with a 5V supply.

MULTIWATT-11



TEST AND APPLICATION CIRCUIT



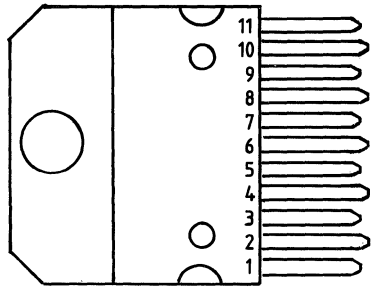
ABSOLUTE MAXIMUM RATINGS

V_{CE}	Power Darlington collector voltage	450	V
I_C	Power Darlington collector current	8	A
V_D	Driver stage supply voltage	15	V
V_S	Control stage supply voltage	15	V
I_D	Driver stage current	350	mA
V_{IN},V_{NI}	Comparator input voltage	V_S to −10	V
P_{tot}	Power dissipation	internally limited	
T_{op}	Junction operating temperature	−45 to 150	°C
T_{stg}	Storage temperature	−55 to 150	°C

THERMAL DATA

$R_{thj\text{ - case}}$	Thermal resistance junction-case	max	3.0	°C/W

CONNECTION DIAGRAM (Top view)



TAB CONNECTED TO PIN 6

PC-0290

PIN FUNCTION

N°	NAME	FUNCTION
1	V_{E1} High voltage Darlington emitter	Output stage ground n.1. It must be short circuited with V_{E2}; if no current sensing is used, a filtering capacitor must be provided between this pin and the high voltage supply. If current sensing is required, a shunt resistor can be connected between pin V_{E1} and V_{E2} and power ground and the filtering capacitor must be connected between ground and high voltage supply.
2	V_{SN1} Signal negative supply voltage	This pin is connected to the PWM ground and to the control circuit substrate. Supply range is from 0 to $-5V$. The applied negative supply voltage must be the most negative voltage of the device and must be the same voltage of pin V_{SN2}.
3	V_{SN2} High current negative supply voltage	This pin is connected to the driver ground. Supply range is from 0 to $-5V$. An applied negative supply, speeds-up the output Darlington.
4	V_D Driver stage supply voltage	This pin supplies the base current for the darlington driver during t_{ON} (output darlington on-time) $I_{D\,(on)} = (V_S - V_{D\,(sat)})/R_D$.
5	V_S Control circuit power supply	Supply voltage input. Being the internal reference voltage taken from V_S a 5V $\pm 5\%$ D.C. supply is required.
6	V_C High voltage output collector	This pin is internally connected to package header. It is the high voltage open collector output.
7	V_{IN} Inverting input	Input of the PWM comparator. A D.C. value between V_{CHL} and V_{CHH} sets the output duty cycle from minimum to maximum value.
8	V_{CH} Non inverting input	Non inverting input of the PWM comparator and external capacitance pin. The capacitance C_{EXT} (togheter with R_{EXT}) fixes the sawtooth generator frequency (f_{osc}). A low leakage capacitance is necessary for a linear operation. The relationship between frequency and C_{EXT} R_{EXT} is: $f_{osc} \simeq 1.1/(R_{EXT} \times C_{EXT})$
9	V_R Biasing Resistor	It fixes the current I_{ch} of the current generator which changes according to the following relation: $I_{ch} = 0.56 \times V_S/R_{EXT}$
10	GND Analog ground	It is the control circuit ground: for a reliable circuit operation only few millivolt drop ($< 10mV$) are allowed between this pin and C_{EXT}, R_{EXT} common point.
11	V_{E2} High voltage darlington emitter	Output stage ground n 2. It must be short circuited with V_{E1}; if no current sensing is used, a filtering capacitor must be provided between this pin and the high voltage supply. If current sensing is required, a shunt resistor can be connected between pins V_{E1} and V_{E2} and power ground and a filtering capacitor must be connected between power ground and high voltage supply.

ELECTRICAL CHARACTERISTICS: V_S = 5V; V_{CC} = 300V; V_A = 2V; V_B = 0V; R_{IN} = 10kΩ; R_{EXT} = 50KΩ; R_{CC} = 88Ω; R_D = 330Ω; R_{CH} = 100Ω; T_C = T_{case} = 25°C
See fig. 1. - unless otherwise specified.

Parameters		Test Conditions	Min.	Typ.	Max.	Unit
V_{CE}	Voltage between pins 6 and 1		450			V
$I_{C\ (leak)}$	High voltage collector leakage current	V_{CC} = 350 V			1	mA
$V_{CE\ (sat)}$	Saturation voltage of the output Darlington (between pins 6 and 1)	V_B = 2 V; V_A = 0 I_C = 3 A; I_D = 150 mA I_C = 5 A; I_D = 250 mA		2.5 2.7	2.9 3.3	V V
$V_{D\ (sat)}$	Saturation voltage between pins 4 and 1	V_B = 2 V; V_A = 0 I_D = 50 mA; I_C = 2A		2.8	3.5	V
V_S	Control circuit power supply		4.75	5.0	5.25	V
$I_{S\ off}$	Control circuit current		20	30	45	mA
$I_{S\ on}$	Control circut current	V_B = 2 V; V_A = 0	2.5	6	10	mA
V_{inTHH}	PWM comparator high threshold	V_B = 2 V; V_C = 50 V T_C = −40 to 130°C V_A = 0 → 3 V ⎍ (see fig. 2)	0		120	mV
V_{inTHL}	PWM comparator low threshold	V_B = 2 V; V_C = 50 V T_C = −40 to 130°C V_A = 3 V → 0 ⎎ (see fig. 2)	100		260	mV
$V_{inTH(hyst.)}$	PWM comparator hysteresis	V_B = 2 V; V_C = 50 V T_C = −40 to 130°C (see fig. 2)	50		250	mV
I_{IN}	PWM comparator input bias current	V_B = 2 V; V_C = 0.3 V T_C = −40 to 130°C		1	10	μA
V_{CHH}	High level threshold sawtooth generator	V_A = 0 V → 3.2 V ⎍; V_B = 0.3 V	2.45	2.55	2.8	V
V_{CHL}	Low level threshold sawtooth generator	V_A = 3.2 V → 0 V ⎎	0.4	0.5	0.7	V
$\frac{I_{CH} - I_R}{I_R}$	External capacitor charging current, pin 8 versus I_R, pin 9	I_R = 50 to 110 μA V_A = 1 V; V_B = 0.3 V	−7		+7	%

ELECTRICAL CHARACTERISTICS:

Parameters		Test Conditions		Min.	Typ.	Max.	Unit
$\frac{I_{CH}^*}{T} \times \frac{1}{I_{CH}}$	Capacitor charging current change with temperature (pin 8)	V_A = 1 V I_R = 100 µA	V_B = 0.3 V T_C = −40 to 130°C			300	ppm/°C
V_R	Reference bias voltage pin 11	I_R = 100 µA		2.7	2.8	2.92	V
t_r	Rise time of the Darlington collector current, I_C (see fig. 3)	I_D = 150 mA	I_C = 3 A		0.25		µs
t_s	Storage time of the Darlington collector current, I_C (see fig. 3)	I_C = 3 A V_{SN} = −5 V V_{SN} = 0 V	I_D = 150 mA		 1.5 8.0		 µs µs
t_f	Fall time of the Darlington collector current, I_C (see fig. 3)	I_C = 3 A V_{SN} = −5 V V_{SN} = 0 V	I_D = 150 mA		 0.2 1.0		 µs µs
$t_{ON\ (min)}$	Minimum duration of the Darlington collector current, I_C (see fig. 3)	I_C = 3 A V_{SN} = −5 V V_{SN} = 0 V	I_D = 150 mA		 2.0 10.0		 µs µs

$I_{CH}^* = I_{CH}$ (130°C) − I_{CH} (−40°C)
N.B.* pulsed operation: $t_{rep.}$ = 10 ms t_{ON} = 100 µs

Fig. 1 Test Circuit

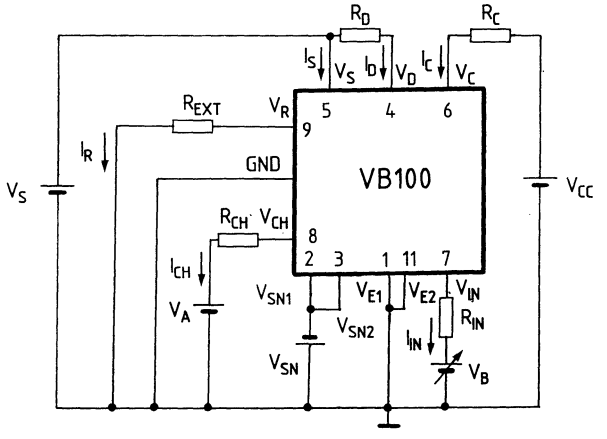


Fig. 2 Comparator threshold hysteresis

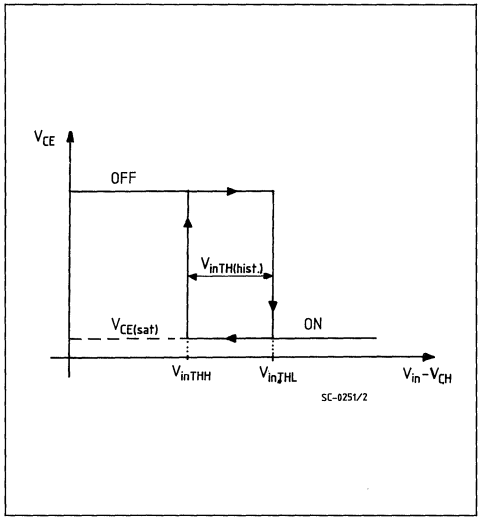


Fig. 3 Switching waveforms

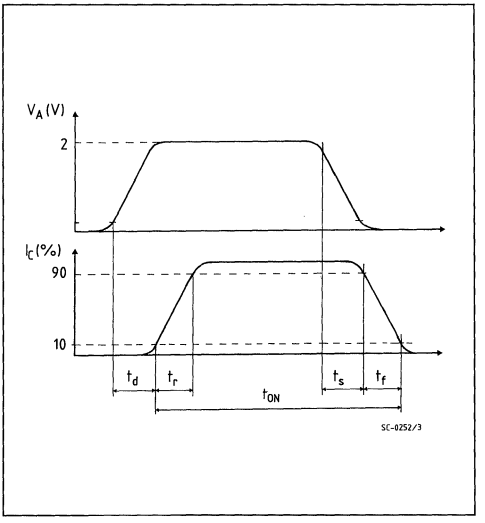
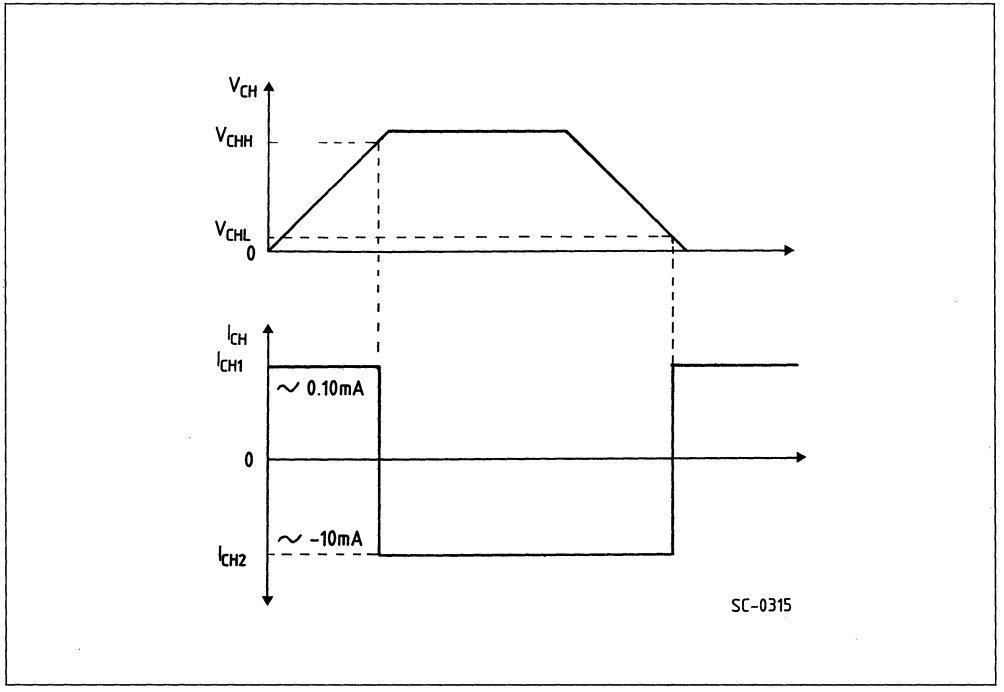


Fig. 4 Switching waveforms



APPLICATION INFORMATION

The VB100 is mainly intended as a quarter bridge controller. The sawtooth generator frequency is set by two external components, $R_{EXT.}$ and $C_{EXT.}$:

$$f_{osc} = 1.1/(R_{EXT.} \times C_{EXT.})$$

in the ranges:

$23.3\ k\Omega < R_{EXT.} < 100\ k\Omega$
$400pF < C_{EXT.} < 200\ \mu F$
$0.5\ Hz < f_{osc.} < 100kHz$

The input voltage V_{IN} sets the duration of t_{ON} for the output stage. As V_{IN} increases t_{ON} increases following the relationship:

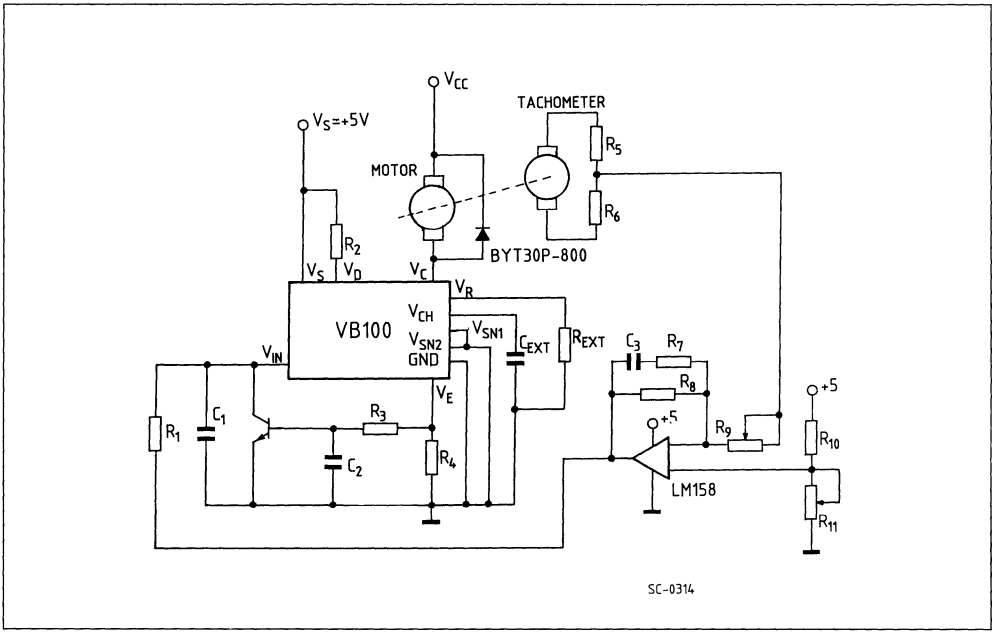
$$t_{ON} = t_s + t_f + t_r + 0.91 \times \frac{R_{EXT.} \times C_{EXT.}}{(V_{CHH} - V_{CHL})} \times V_{IN}$$

in the range:

$0.5Hz < f_{osc.} < 5\ kHz$ with $V_{SN} = 0$
$0.5Hz < f_{osc.} < 20\ kHz$ with $V_{SN} = -5\ V$

If an inductive load is used, it is necessary to provide a current limiting circuit. The device can form part of a closed loop control by just adding a few external components; fig. 5 shows a typical application example.

Fig. 5 Application Circuit



$R_1 = 100$
$R_2 = 33\ \Omega$
$R_3 = 1\ k\Omega$
$R_4 = 0.15\ \Omega$
$R_5 = 100\ k\Omega$
$R_6 = 1.8\ k\Omega$
$R_7 = 2\ k\Omega$
$R_8 = 100\ k\Omega$
$R_9 = 50\ k\Omega$
$R_{10} = 3.3\ k\Omega$
$R_{11} = 4.7\ k\Omega$
$R_{EXT} = 50\ k\Omega$
$C_1 = 1\ nF$
$C_2 = 1\ nF$
$C_3 = 33\ nF$
$C_{EXT} = 1.8\ nF$

PACKAGES

DESIGNING WITH THERMAL IMPEDANCE

by T. Hopkins, C. Cognetti, R. Tiziani

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ABSTRACT

Power switching techniques used in many modern control systems are characterized by single or repetitive power pulses, which can reach several hundred watts each. In these applications where the pulse width is often limited to a few milliseconds, cost effective thermal design considers the effect of thermal capacitance. When this thermal capacitance is large enough, it can limit the junction temperature to within the ratings of the device even in the presence of high dissipation peaks. This paper discusses thermal impedance and the main parameters influencing it. Empirical measurements of the thermal impedance of some standard plastic packages showing the effective thermal impedance under pulsed conditions are also presented.

INTRODUCTION

Power switching applications are becoming very common in many industrial, computer and automotive ICs. In these applications, such as switching power supplies and PWM inductive load drivers, power dissipation is limited to short times, with single or repeated pulses. The normal description of the thermal performance of an IC package, Rth (j-a) (junction to ambient thermal resistance), is of little help in these pulsed applications and leads to a redundant and expensive thermal design.

This paper will discuss the thermal impedance and the main factors influencing it in plastic semiconductor packages. Experimental evaluations of the thermal performance of small signal, medium power, and high power packages will be presented as case examples. The effects of the thermal capacitance of the packages when dealing with low duty cycle power dissipation will be presented and evaluated in each of the example cases.

THERMAL IMPEDANCE MODEL FOR PLASTIC PACKAGES

The complete thermal impedance of a device can be modeled by combining two elements, the thermal resistance and the thermal capacitance.

The thermal resistance, Rth, quantifies the capability of a given thermal path to transfer heat. The general definition of resistance of the thermal path, which includes the three different modes of heat dissipation (conduction, convection and radiation), is the ratio between the temperature increase above the reference and the heat flow, ΔP, and is given by the equation:

$$R_{th} = \frac{\Delta T}{\Delta P} = \frac{\Delta T}{\frac{\Delta Q}{\Delta t}}$$

where: ΔQ = heat
Δt = time

Thermal capacitance, C_{th}, is a measure of the capability of accumulating heat, like a capacitor accumulates a charge. For a given structural element, C_{th} depends on the specific heat, c, volume V, and density d, according to the relationship:

$$C_{th} = c\ d\ V$$

The resulting temperature increase when the element has accumulated the heat Q, is given by the equation:

$$\Delta T = \Delta Q / C_{th}$$

The electrical analogy of the thermal behavior for a given application consisting of an active device, package, printed circuit board, external heat sink and external ambient is a chain of RC cells, each having a characteristic time constant:

$$\tau = R\ C$$

To show how each cell contributes to the thermal impedance of the finished device consider the simplified example shown in figure 1. The example device consists of a dissipating element (integrated circuit) soldered on a copper frame surrounded by a plastic compound with no external heat sink. Its equivalent electrical circuit is shown in figure 2.

Fig. 1 - Simplified Package Outline

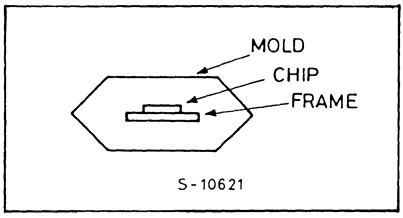
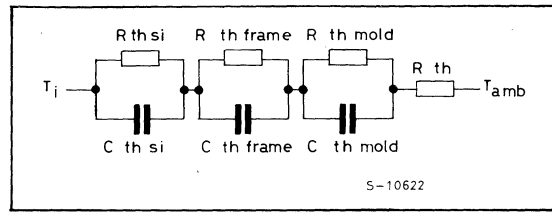


Fig. 2 - Equivalent Thermal Circuit of Simplified Package



The first cell, shown in figure 2, represents the thermal characteristics of the silicon itself and is characterized by the small volume with a correspondingly low thermal capacitance, in the order of a few mJ/°C. The thermal resistance between the junction and the silicon/slug interface is of about 0.2 to 2 °C/W, depending on die size and on the size of the dissipating elements existing on the silicon. The time constant of this cell is typically in the order of a few milliseconds.

The second cell represents the good conductive path from the silicon/frame interface to the frame periphery. In power packages, where the die is often soldered directly to the external tab of the package, the thermal capacitance can be large. The time constant for this cell is in the order of seconds.

From this point, heat is transferred by conduction to the molded block of the package, with a large thermal resistance and capacitance. The time constant of the third cell is in the order of hundreds of seconds.

After the plastic has heated, convection and radiation to the ambient starts. Since a negligible capacitance is associated with this phase, it is represented by a purely resistive element.

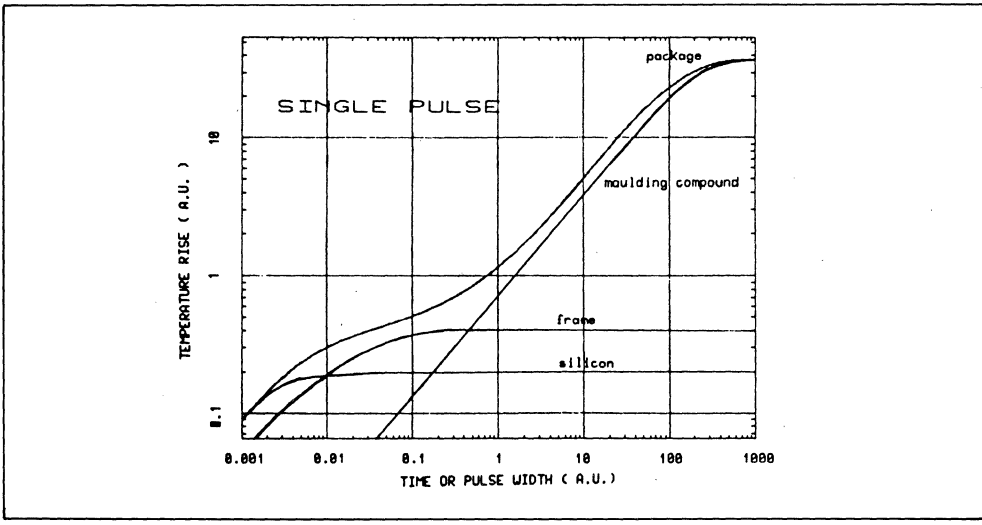
When power is switched on, the junction temperature increase is ruled by the heat accumulation in the cells, each following its own time constant according with the equation:

$$\Delta T = R_{th}\, P_d\, [1 - e^{(t/\tau)}]$$

The steady state junction temperature, T_j, is a function of the $R_{th\ (j\ -\ a)}$ of the system, but the temperature increase is dominated by thermal impedance in the transient phase, as is the case in switching applications.

A simplified example of how the time constants of each cell contribute to the temperature rise is shown in figure 3 where the contribution of the cells of figure 2 is exaggerated for a better understanding.

Fig. 3 - Time Constant Contribution of Each Thermal Cell (Qualitative Example)



When working with actual packages, it is observed that the last two sections of the equivalent circuit are not as simple as in this model and possible changes will be discussed later. However, with switching times shorter than few seconds, the model is sufficient for most situations.

EXPERIMENTAL MEASUREMENTS

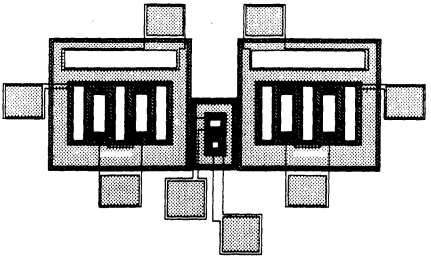
When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method. At present, only draft specifications exist, proposed last year and not yet standardized (1).

The experimental method used internally for evaluations since 1984 has anticipated these preliminary recomendations to some extent, as it is based on test patterns having, as dissipating element, two power transistors and, as measurement element, a sensing diode placed in the thermal plateau arising when the transistors are biased in parallel.

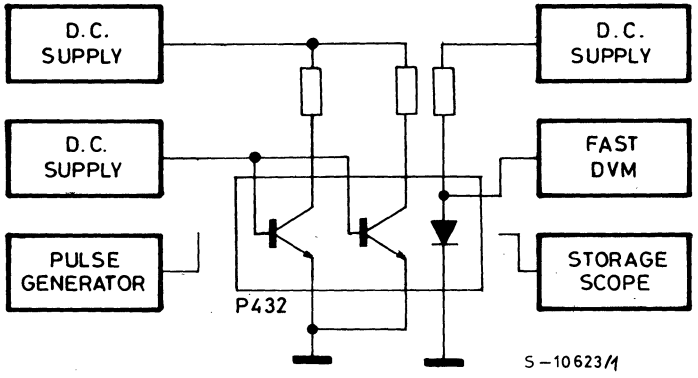
The method used has been presented elsewhere (2) for the pattern P432 (shown in figure 4), which uses two small (1000 sq mils) bipolar power transistors and has a maximum DC power capability of 40W (limited by second breakdown of the dissipating elements).

A similar methodology was followed with the new H029 pattern, based on two D-Mos transistors (3) having a total size of 17,000 sq mils and a DC power capability of 300 W on an infinite heat sink at room temperature (limited by thermal resistance and by max operating temperature of the plastics).

Fig. 4



a) P432 Test Die

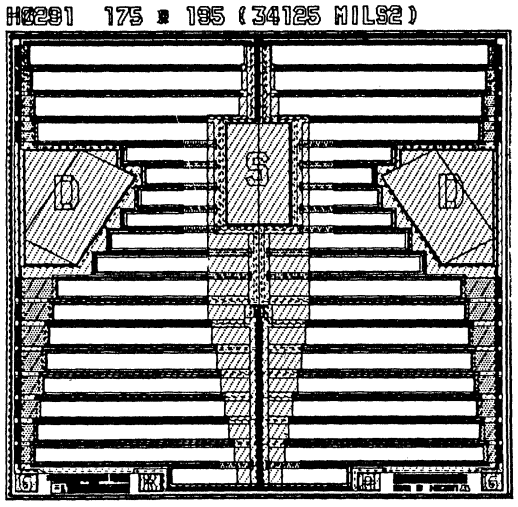


b) P432 Measurement System

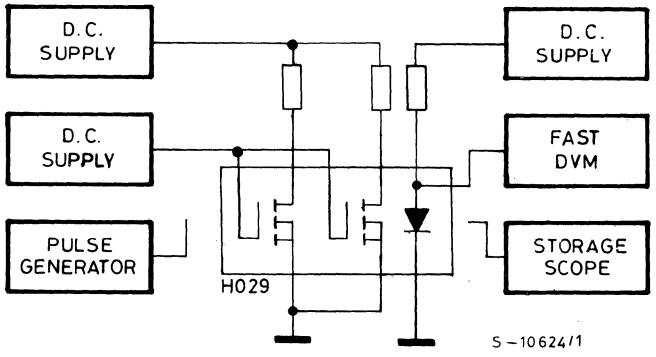
Using the thermal evaluation die, four sets of measurements were performed on an assortment of insertion and surface mount packages produced by SGS-Thomson Microelectronics. The complete characterization is available elsewhere (4). The four measurements taken were:

1) Junction to Case Thermal Resistance (Power Packages)
2) Junction to Ambient Thermal Resistance
3) Transient Thermal Impedance (Single Pulse)
4) Peak Transient Thermal Impedance (Repeated Pulses)

Fig. 5

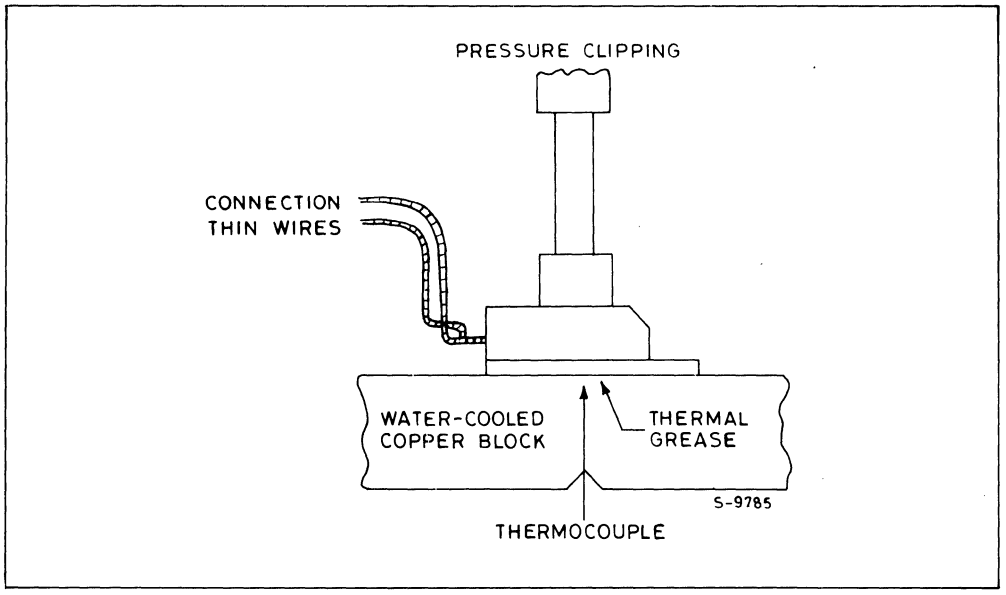


a) H029 Test Die



b) H029 Measurement System

Fig. 6 - Set-up for $R_{th\ (j\ -\ c)}$ Measurement

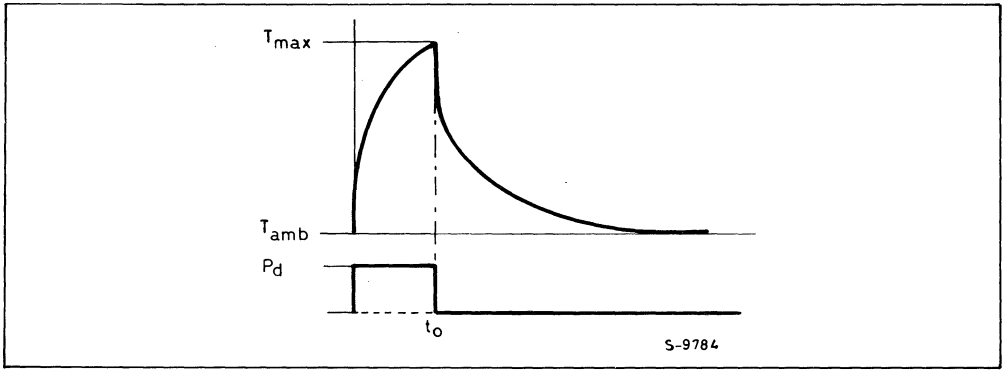


The junction to case thermal resistance measurements were taken using the well known setup shown in figure 6 where the power device is clamped against a large mass of controlled temperature.

The junction to ambient thermal resistance in still air, was measured with the package soldered on standard test boards, described later, and suspensed in 1 cubic foot box, to prevent air movement.

The single pulse transient thermal impedance was measured in still air by applying a single power pulse of duration t_0 to the device. The exponential temperature rise in response to the power pulse is shown qualitetively in figure 7. In the presence of one single power pulse the temperature, ΔT_{max}, reached at time t_0, is lower than the steady state temperature calculated from the junction to ambient thermal resistance. The transient thermal impedance R_O, is obtained from the ratio $\Delta T_{max}/P_d$.

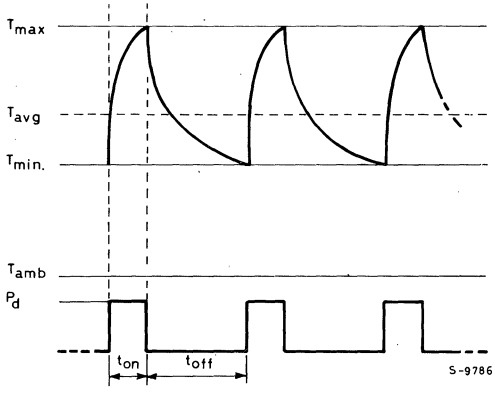
Fig. 7 - Transient Thermal Response for a Single Pulse



The peak transient thermal impedance for a series of repetitive pulses was measured by applying a string of power pulses to the device in free air. When power pulses of the same height, P_d, are repeated with a given duty cycle, DC, and the pulse length, t_p, is shorter than the total time constant of the system, the train of pulses is seen as a continuous source with mean power level given by the equation:

$$P_{davg} = P_d \, DC$$

Fig. 8 - Transient Thermal Response for Repetitive Pulses



On the other hand, the silicon die has a thermal time constant of 1 to 2 ms and the die temperature is able to follow frequencies of some kHz. The result is that T_j oscillates about the average value:

$$\Delta T_{javg} = R_{th} \, P_{davg}$$

The resulting die temperature excursions are shown qualitatively in figure 8. The peak thermal impedance, R_{thp}, corresponding to the peak temperature, ΔT_{max}, at the equilibrium can be defined:

$$R_{thp} = \Delta T_{max}/P_d = F\,(t_p, DC)$$

The value of R_{thp} is a function of pulse width and duty cycle. Knowledge of R_{thp} is very important to avoid a peak temperature higher than specificed values (usually 150°C).

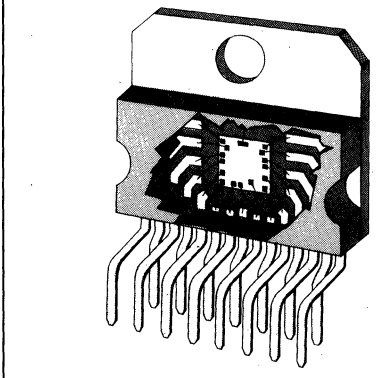
EXPERIMENTAL RESULTS

The experimental measurements taken on several of the packages tested are summarized in the following sections.

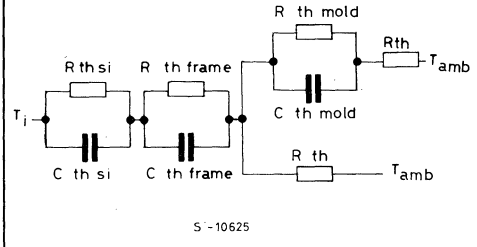
MULTIWATT Package

The MULTIWATT (R) package, shown in figure 9a, is a multileaded power package in which the die is attached directly to the tab of package using a soft solder (Pb/Sn) die attach. The tab of the package is a 1.5 mm thick copper alloy slug. The thermal model of the MULTIWATT, shown in figure 9b, is not much different from that shown in figure 2. The main difference being that when heat reaches the edge of the slug, two parallel paths are possible; conduction towards the molding compound, and convection and radiation towards the ambient. After a given time, convection and radiation taked place from the plastic.

Fig. 9



a) MULTIWATT assembly



b) Equivalent Thermal Circuit

Using the two test die, the measured junction to case thermal resistance is:

P432 $R_{th\,(j-c)} = 2°C/W$
H029 $R_{th\,(j-c)} = 0.4°C/W$

The measured time constant is approximately 1 ms for each of the two test patterns, but the two devices have a different steady state temperature rise.

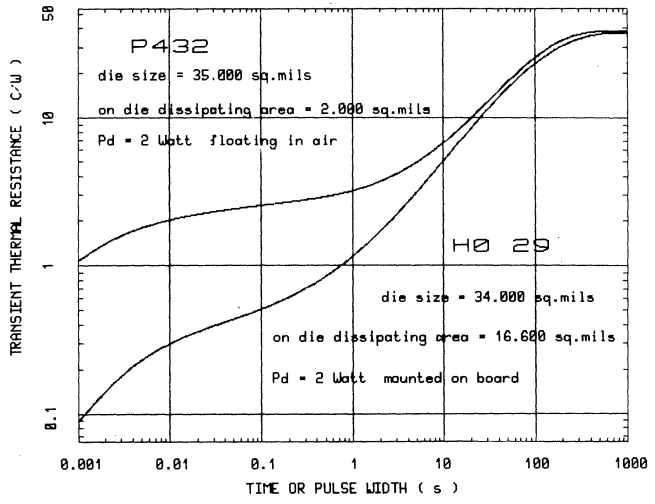
The second cell shown in figure 9 is dominated by the large thermal mass of the slug. The thermal resistance of the slug, R_{thslug} is about 1°C/W and the thermal time constant of the slug is in the order of 1 second.

The third RC cell in the model has a long time constant due to the mass of the plastic molding and its low thermal conductivity. For this cell the steady state is reached after hundreds of seconds.

For the MULTIWATT the DC thermal resistance of the package in free air, $R_{th\ j-a}$, is 36°C/W with the P432 die and 34.5°C/W with the H029 die.

Figure 10 shows the single pulse transient thermal impedance for the MULTIWATT with both the P432 and H029 test die. As can be seen on the graph, the package is capable of high dissipation for short periods of time. For a die like the H029 the power device is capable of 700 to 800 W for pulse widths in the range of 1 to 10 ms. For times up to a few seconds the effective thermal resistance for a single pulse is still in the range of 1 to 3°C/W.

Fig. 10 - Transient Thermal Response MULTIWATT Package



The peak transient thermal impedance for the MULTIWATT package containing the P432 die in free air is shown in figure 11.

Power DIP Package

The power DIP package is a derivative of standard small signal DIP packages with a number of leads connected to the die pad for heat transfer to external heat sinks. With this technique low cost heat sinks can be integrated on the printed circuit board as shown in figure 12a. The thermal model of the power DIP, shown in figure 12b accounts for the external heat sink on the circuit board by adding a second RC cell in parallel with the cell corresponding to the molding compound.

In this model, the second cell has a shorter time constant than for the MULTIWATT package, due in large part to the smaller quantity of copper in the frame (the frame thickness is 0.4 mm compared to 1.5 mm). Thus the capacitance is reduced and the resistance increased.

The increased thermal impedance due to the frame can partially be compensated by a better thermal exchange to the ambient by adding copper to the heat sink on the board. The DC thermal resistance between the junction and ambient can be reduced to the same range as the MULTIWATT package in free air, as shown in figure 13.

Fig. 11 - Peak Thermal Resistance MULTIWATT Package

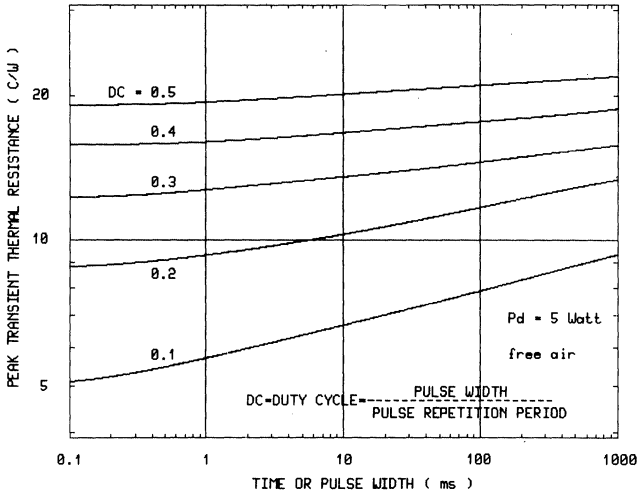
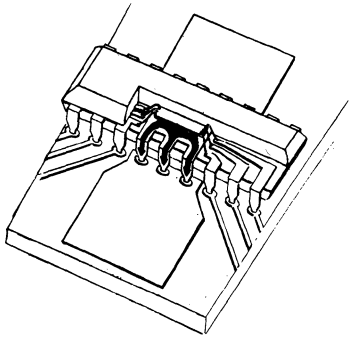
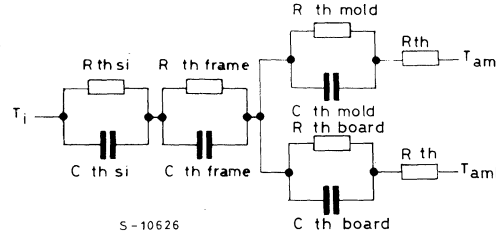


Fig. 12

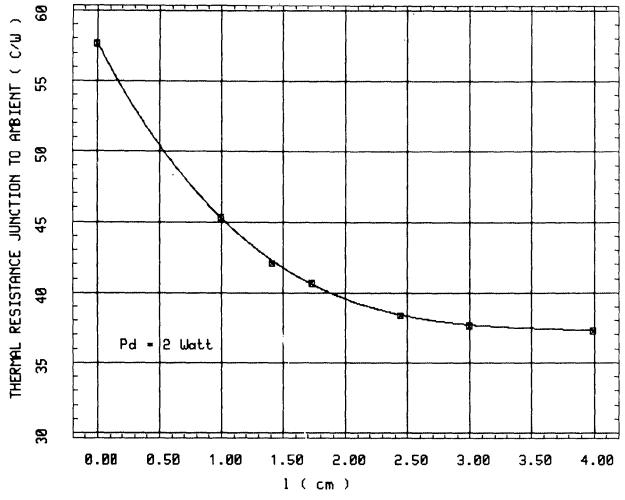


a) Power DIP Package



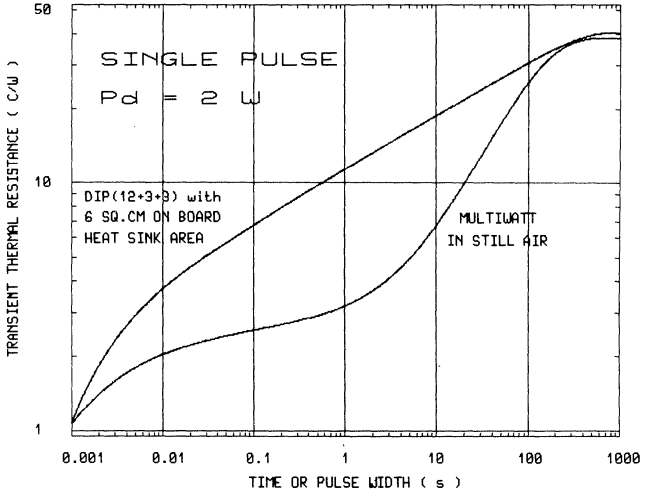
b) Equivalent Thermal Circuit

Fig. 13 - Rth (j - a) vs. PCB Heat Sink Size 12 + 3 + 3 Power Dip



As a comparison, figure 14 compares the thermal performance of the power DIP and the MULTIWATT package. It is clearly seen that even though the DC thermal resistance may be similar, the MULTIWATT is superior in its performance for pulsed applications.

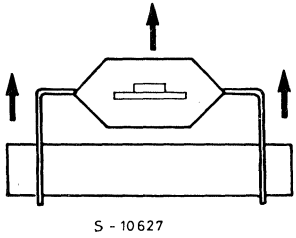
Fig. 14 - Transient Thermal Impedance for Single Pulses in Power DIP and MULTIWATT Packages



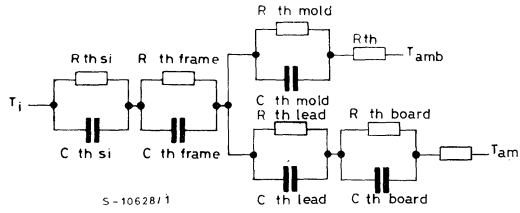
Standard Signal Packages

In standard, small signal, packages the easiest thermal path is from the die to the ambient through the molding compound. However, if a high conductivity frame, like a copper lead frame, is used another path exists in parallel. Figure 15 shows the equivalent thermal model of such a package. The effectiveness of a copper frame in transferring heat to the board can be seen in the experimental results in DC conditions.

Fig. 15



a) DIP Package Mounted on PCB



b) Equivalent Thermal Circuit DIP Package on PCB

Table 1 shows the thermal resistance of some standard signal packages in two different conditions; with the device floating in still air connected to the measurement circuit by thin wires and the same device soldered on a test board.

Table 1 - Thermal Resistance of Signal Packages

Package	Frame Thickness & Material	Rth (j-a) floating	°C/W on board
DIP 8	(0.4 mm Copper)	125-165	78-90
DIP 14	(0.4 mm Copper)	98-128	64-73
DIP 16	(0.4 mm Copper)	95-124	62-71
DIP 20	(0.4 mm Copper)	85-112	58-69
DIP 14	(0.25 mm Copper)	115-147	84-95
DIP 20	(0.25 mm Copper)	100-134	76-87
DIP 24	(0.25 mm Copper)	67-84	61-68
DIP 20	(0.25 mm Alloy 42)	158-184	133-145
SO 14	(0.25 mm Copper)	218-250	105-180
PLCC 44	(0.25 mm Copper)	66-83	48-72

The transient thermal resistance for single pulses for the various packages are shown in figures 16 through 20.

The results of the tests, as shown in the preceding figures, show the true capabilities of the packages. For example, the DIP 20 with a Alloy 42 frame is a typical package used for signal processing applications and can dissipate only 0.5 to 0.7 W in steady state conditions. However, the transient thermal impedance for short pulses is low (11°C/W for t_p = 100 ms) and almost 7 Watts can be dissipated for 100 ms while keeping the junction temperature rise below 80°C.

The packages using a 0.4 mm Copper frame have a low steady state thermal resistance, especially in the case of the DIP 20. The thicker lead frame increases the thermal capacitance of the die flag, which greatly improves the transient thermal impedance. In the case of the DIP 20, which has the largest die pad, the transient R_{th} for 100 ms pulses is about 4.3°C/W. This allows the device to dissipate an 18 Watt power pulse while keeping the temperature rise below 80°C.

As with the previous examples the peak transient thermal impedance for repetitive pulses depends on the pulse length and duty cycle as shown in figure 14. With the signal package, however, the effect of the duty cycle becomes much less effective for longer pulses, due primarily to the lower thermal capacitance and hence lower time constant of the frame.

Fig. 16 - Transient Thermal Impedance DIP 20 (Alloy 42)

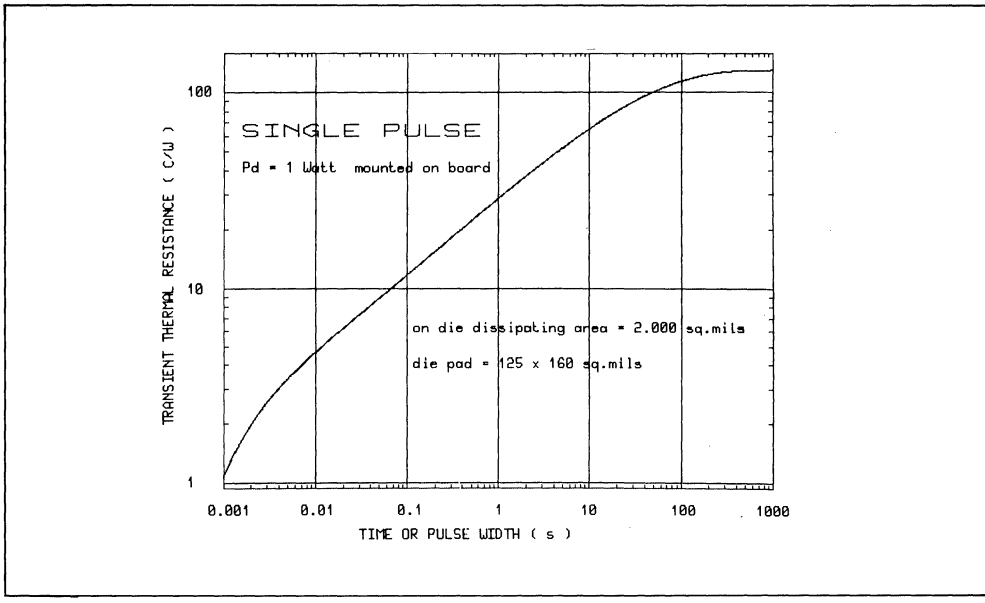


Fig. 17 - Transient Thermal Impedance 0.4 mm Copper Frame DIP Packages

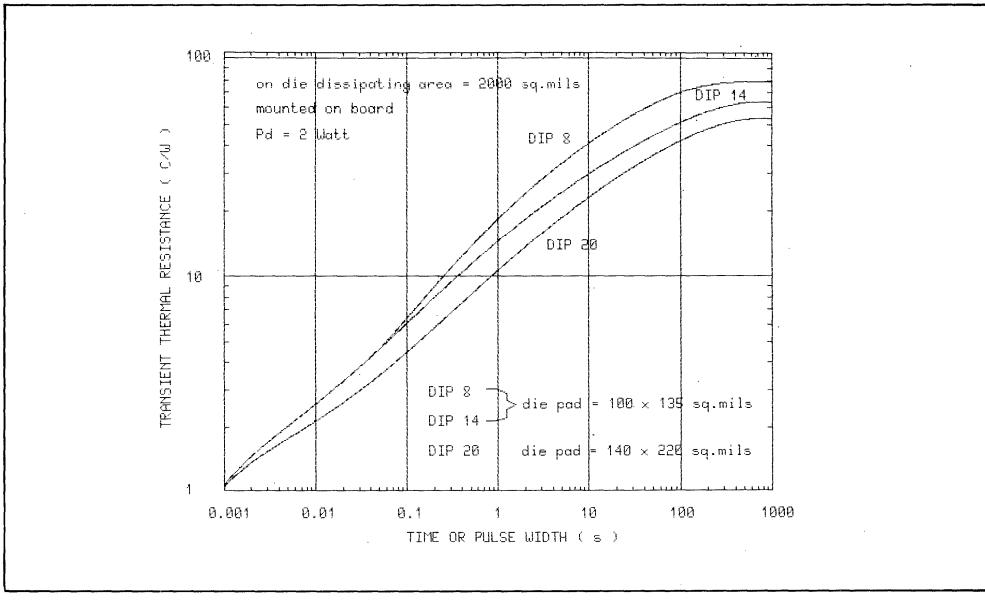


Fig. 18 - Transient Thermal Impedance 0.25 mm Copper Frame DIP Packages

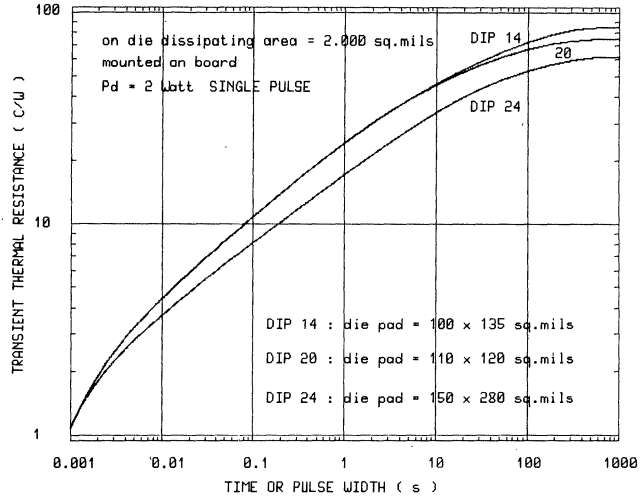


Fig. 19 - Transient Thermal Impedance 0.25 mm Frame PLCC Package

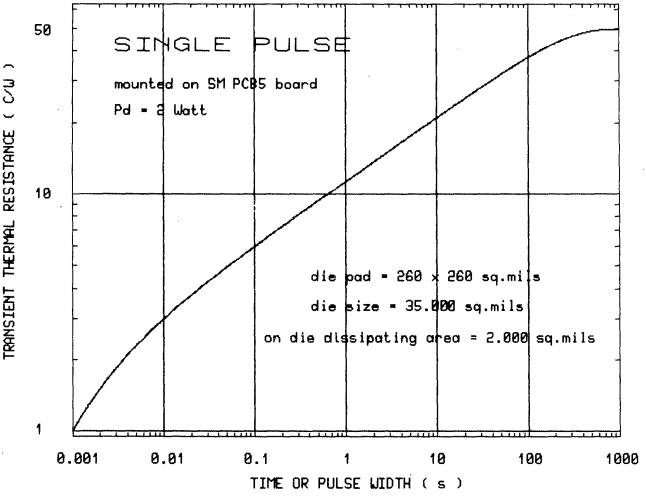


Fig. 20 - Transient Thermal Impedance 0.25 mm Copper Frame SO14 Package

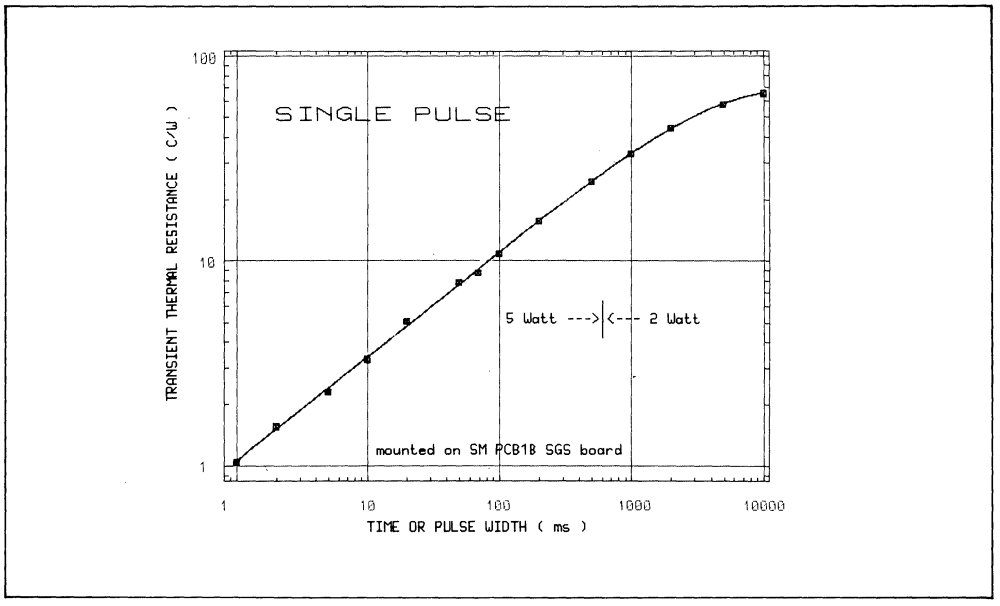
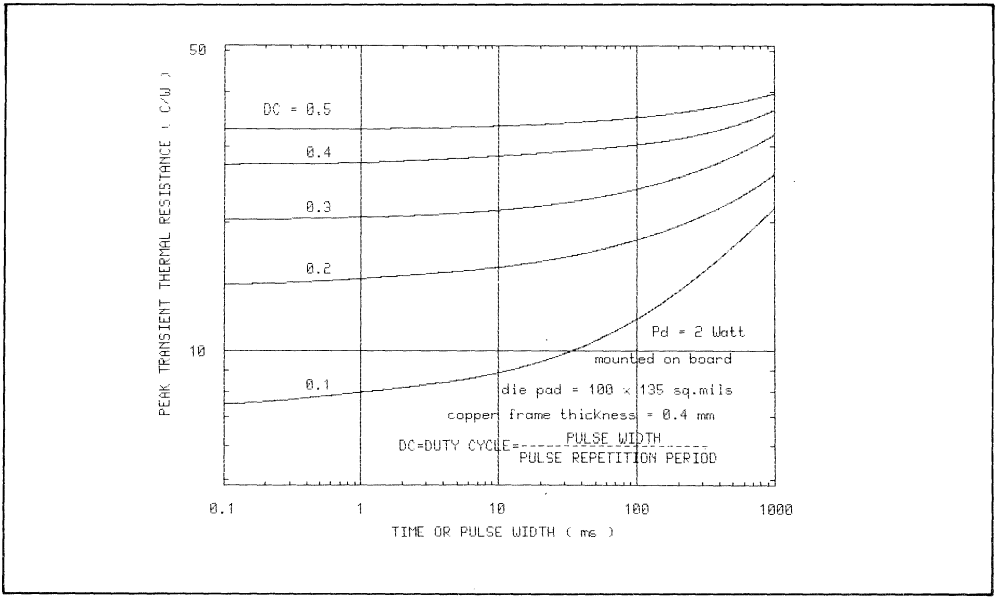


Fig. 21 - Peak Thermal Impedance 0.25 mm Copper Frame 14 Lead DIP



CONCLUSION

This paper has discussed a test procedure for measuring and quantifying the thermal characteristics of semiconductor packages. Using these test methods the thermal impedance of standard integrated circuit packages under pulsed and DC conditions were evaluated. From this evaluation two important considerations arise:

1) The true thermal impedance under repetitive pulsed conditions needs to be considered to maintain the peak junction temperature within the rating for the device. A proper evaluation will result in junction temperatures that do not exceed the specified limits under either steady state or pulsed conditions.

2) The proper evaluation of the transient thermal characteristics of an application should take into account the ability to dissipate high power pulses allowing better thermal design and possibly reducing or eliminating expensive external heat sinks when they are oversized or useless.

REFERENCES

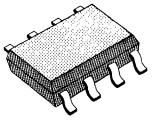
(1) SEMI Draft Specifications 1377 and 1449, 1986

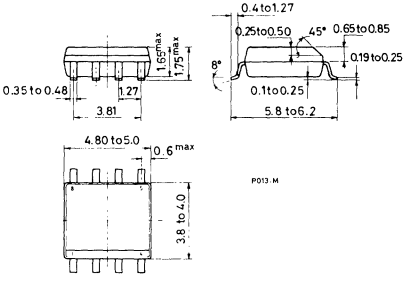
(2) T. Hopkins, R. Tiziani, and C. Cognetti, "Improved thermal impedance measurements by means of a simple integrated structure", presented at SEMITHERM 1986

(3) C. Cini, C. Diazzi, D. Rossi and S. Storti, "High side monolithic switch in Multipower-BCD technology", Proceedings of Microelectronics Conference, Munchen, November 1986

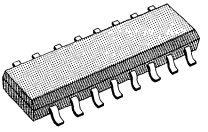
(4) Application Notes 106 through 110, SGS-THOMSON Microelectronics, 1987

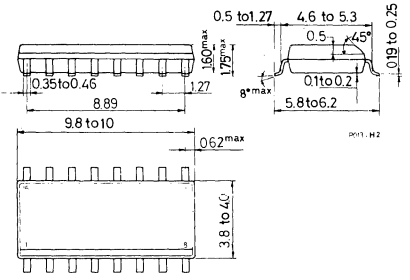
SO-8J



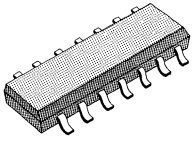


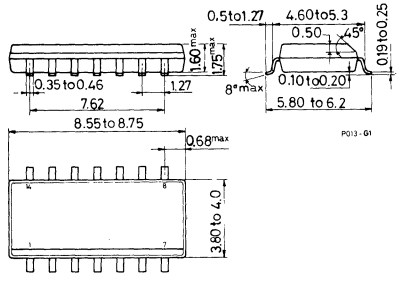
SO-16J



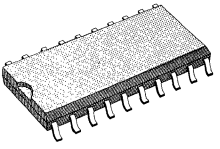


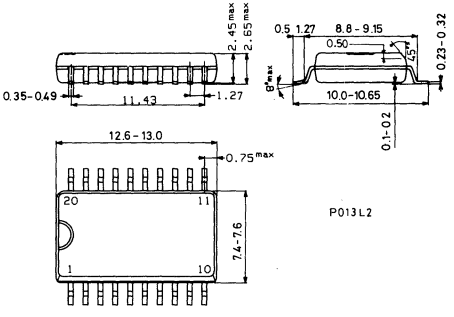
SO-14J



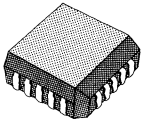


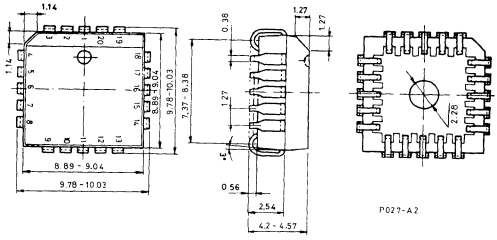
SO-20L
SO-20 (12+4+4)



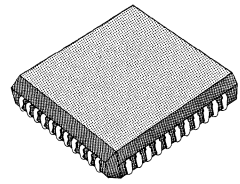


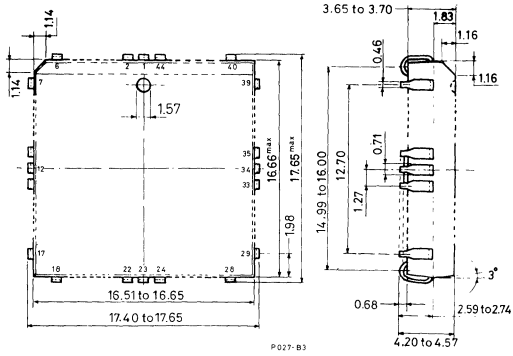
PLCC - 20 Plastic Chip Carrier
PLCC 15 + 5





PLCC - 44 Plastic Chip Carrier





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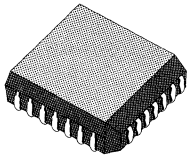
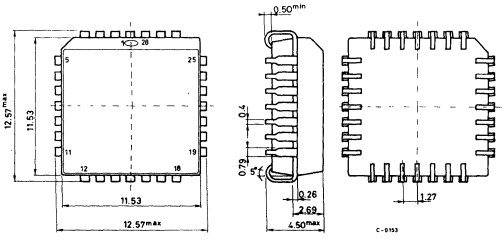
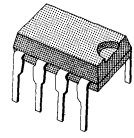
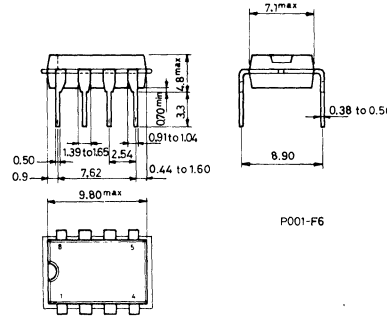




8 lead Plastic Minidip
4+4 lead Powerdip





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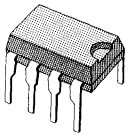
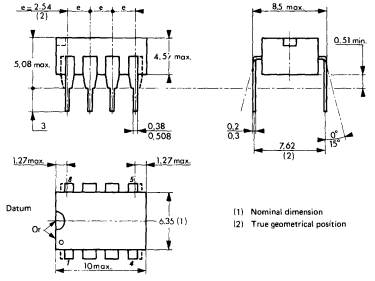
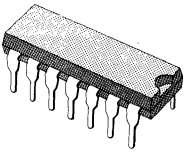
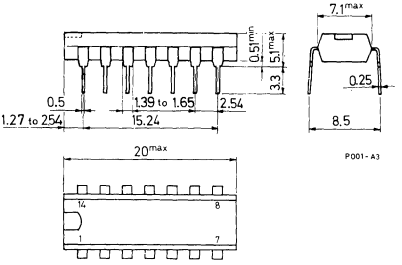


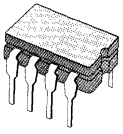


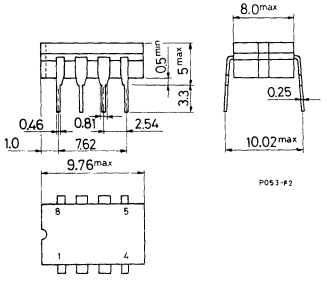
14 lead Plastic Dip





8 lead Ceramic Minidip





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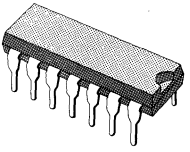
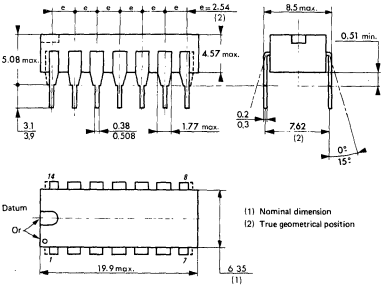
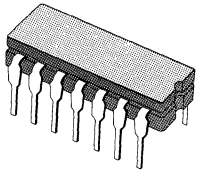
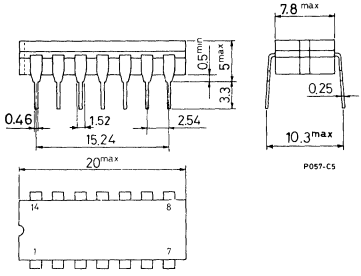




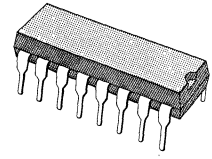
PACKAGES

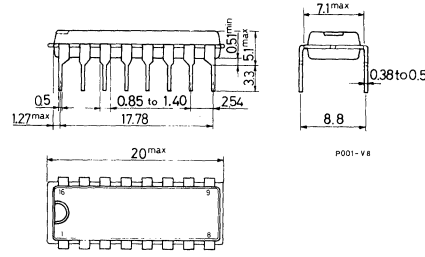
14 lead Ceramic Dip



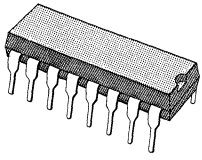


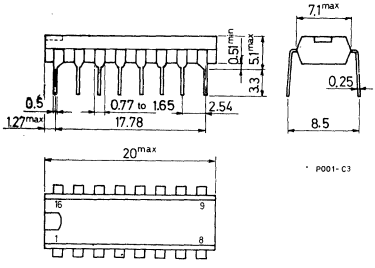
16 lead Plastic Dip (0.4)
8+8 lead Powerdip
12+2+2 lead Powerdip



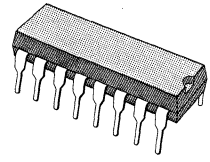


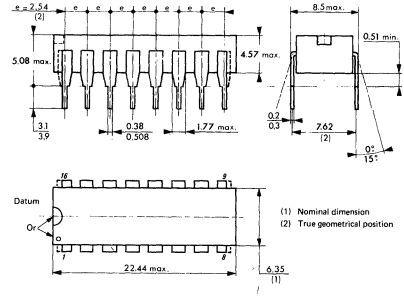
16 lead Plastic Dip (0.25)



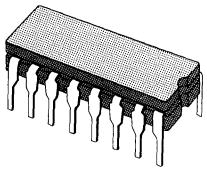


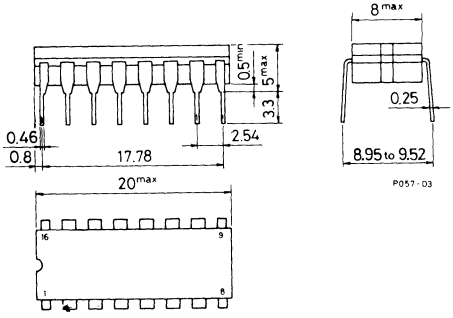
16 lead Plastic Dip/2



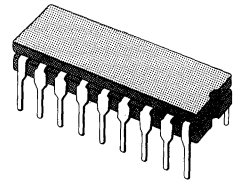


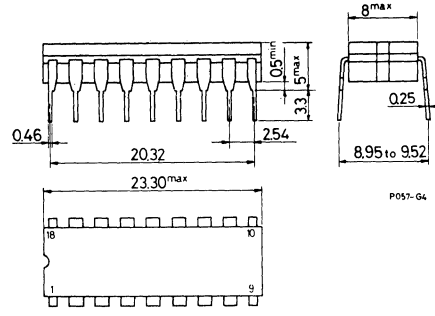
16 lead Ceramic Dip



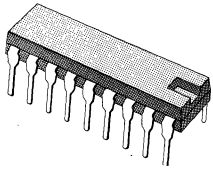


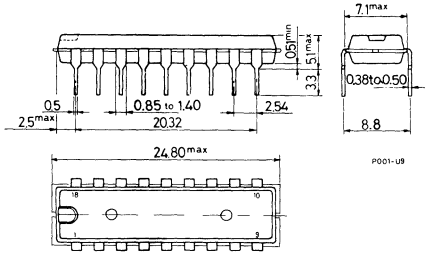
18 lead Ceramic Dip



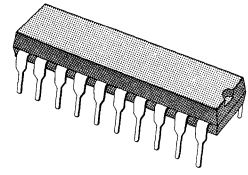


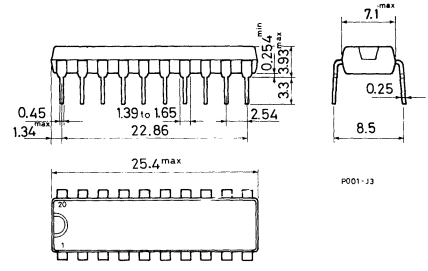
18 lead Plastic Dip
12+3+3 lead Powerdip





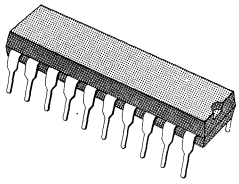
20 lead Plastic Dip (0.25)

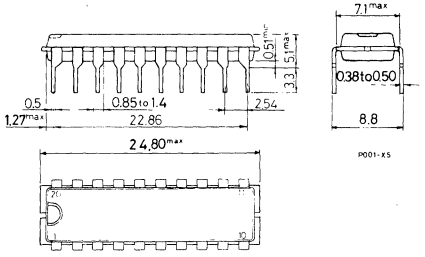




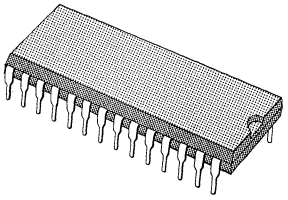
PACKAGES

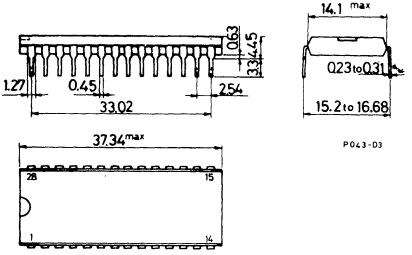
20 lead Plastic Dip (0.4)
16+2+2 Powerdip
14+3+3 Powerdip





28 lead Plastic Dip





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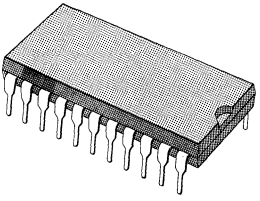

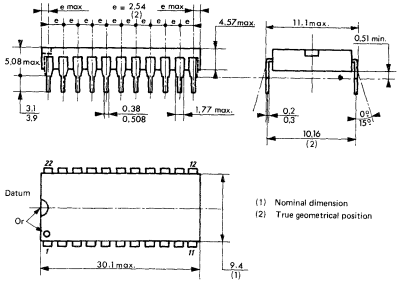

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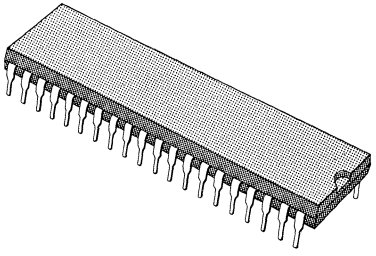

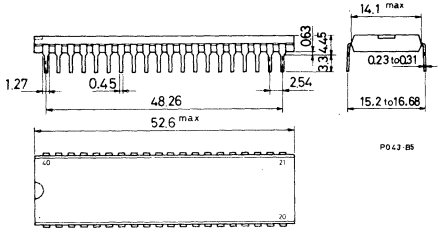

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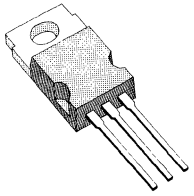

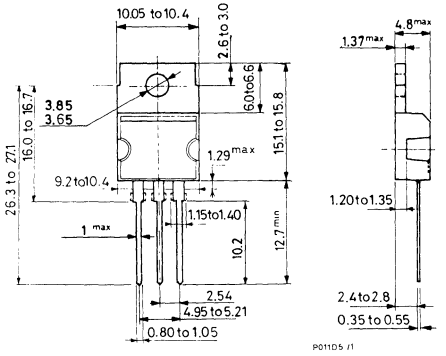

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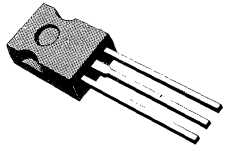
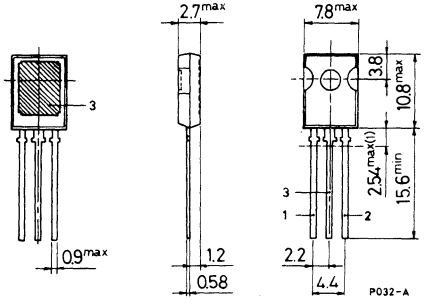
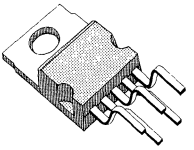




(1) Within this region the cross-section of the leads is uncontrolled

PENTAWATT



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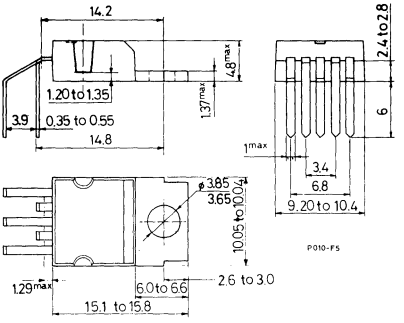

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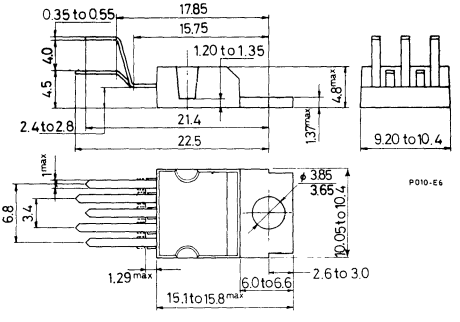
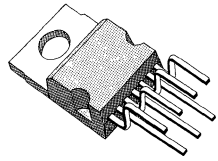


PACKAGES

HEPTAWATT



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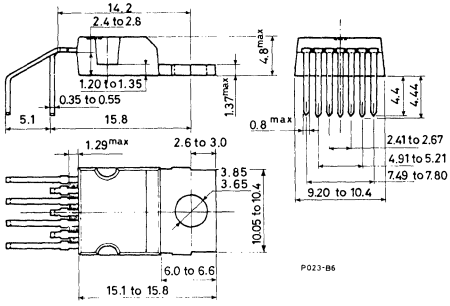

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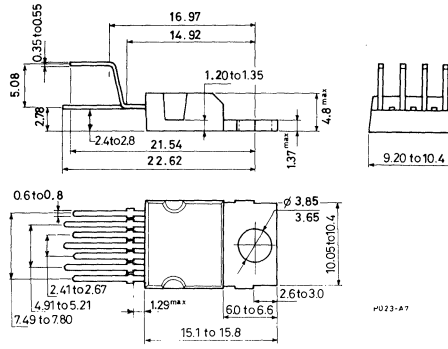

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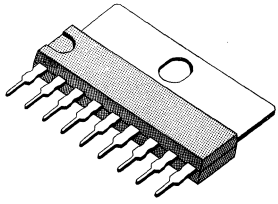
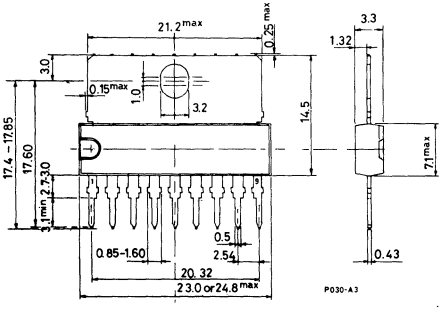
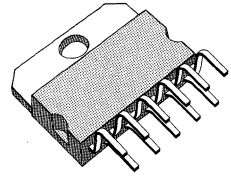
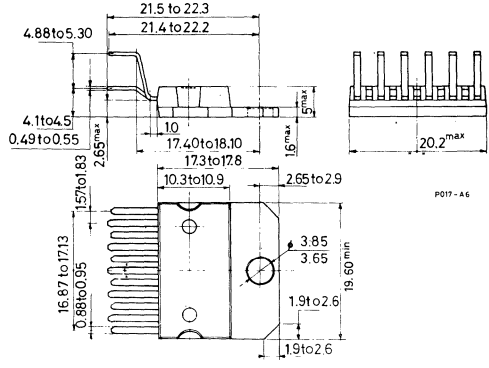




MULTIWATT-11





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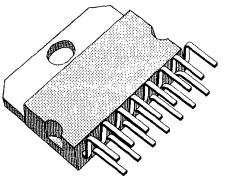
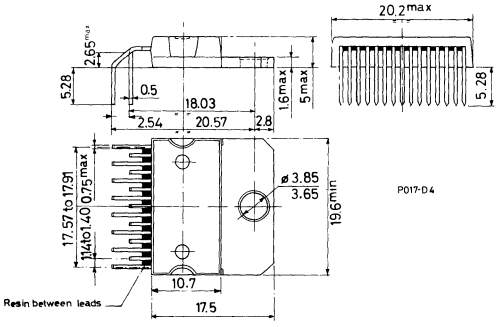
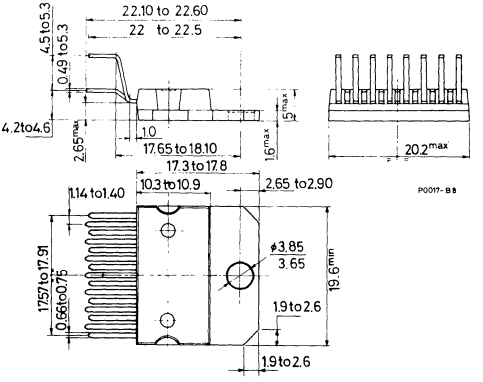


Horizontal Version



Vertical Version



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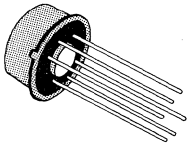

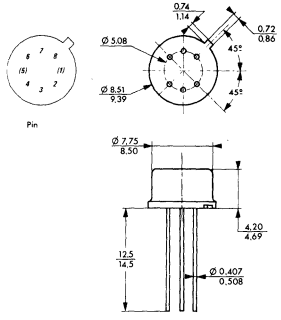

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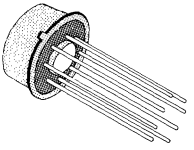

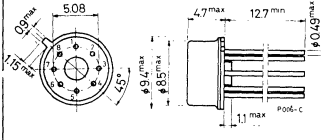

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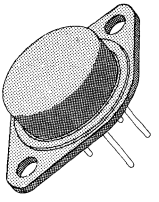

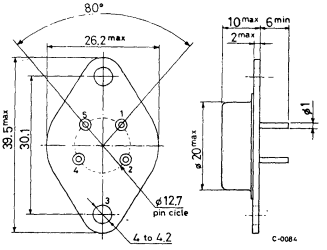

NOTES

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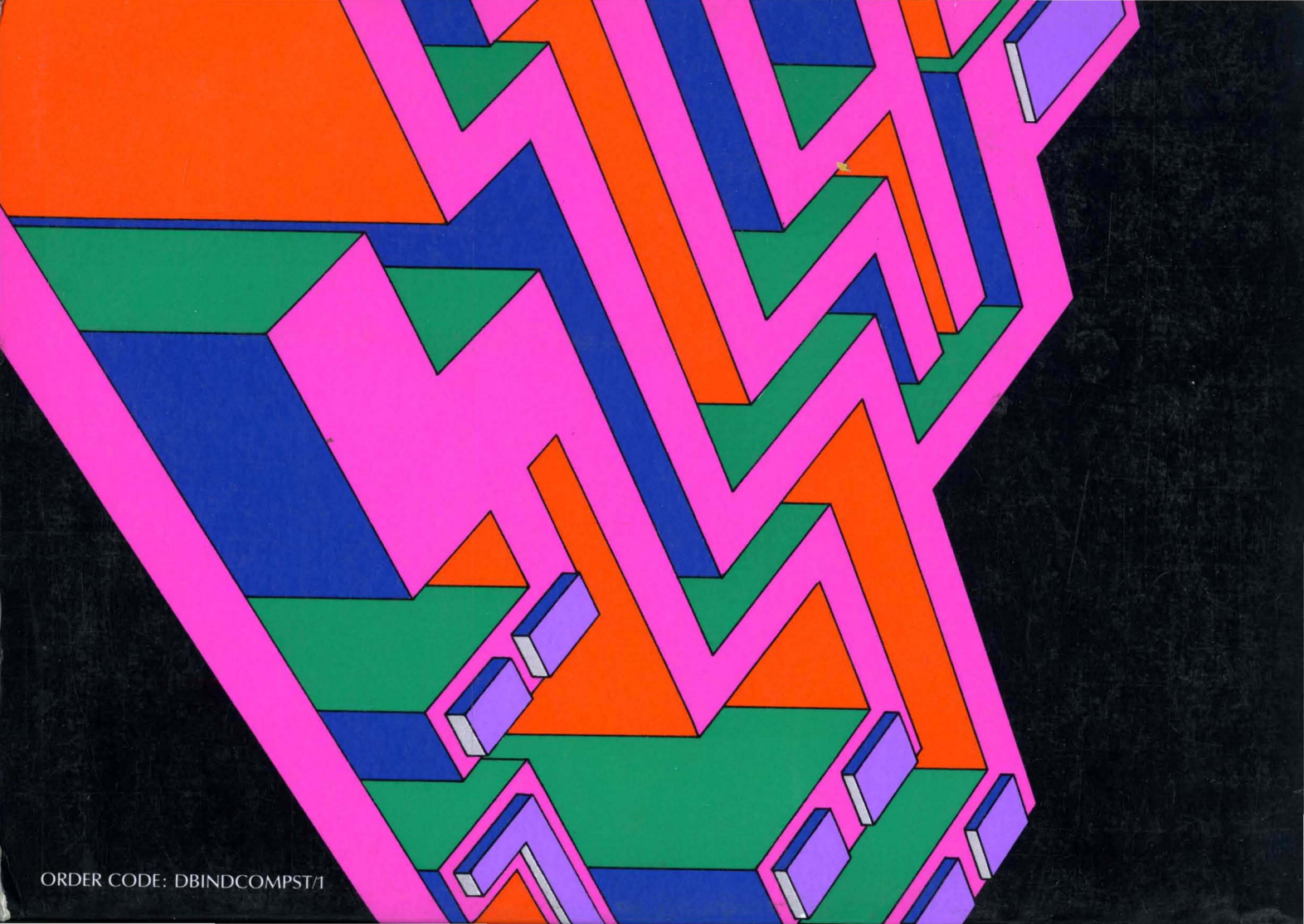

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